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MEMORY MAP UNIT, INTERDATA 7/16 HSALU:
DESCRIPTION AND INSTRUCTIONS

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MEMORY MAP UNIT, INTERDATA 7/16 HSALU: DESCRIPTION AND INSTRUCTIONS

ABSTRACT

The Memory Map Unit (MMU) provides the capability for an Interdata 7/16 computer with High Speed Arithmetic Logic Unit (HSALU) to operate with up to 256K bytes of memory (1K = 1024). Memory addresses, consisting of 16 bits, are mapped into 18 bits whenever a memory cycle occurs. Mapping occurs by 1K pages; selectable low-address areas are not mapped.

GENERAL DESCRIPTION OF THE MEMORY MAP UNIT

The Memory Map Unit (MMU) is constructed on an Interdata 48-013 Universal Logic Interface (ULI) board that is plugged into slot 4 of the processor card bin. This slot is used by the 7/32 computer for the Memory Access Controller. A number of back plane wiring changes must be made and are detailed in a separate section.

Basically, the unit contains three memory maps, each consisting of a 64-word, 8-bit semiconductor memory. Two of the maps, the Task Map and the Interrupt Map, are used by the central processor unit (CPU); the third map is used by the Selector Channel (SELCH). Bit 11 of the Program Status Word (PSW) selects which of the two CPU maps to use. Ideally, the SELCH map would be constructed on the SELCH board, but fabrication problems prevent this alternative; the present design allows for the use of only one SELCH.

Generally, a portion of the computer memory must be reserved for system programs and parameters, as well as subroutines used by many tasks. To provide for such common areas, the map unit allows a selectable number of low address pages to be passed through the map unit without change. There are two such areas as determined by PSW bit 7, the Protect Mode bit. The unmapped area must be smaller when PSW bit 7 = 1 than when PSW bit 7 = 0.

PROGRAMMING THE MEMORY MAP UNIT

An Output Command (OC or OCR) instruction is used to turn the MMU on and off and to enable and disable the interrupts. The bit assignments are:

- Bit 0 = 1, bit 1 = 0: Disable interrupts
- Bit 0 = 0, bit 1 = 1: Enable interrupts
- Bit 0 = 1, bit 1 = 1: Disarm interrupts
- Bit 0 = 0, bit 1 = 0: No change in interrupt status
- Bit 4 = 1, bit 5 = 0: Turn on MMU
- Bit 4 = 0, bit 5 = 1: Turn off MMU
- Bit 4 = 1, bit 5 = 1: Toggle the on/off state
- Bit 4 = 0, bit 5 = 0: No change in on/off state

The MMU generates an interrupt if it is on, interrupts are enabled, and a memory protect error occurs. A memory protect error occurs on a non-privileged memory write with PSW bit 7 = 1 if the memory address presented by the CPU is less than TSKBOT or the Task Map entry for the address is zero (PSW bit 11 = 0) or the Interrupt Map entry for the address is zero (PSW bit 11 = 1).

The status read on a Sense Status (SS or SSR) command is as follows:

Bit 2 = 1 if MMU is on

Bits 3 and 5 = 1 if a memory protect error occurs

Bits 3 and 5 are reset by the acknowledgement of an interrupt and by an OC or OCR instruction.

A Write Halfword (WH or WHR) command sends two parameters, LIBBOT and TSKBOT, to the MMU. Bits 0 through 7 of the halfword contain the eight most significant bits of the library bottom address (LIBBOT), and bits 8 through 15 contain the eight most significant bits of the task bottom address (TSKBOT). TSKBOT must be greater than or equal to LIBBOT. Only the six most significant bits of each address are actually used by the hardware since these six bits define the lowest 1K page which will be mapped. PSW bit 7 determines whether LIBBOT or TSKBOT is used.

The three maps are treated as memory locations; thus, they are loaded with any memory reference instruction. The hexadecimal addresses of the maps are:

300 - 33F	Task Map
340 - 37F	Interrupt Map
380 - 3BF	SELCH Map

The 64 bytes in each map provide a map for the 64 1K pages which may be addressed by the CPU or SELCH. Ordinarily, the maps are loaded with STH, STB, or STM commands. Core memory locations between X'300' and X'3BF' are loaded with the same information as the maps. If the core locations and map entries do not contain the same information as, for example, after a power failure, the data in core is copied to the maps by any memory reference instruction with an address between X'300' and X'3BF' (when the data is rewritten to core).

When the MMU is on, the following mappings occur:

If PSW bit 7 = 1 (PROTECT), the memory protect operates and all addresses at LIBBOT and above are mapped.

If PSW bit 7 = 0, the memory protect does not operate and all addresses at TSKBOT and above are mapped.

If PSW bit 11 = 0, the Task Map is used.

If PSW bit 11 = 1, the Interrupt Map is used.

If the SELCH requests a memory cycle, the SELCH map is used.

However, when the MMU is off, no mapping or memory protection occurs. The computer master clear signal, SCLR0, turns the MMU off and disarms the interrupts.

For the following examples of mapping, we assume that LIBBOT = X'1000', TSKBOT = X'8000', and that the MMU is on. All numbers in the following table are hexadecimal.

Location	Contents	CPU		Memory	
		Address	PSW7	PSW11	Address
324	45	9000	0	0	11400
324	45	9000	1	0	11400
364	26	9000	0	1	09800
364	26	9000	1	1	09800
306	1A	1800	0	0	01800
306	1A	1800	1	0	06800
346	21	1800	0	1	01800
346	21	1800	1	1	08400
301	32	0400	0	0	00400
301	32	0400	1	0	00400
341	43	0400	0	1	00400
341	43	0400	1	1	00400

In the first four examples, mapping always occurs because the CPU address is greater than TSKBOT. PSW11 determines which map is used. Figure 1 shows how CPU-address 9000 causes the contents of location 324 to be used as a page number to create memory address 11400. In the next four examples, mapping only occurs when PSW7 = 1 because the CPU address is between LIBBOT and TSKBOT. In the last four examples, no mapping occurs because the CPU address is less than LIBBOT.

□

Fig. 1. Example of mapping.

AN APPLICATION OF THE MEMORY MAP

The memory map unit has been used to enhance the operation of Interdata's Real Time Operating System (RTOS). Figure 2 shows how the virtual address space is used. The memory below LIBBOT contains data which must be available to the system whether running in the system mode (PROTECT on) or the task mode (PROTECT off); this data includes all the hardware-specified addresses (0 to X'2CF'), the maps, the Device Control Blocks (DCB's), the Channel Control Blocks (CCB's), any Program Status Word (PSW) swaps which could result in changing the PROTECT mode, and the termination queue. The address LIBBOT is determined by the number of bytes required for this unmapped area.

The remainder of the operating system and the reentrant library share the virtual address space between LIBBOT and TSKBOT. The operating system uses the address space when PROTECT is off, and the reentrant library uses the address space when PROTECT is on (when a task is running). Since tasks, including the reentrant library, generally do not access the operating system directly and since the operating system seldom accesses the reentrant library, this sharing of virtual address space places little limitation on the overall system. The address TSKBOT is determined by the size of the operating system or by the size of library plus system common, whichever is the larger. All tasks are loaded at the virtual address TSKBOT and may be any size up to 64K less TSKBOT (less the size of Task Common if used by the task).

Figure 3 shows the placement of the system components in core memory. The operating system resides at the bottom of memory with the reentrant library immediately above it. If Task Common is allocated before any tasks are loaded, it will be allocated just above the library. Tasks are loaded in the remainder of memory. Since the virtual task address space no longer matches the actual core address space, a task need not occupy contiguous core pages; thus, if a task requires eight pages, the RTOS Loader need only find eight pages somewhere in memory, not eight contiguous pages. This more efficient utilization of core memory results from a complete rewriting of the Supervisor Call (SVC) routines which allocate and release memory for tasks (including the Loader).

Fig. 2. Virtual address space.

Fig. 3. Core memory layout.

DESCRIPTION OF OPERATION

The flip-flop IC76-5 (1D8, page 1, section D8 of the schematic diagram in the Appendix) is set at the beginning of the memory cycle by ERO and is reset by INH0 going positive at the end of a memory cycle. The flip-flop is set for the portion of the memory cycle during which the memory address and data must be stable. The outputs of the flip-flop are used to hold the eight most significant bits of the memory address in the latches, IC's 87 and 98, so that the FMA000 through FMA070 signals are stable during the memory cycle. The MAR000 through MAR070 lines from the CPU may change during the memory cycle. The other seven bits, MA080 through MA140, do not change during a memory cycle.

The output of the 8-input gate, IC86-8 (1D6), goes to ground if any address between X'0300' and X'03FF' appears on the memory address lines. If IC86-8 is ground and PSEL0 is ground, indicating a processor memory cycle (not a SELCH memory cycle), LDMAPI goes positive at IC75-1 to indicate that data is to be entered into one of the maps.

Sixteen bits of data are actually written on any memory cycle; so, for example, if data is changed in either location X'300' or X'301', both X'300' and X'301' are rewritten. The memory data appears on the MD000 through MD150 lines (2B2-2A2) and is inverted to become MD001 through MD151. MD001 through MD071 appear at the even-numbered locations of all maps (IC's 97, 96, 84, and 83 in the Task Map), and MD081 through MD151 appear at the odd-numbered locations.

The address decoding for writing data into the maps occurs in IC's 131 (1C7), 109 (1C6), 118 (1B6), 108 (2C7), and the 7489 16-by-4 memory IC's (see Appendix A). IC's 109, 118 and 108 pass the MA100 through MA130 signals to their outputs when LDMAPI is positive. These four lines are decoded in each 7489 16-by-4 memory IC. IC131 decodes MA081, MA091, and MA141 according to the following table (the inversions, MA080, MA090, and MA140, actually appear at the IC):

MA081	MA091	MA141	OUTPUT	IC'S ENABLED
0	0	0	1Y3	97 84 95 82
0	0	1	1Y2	96 83 94 81
0	1	0	1Y1	129 140 127 138
0	1	1	1Y0	128 139 126 137
1	0	0	2Y3	105 114 103 112
1	0	1	2Y2	104 113 102 111

The indicated output goes to ground for 100 nsec. during the rewrite part of the core memory cycle due to the one shot IC79 (1C8). The ME and WE inputs of the memory IC's must both be ground in order to write data into them. Thus, any address between X'300' and X'3BF' causes data to be written into 4 memory IC's. For example, if FMA000 through FMA070 are 11111100 and MA080 through MA140 are 1000100, corresponding to addresses 0000001101110110 and 0000001101110111 (X'376' and X'377'), the 1Y0 output of IC131 goes to ground, and data is written into IC's 128, 139, 126, and 137 in the Interrupt Map.

When any address other than one between X'0300' and X'03FF' appears on the FMA lines, LDMAPI is ground, and IC's 109 and 118 pass the FMA000, FMA010, FMA020, and FMA030 signals through to the Task Map and Interrupt Map for decoding by the individual memory IC's. IC120 decodes the FMA041, FMA051, and

PSW271 signals according to the following table (FMA040 and FMA050 actually appear at the IC):

PSW271	FMA041	FMA051	OUTPUT	IC'S ENABLED
0	0	0	2Y3	97 84
0	0	1	2Y2	95 82
0	1	0	2Y1	96 83
0	1	1	2Y0	94 81
1	0	0	1Y3	129 140
1	0	1	1Y2	127 138
1	1	0	1Y1	128 139
1	1	1	1Y0	126 137

PSW27 corresponds to PSW11 in the programming discussion. PSW27 determines whether the Task Map or the Interrupt Map is used, and FMA04 and FMA05 determine which memory IC's are enabled within the map. The selected pair of memory IC's present their data (inverted) at IC's 93 (IC2), 142 (IC1), and 141 (1A1).

Meanwhile, the FMA000 through FMA050 lines are being compared to LIBBOT (inverted) and TSKBOT (inverted) at IC's 107, 117, 116, and 106 (1B7, 1A7). LIBBOT and TSKBOT are stored in flip-flops on the Interdata-provided portion of the board. If the memory address is less than LIBBOT, the MA<LIBBOT line goes positive; if the memory address is less than TSKBOT, the MA<TSKBOT line goes positive and INTASK1 at IC75-4 (1A6) goes to ground, indicating that the presented address is below TSKBOT. The IC70 gates (1A5) provide the following function at IC70-8:

ON (MA>=TSKBOT + (PSW23) (MA>=LIBBOT))

If this signal is positive and PSEL0 is ground, indicating a CPU memory cycle, the outputs of the selected memory IC's are passed through IC's 141 and 142 (1A1 and IC1) to become XMA140, XMA150, and MA000 through MA050, the most significant 8 bits of the 18-bit memory address. If the IC70-8 signal is ground and PSEL0 is ground, the FMA000 through FMA050 signals are passed through IC's 141 and 142; XMA140 and XMA150 are forced positive. IC130 (1A4) passes FMA060 and FMA070 through to MA060 and MA070 when FPSEL0 is ground. Thus, when PSEL0 is ground and the MMU is on, all CPU addresses at or above TSKBOT are always mapped, and all CPU addresses at or above LIBBOT are mapped when PSW23 (PSW7) is 1.

If all outputs of the selected memory IC's are positive, indicating that the memory byte is all zeros, IC93-8 (IC2) goes to ground and ERR1 goes positive, indicating a possible error; that is, the CPU is accessing a memory location which is mapped to the 0th 1K page. ERR1 also goes positive if INTASK1 is ground, indicating that the CPU memory address is below TSKBOT. These conditions are erroneous only if the CPU tries to write new data to memory.

If LDMAP1 is ground, IC108 (2C7) passes the SELCH memory address lines, SMA000 through SMA030 through to the SELCH map memory IC's (page 2 of the schematic). IC119 (2D7) decodes the SMA041 and SMA051 lines as follows (SMA040 and SMA050 actually appear at the IC):

SMA041	SMA051	OUTPUT	IC'S ENABLED
0	0	2Y3	105 114
0	1	2Y2	103 112
1	0	2Y1	104 113
1	1	2Y0	102 111

The selected memory IC's present their outputs to IC's 115 and 125 (2C1 and 2D1). If the MMU is ON and PSEL1 is ground, indicating that the SELCH is selected, the mapped address appears on the XMA140, XMA150, and MA000 through MA050 lines, which go to the core memory. If the MMU is not ON and PSEL1 is ground, the SELCH address lines SMA000 through SMA050 are passed through IC's 115 and 125 to become MA000 through MA050; XMA 140 and XMA150 are held positive. If PSEL1 is ground at IC130 (1A4), SMA060 and SMA070 are passed through to become MA060 and MA070.

Whenever a command is sent from the CPU to the MMU, CMG1B (2B8) goes positive; the one shot IC80-13 is triggered when CMG1B returns to ground. The output of the one shot changes the state of the flip-flop IC90 according to the states of COT040 and COT050, which represent bits 4 and 5 in the command byte sent to the MMU. When the output of the flip-flop, ON1, is positive, the MMU is on. SIN020 provides status bit 2.

Whenever the CPU attempts to write new data to memory with PSW bit 7 set to 1, PROTECT, the CPU generates the signal PRTECT0, unless it is a privileged write. On the trailing edge of PRTECT0, the one shot IC80-5 is triggered. If the MMU is ON and ERR1 is positive, IC92-8 goes positive, setting the flip-flop IC76-9 to indicate a memory protect violation, and generating CWR0, which inhibits the write operation in the CPU. The flip-flop IC76-8 provides SIN030 and SIN050, status bits 3 and 5, and SATN0, which causes the Universal Logic Interface to generate an interrupt, if enabled. IC76-9 is reset by the acknowledgement of the interrupt, RATN1B, by a new command addressed to the MMU, CMG1B, or by master clear, SCLR0.

WIRING CHANGES FOR THE MEMORY MAP UNIT

The following wiring changes apply only to the Model 7/16 with High Speed Arithmetic Logic Unit (HSALU). In the following wiring changes, back plane pin numbers are referenced in the format ABB-CCDD, where:

A = Row on connector, 1 or 2
BB = Pin number on connector, 00 through 41
CC = Connector number, 00 through 07
DD = Connector side, 00 or 01

The memory map unit plugs into slot 4 of the CPU chassis. Remove the following jumpers on the back plane:

Memory Map	Memory Map	Signal
221-0400	208-0400	MXR150 XMA150
222-0400	108-0400	MXR140 XMA140
228-0400	205-0400	MXR141 XMA141
121-0400	106-0400	MAR000 MA000
123-0400	109-0400	MAR020 MA020
127-0400	110-0400	MAR030 MA030
134-0400	210-0400	MAR040 MA040
107-0400	122-0400	MA010 MAR010
135-0400	129-0400	MAR050 MA050
136-0400	229-0400	MAR060 MA060
137-0400	130-0400	MAR070 MA070

Cut the following conductors between the slot containing the SELCH and the slot above the SELCH.

SELCH	Above SELCH	Signal
106-XX00	106-YY00	MA000
107-XX00	107-YY00	MA010
109-XX00	109-YY00	MA020
110-XX00	110-YY00	MA030
210-XX00	210-YY00	MA040
129-XX00	129-YY00	MA050
229-XX00	229-YY00	MA060
130-XX00	130-YY00	MA070

Here,

XX = Slot containing SELCH

YY = Slot one above SELCH

Cut the following conductor.

CPU-A	CPU-B	Signal
111-0700	111-0600	PSW271

Remove the following leads.

CPU-A -----	Ground Plane -----	Signal -----
111-0700	GND	PSW271
CPU-A -----	Memory 1 -----	Signal -----
122-0700	222-0301	ACK0 TACK0

On each slot where memory is to be plugged in, remove the wires on pins 108-ZZ00 and 208-ZZ00, XMA150 and XMA140 (MA01 and MA02). ZZ is any slot containing a memory board.

Add the following wires on the back plane.

SELCH -----	Memory Map -----	Signal -----
106-XX00	106-0401	SMA000
107-XX00	206-0401	SMA010
109-XX00	107-0401	SMA020
110-XX00	207-0401	SMA030
210-XX00	108-0401	SMA040
129-XX00	208-0401	SMA050
229-XX00	109-0401	SMA060
130-XX00	209-0401	SMA070

Again, XX is the slot containing the SELCH.

Add the following wires on the back plane.

Memory Map	Slot below Memory Map	Signal
119-0401	119-0301	SRO
120-0401	120-0301	DRO
123-0401	123-0301	SYNO
219-0401	219-0301	ADRSO
220-0401	220-0301	CMDO
221-0401	221-0301	DAO
223-0401	223-0301	ATNO
226-0401	226-0301	HWO
126-0401	126-0301	SCLRO
111-0401	111-0301	D000
211-0401	211-0301	D010
112-0401	112-0301	D020
212-0401	212-0301	D030
113-0401	113-0301	D040
213-0401	213-0301	D050
114-0401	114-0301	D060
214-0401	214-0301	D070
115-0401	115-0301	D080
215-0401	215-0301	D090
116-0401	116-0301	D100
216-0401	216-0301	D110
117-0401	117-0301	D120
217-0401	217-0301	D130
118-0401	118-0301	D140
218-0401	218-0301	D150
222-0401	122-0301	TACKO RACKO
108-0400	208-0300	XMA140
208-0400	108-0300	XMA150
CPU-A	Memory Map	Signal
122-0700	122-0401	ACKO RACKO
111-0700	210-0401	PSW271
CPU-B	Memory Map	Signal
137-0601	110-0401	PSW231
CPU-B	Ground plane	Signal
111-0600	GND	PSW271

Bus the 108-0300 and 208-0300 connections one-to-one through all slots containing memory (XMA150 and XMA140 or MA01 and MA02).

On the CPU-C board, 35-524, remove the following jumpers:

A2 to A3
 B2 to B3
 C2 to C3
 D2 to D3
 E2 to E3
 F2 to F3
 G2 to G3
 H2 to H3
 J1 to J2

On the CPU-C board, 35-524, add the following jumpers:

A1 to A3
 B1 to B3
 C1 to C3
 D1 to D3
 E1 to E3
 F1 to F3
 G1 to G3
 H1 to H3

On the SELCH board, 35-391, cut the conductor SEL1A so that IC's 103 and 125 are isolated from the source of SEL1A. Add a 1K resistor between +5V and the conductor connected to IC's 103 and 125. On 35-391M02R03, this change can easily be made in the vicinity of IC 103, pin 13. The address selection jumpers on all memory boards should be connected as they would be in an Interdata 7/32 computer. See the instruction manuals for the memories.

Connector 2 on the Memory Map board must have a mating connector, wired as follows:

Memory Map	CPU-A	Signal
108	111	CWRO
208	211	GND
109	107	PRTECTO
209	207	GND

Each pair of wires should be run as a twisted pair. These signals also go to the Memory Protect board; this board may remain in the system so that a standard RTOS software system will operate. If a Memory Protect board is not in the system, a 220 ohm - 330 ohm terminator should be added to the Memory Map board at PRTECTO.

PARTS LIST

QUANTITY	DESCRIPTION	PART NUMBER	STOCK NUMBER
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PRINTED CIRCUIT BOARD

1 ea	Interdata Universal Logic Interface	M48-013	Not Stock
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INTEGRATED CIRCUITS

1 ea	Quad 2-input NAND gate	SN7400N	5961-53218
1 ea	Quad 2-input NOR gate	SN7402N	5961-53220
4 ea	Hex inverter	SN7404N	5961-57216
3 ea	Quad 2-input AND gate	SN7408N	5961-57564
1 ea	Triple 3-input NAND gate	SN7410N	5961-53221
1 ea	Triple 3-input AND gate	SN74H11N	Not stock
2 ea	8-input NAND gate	SN7430N	5961-53223
1 ea	Quad 2-input NAND buffer, open coll.	SN7438N	5961-58467
1 ea	Gated J-K edge triggered flip-flop	SN7470N	5961-53228
2 ea	Quad D latch	SN7475N	5961-53238
1 ea	Dual D flip-flop, buffered output	SN7479N	5961-58004
4 ea	4-bit magnitude comparators	SN7485N	Not stock
24 ea	64-bit read/write memory	SN7489N	Not stock
2 ea	Dual monostable multivibrator	SN74123N	5961-59093
3 ea	Dual 2-line-to-4-line decoders	SN74155N	Not stock
8 ea	Quad 2-input multiplexer, tri-state	DM8123N	5961-62193

RESISTORS

3 ea	1K, 1/4W, composition 5%		5905-49070
2 ea	6.8K, 1/4W, composition 5%		5905-49083
1 ea	20K, 1/4W, composition 5%		5905-49091
3 ea	Package of 15, 470 ohm, 1/4W	Beckman 899-1-R407	5905-90971

INTEGRATED CIRCUIT SOCKETS

16 ea	14 pin sockets	TI C7519	5975-56092
46 ea	16 pin sockets	TI C7520	5975-56093

APPENDIX A: SCHEMATIC DIAGRAM OF THE MEMORY MAP BOARD

Fig. A1. Schematic diagram of the memory map board.

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126-150	6.00	451-475	12.00
151-175	6.75	476-500	12.50
176-200	7.50	501-525	12.75
201-225	7.75	526-550	13.00
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