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AUTOMATED ARRAY ASSEMBLY

Quarterly Report No. 3, July 1, 1976—September 30, 1976

B. F. Williams

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**RCA Laboratories
Princeton, New Jersey**

MASTER

**ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
Division of Solar Energy**

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QUARTERLY REPORT NO. 3

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PREFACE

This Quarterly Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes work performed during July through September 1976 in the Communications Research Laboratory, K. H. Powers, Director; Process and Applied Materials Research Laboratory, P. Rappaport, Director; Materials Research Laboratory, J. J. Tietjen, Director; and at the Advanced Technology Laboratory, Government and Commercial Systems, Camden, NJ, P. Wright, Director. The Program Manager is B. F. Williams. Others who participated in the research and writing of this report are: J. Toner, D. Richman, H. Kressel, G. Schnable, W. Kern, R. D'Aiello, D. Redfield, B. Schelpuk, and F. Mayer.

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SECTION I

SUMMARY

A review of the quality of the various possible forms of the starting silicon material leads to the conclusion that wafers from Czochralski-pulled ingots are the only form of silicon which will be available for automated array processing for the next several years.

A new calculational procedure has been developed and tested for the optimization of performance of both the front and back contact metallizations. For the front contact, all four principal sources of loss are included; appropriate constraints are imposed, arising from both general principles of contact design and the physical limitations of specific technologies; the optimum grid line spacing is found; and the total power output is evaluated. The chief technical uncertainty is found to be the metal-Si contact resistivity ρ_c , and a general criterion can be stated that ρ_c must be $\lesssim 10^{-2}$ ohm-cm². If this condition is met, a number of cost-effective options for both front and back contacts appear to offer satisfactory performance.

The survey of present-day contact and interconnect metallization technology for silicon devices has been completed. The evaluation of the various processes has been treated from the viewpoints of technical applicability to silicon solar cells, manufacturing feasibility on a large scale (10^6 to 10^8 cells per year), production cost, and device reliability. Detailed cost analyses of selected processes have been conducted using computer techniques. From a quite thorough analysis, screen-printed Ag contacts appear the most cost effective.

A semi-automated parallel gap welding procedure is defined in detail, and a further analysis of panel material costs is presented. Glass panels of three configurations are considered the best choice and these are described.

A complete description of the cost analysis procedure for one particular solar array module manufacturing sequence is given. This sequence, using gas diffusion junction formation technology, screen-printed Ag contacts, spin-on AR coating, gap welding for interconnects, and a glass plate-conformal coating-metal foil moisture barrier panel, produces panels at a cost of \$0.9/W.

The basic materials costs of the process sequences developed and studied are beginning to approach interesting values. The lowest cost projected to date for material and expense items for array module manufacturing is \$0.30/W.

SECTION II

INTRODUCTION

We have completed the first phase of our program. A summary of the analysis of the existing technologies which could be applicable to solar array module manufacturing is given in this report. A more speculative study, upgrading and refining existing technologies, is underway. In this area, technologies such as vapor epitaxy and ion implantation, which at present do not provide reasonable processing alternatives, are being reevaluated using new conceptual equipment designs. The importance of high conversion efficiency is difficult to overstate. The basic material expense costs have been brought to the \$0.30 to \$0.40/W range for 11% efficient cells, 9% efficient panel. Further significant cost reductions are becoming increasingly difficult to realize. The impact of increased conversion efficiency is obvious.

In this report, we give an example of a complete manufacturing sequence with all the supporting documentation. With this documentation, the interested reader will be able to determine exactly where all of the costs for each of the processes in this particular sequence come from. Such a collection of documents is produced on demand when any sequence is selected from the list of evaluated processes included in this report. A comparison of the resulting final panel costs is the basis for selecting the most desirable process step. The implementation of our software for this analysis has greatly facilitated this comparison.

SECTION III

TECHNICAL DISCUSSION

A. STARTING MATERIALS

It is becoming increasingly evident that of the many possible forms of starting Si sheet, wafers cut from Czochralski-pulled ingots will be the primary source of material for automated array processing studies for at least the next 3 to 5 years. This material can be prepared with the quality necessary to produce 15% efficient cells and in the quantity necessary to establish the mass production concepts inherent in automated array processing. The only other Si of comparable quality prepared in large quantities is epitaxial Si on single crystal Si substrates, and with existing CVD reactors, this is not a cost effective approach.

While progress is being made in other areas of sheet growth, there appear to be significant problems which must be overcome before a commercially viable process is developed. Next in quality behind pulled crystal and single crystal homoepitaxy is the dendritic web crystal. However, it is yet to be shown that web can be controllably pulled in widths greater than 1 in. at rates which will make the area production cost competitive with pulled crystal. Also, the dog-bone type of ribbon cross-section produced by this technique may present special problems in handling this material.

Ribbon pulled from a wetted die is also available in sufficient quantity to begin to assess its quality. For this type of growth, considerable work must still be done to pull low strain ribbons of 2- to 3-in. widths at speeds which will be comparable to Czochralski area yields. Perhaps more serious is the presence of random defects which degrade the quality of the Si or solar cells which contain the defect. Until these defects can be reduced to the point where defect-free cell yields of the order of 95% are obtained, this material will not be suitable for automated array processing. Also, due to dissolution of some die material, a gettering step is necessary to make 10% efficient cells from ribbon material. Other techniques of ribbon formation have not progressed far enough to assess the quality of the material produced.

Another class of material is that which includes the various forms of Si deposited on substrates of a material other than Si. The most advanced method

here is the epitaxial growth of Si on sapphire from the gas phase. This method yields a Si layer whose crystal structure near the sapphire is so disordered that it is unlikely that high quality solar cells can be made unless this region of the silicon layer is removed from the active region of the cell. Also, the present cost of epitaxy and substrates makes this process not cost effective. All of the other deposition techniques, whether gaseous or liquid based, yield polycrystalline silicon. Before any of these materials may be considered, it will be necessary to learn how to control the grain boundaries. While there has been a slow improvement in the efficiencies reported for polycrystalline Si solar cells in the recent past, values greater than 7% have not been achieved.

Considerations such as these lead to the conclusion that wafers from pulled ingots must be considered as the starting Si material for the near term and possibly longer.

B. SOLAR CELL PERFORMANCE PREDICTION

To evaluate the impact of cell processing variations on the cell performance, it would be desirable to be able to calculate the ways in which the principal electrical parameters of cell (J_{sc} , V_{oc} , and F) change with processing changes. It was decided not to attempt an all-encompassing single calculation of the type used by Wichner et al. [1] or by Dunbar and Hauser [2] because of the complexity of those calculations and the difficulty in matching them to individual processing step variations. Instead, an approach has been developed which evaluates, to the maximum extent possible, separate effects on the three electrical parameters. To date, analysis has been performed on J_{sc} because it is the most sensitive of the three and is most amenable to quantitative assessment. This analysis is now fairly well established, and the corresponding efforts for V_{oc} and F are beginning.

1. R. Wichner et al., "Design Optimization of Beta- and Photovoltaic Conversion Devices," Lawrence Livermore Lab. Report VCRL-51993, Jan. 8, 1976 for ERDA Contract No. W-7405-Eng-48.
2. P. M. Dunbar and J. R. Hauser, "A Study of Efficiency in Low Resistivity Si Solar Cells," Sol. St. Electron. 19, 95 (1976).

Techniques for computing the current collection efficiency are fairly well known. They have been extended to permit inclusion of a "dead layer" at the front surface in the calculation of the quantum efficiency as a function of wavelength $Q(\lambda)$ at values of λ separated by $0.02 \mu\text{m}$. Also, the calculations are made with air mass (AM) 0, 1, 2 (using Thekaekara's irradiance values [3]) so that the efficiencies at different air mass numbers can be compared. The total J_{sc} is given by

$$J_{sc} = \sum_{\lambda = 0.2}^{1.12} Q(\lambda) N_p(\lambda) \quad (1)$$

where $N_p(\lambda)$ is the solar irradiance in number of photons/cm² s μm . The collection efficiency of a cell is just

$$\eta = \frac{J_{sc}}{\sum N_p(\lambda)} \quad (2)$$

The often-necessary photon flux spectrum $N_p(\lambda)$ seems not to have been published, so it is presented in Fig. 1 for AM 0, 1, 2 as a general reference.

There are seven parameters describing the properties of the cell: in the back (the bulk of the cell) are the thickness T_B , diffusion length L_B , and back surface recombination velocity $BSRV$; in the front are the thickness (i.e., junction depth) T_F , diffusion length L_F , front surface recombination velocity $FSRV$, and dead layer thickness DE . No reflection loss is introduced computationally. Of these seven, only three or four are well known: the back ($\approx$ cell) thickness, diffusion length, and recombination velocity (in some cases), and the front thickness. The other values are adjusted to fit measured curves of $Q(\lambda)$.

After developing the necessary familiarity with the physically significant ranges of the parameters it has become possible to make very good fits

3. M. P. Thekaekara, in *Proc. Symp. on Solar Energy Utilization* (NASA Goddard Space Flight Center, Greenbelt, Md., 1974), p. 21.

Figure 1. Solar irradiance expressed in terms of photon flux.

to measured data on $Q(\lambda)$ for experimental cells being made to test processing variations. Figure 2 shows a set of data points for one such cell and the calculated curve of $Q(\lambda)$ using the values of parameters shown. This cell, which has a texturized front that is coated with Ta_2O_5 , can be seen to have an almost negligible reflection loss over most of the spectrum. The adjusted values of the unmeasurable front parameters can be inferred because (a) dead layers are found to cause a somewhat different blue response and (b) unphysically high values of FSRV would be required to cause the fall-off in $Q(\lambda)$ at $0.4 \mu m$. Thus, it appears possible to model well cells of reasonably good quality. [These calculations appear to cast doubt on the measurement of $Q(1.1 \mu m)$.]

The importance of the AR coating in addition to the texturizing can be seen in Fig. 3. The AR coating provides an additional 10% in quantum efficiency.

These calculations are now being used for evaluation of options being considered for anti-reflection treatment of the front surface. Other results of these calculations show that most expected cell structures give results insensitive to the value of FSRV provided it is in its normal range ($\sim 10^5$ cm/s).

Figure 2. Spectral dependence of the quantum efficiency of current collection. Points are measured values for a cell whose front surface has Ta_2O_5 over texturizing. Line is computed response using the parameters shown and no dead layer at the front.

Figure 3. Measured (points) and calculated (lines) $Q(\lambda)$ for non-AR coated textured cell.

This offers significant freedom in the choice of AR treatments. We also can readily determine the conditions under which a back-surface field can make a significant improvement to J_{sc} and the quantitative effects of lifetime variations in the bulk.

The remaining need in this area is to determine quantitative links between all of the processing options to be studied and the parameter of the calculation. This is requiring experimentation as options are introduced. The analysis of performance of various contact metallization processes that was begun in the previous quarter has been extended to permit a performance evaluation of any metallization option for which a full description is available. A calculational procedure has been developed that now optimizes all four of the significant parameters listed below:

- (1) Current loss due to shadowing.
- (2) Voltage drop due to sheet resistance of the front Si layer.
- (3) Voltage drop due to contact resistance at the metal-Si interface.
- (4) Voltage drop due to resistance of the metal grid itself.

The new procedure provides the important addition of the metal-Si contact resistivity to the procedure. The accomplishment of this optimization in a straightforward manner results from the imposition *a priori* of constraints that represent the known physical limitations of the metallization options and the invoking of the theorem that grid line width be as small as experimentally possible. By simple variations of the analysis developed for the front contact we have also shown that the metallization used on the back can be greatly reduced without serious performance loss. The consequences of this for cost analysis are found to be very favorable. The procedure is described below.

With the requirement that all individual losses be small (i.e., reduce the power by less than 10%), the power delivered by a cell whose front contact is being analyzed is

$$P \approx I_m \left[V_m (1 - S) - J_m \left(\rho_s \frac{d^2}{8} + \rho_c \frac{d}{w} + \rho_g \frac{L^2}{2} \frac{d}{w} \right) \right] \quad (3)$$

where the subscript m denotes the maximum power values; ρ_s is the sheet resistance (ohm/sq) of the Si front layer; ρ_c is the metal-Si specific contact resistance (ohm-cm²); the grid lines have width w, length L, spacing d, and sheet resistance ρ_g (i.e., bulk resistivity/thickness); and the fractional area shadowed is $S = w/d$. Next, we find the fractional power delivered

$$f = \frac{P}{I_m V_m} = 1 - S - (J_m / V_m) B \quad (4)$$

where B is the second term in parentheses in Eq. (3) representing the voltage drops.

By the previously stated theorem, the grid line width must be as small as possible, so w is fixed by the minimum value of the technology of the process being evaluated; ρ_g is also fixed by the technology. Thus, for

example, screen-printed Ag has been characterized by a minimum line width of 125 μm , thickness 12 μm , and bulk resistivity 3.2×10^{-6} ohm-cm (twice that of Ag metal) so that $\rho_g = 3.2 \times 10^{-6} / 12 \times 10^{-4} = 2.7 \times 10^{-3}$ ohm/sq. Further, the physical properties of a fairly good Si solar cell are represented by the values $J_m = 0.028$ A/cm², $V_m = 0.45$ V, and $\rho_s = 50$ -100 ohm/sq; these are also fixed in the calculation, although they are changed for different cells.

The grid line length L is chosen arbitrarily to fix a basic pattern size; a commonly used value has been $L = 2$ cm with a contact strip at one end or 4 cm with double-sided contacts. In this fashion, the optimization reaches the stage of needing only the contact resistivity ρ_c and the line spacing d . In practice, we maximize the output power by differentiating Eq. (4) with respect to d while treating ρ_c as a parameter. This differentiation leads to a cubic equation in d whose root is found by a subroutine. Having thus optimized the grid line spacing for a particular set of physical parameters, Eq. (4) itself is evaluated for the power as a fraction of ρ_m , that available in the absence of any of these four losses. It must be emphasized that the power calculated is independent of the junction quality or any other factors (once J_m and V_m are known); it shows only the performance of the front contact.

This computation is simple enough to be repeated for a wide range of values of ρ_c , which is the least-known physical property of most metallization processes. Thus, curves like those in Fig. 4 are generated to permit the direct observation of the effects of different values of ρ_c . These calculations have provided several useful results. In Fig. 4, 100% power fraction corresponds to the case of no loss from any of the four factors. For thick Ag and low contact resistance, the remaining losses are the shadowing and Si sheet resistance. As can be seen in Figure 4, which models cells with the usual evaporated Ag, the 4- μm thickness normally used is wasteful of Ag since only 1 μm can be used with an additional loss of only 2% of the power, while 0.4 μm causes a 6% power reduction. Applying this analysis to several other types of front contacts shows that it is possible to generalize the requirement (that can be inferred from Fig. 4) that the contact resistivity of any front metallization will be acceptable if, and only if, its $\rho_c \lesssim 10^{-2}$ ohm-cm². This should become one criterion for future choices.

This approach lends itself also to analysis of the *back* contact that normally uses unnecessarily large amounts of Ag. It can be shown that

Figure 4. Output power as a fraction of that generated by a lossless cell vs ρ_c .

screen-printed Ag could be used on the back in a pattern having only 10% area coverage and 5-μm thickness (a projected reduction from the present 12 μm) while losing only ~1% of the power. Such a back contact drastically alters the cost picture for silver contacts.

C. METALLIZATION TECHNOLOGY

The following subjects have been treated from a standpoint of manufacturing feasibility and production cost and complete the survey of present-day metallization technology:

- (1) Vacuum evaporation
- (2) Magnetron sputtering
- (3) Screen printing
- (4) Electroless plating
- (5) Transfer tapes
- (6) Transparent conductors
- (7) Schottky barriers
- (8) CVD and MOD (Metallo-organic depositions)

1. Electron-Beam Vacuum Evaporation

The only well-established production process for successfully preparing contact and interconnect patterns on Si solar cells is vacuum deposition of bilayer Ti-Ag (or Ti-Pd-Ag) or of single layer Al, as described in Quarterly Report No. 2 [4]. We indicated that 33% of the cost of this process is due to Ag for 5% front and 100% backside patterned deposition through a mask, if a film thickness of 4 μm is used. The computations based on output power efficiency as a function of metallization pattern geometry described above have now shown that a factor of 4 reduction in film thickness results in an acceptable loss of only 2% in power output. Thus, a cost reduction for Ag by a factor of at least 4 can be realized. Additional reduction by a factor of about 3 can be obtained by metallizing only 33% of the cell backside area by use of a mask stencil to produce a grid pattern of optimal geometry. However, despite these reductions, the cost of this process is still very high because of the capital equipment cost. Substituting Al for Ti-Ag would, for the same reason, not substantially lower the cost and would necessitate ultrasonic bonding or welding because of its lack of solderability.

2. Magnetron Sputtering

Continuous in-line magnetron sputter deposition of Ti-Ag or of Al metallization patterns was expected to offer interesting cost aspects because of its capability of continuous and automated operation. A detailed cost analysis was therefore undertaken on the same basis as reported previously for electron-beam vacuum evaporation (0.2 μm Ti + 4 μm Ag, or 4 μm Al, 5% coverage front side, 100% on backside, 1.25×10^6 cells/year) to allow direct comparison. The results of the cost analysis revealed that magnetron sputtering of Ti-Ag is only 10% cheaper than the electron-beam evaporation process. For Al, the sputtering process is about 36% more expensive than evaporation because of lower deposition rate which lowers the throughput capacity, thus increasing the capital cost.

4. B. F. Williams, "Automated Array Assembly," Quarterly Report No. 1, ERDA/JPL-954352-76/1, prepared under Contract No. 954352 for Jet Propulsion Laboratory, March 1976.

3. Screen Printing

Automated screen printing of Ag paste comes close to an established process for solar cell applications. The main problems are to formulate optimal sintering conditions that minimize the specific contact resistance to Si to $\sim 10^{-2}$ ohm-cm² and to control depth of penetration.

Substantial cost savings over the estimates previously made are possible by reducing the film thickness and contact area to the minimum compatible with required sheet conductance and printing technology. Reducing the contact area on the back requires a diffused contact on the backside. Latest estimates have shown that by introducing changes in paste formulation, we could reduce the thickness from 12.5 μ m to 5 μ m and the backside contact area from 100% to about one-third. The cost of the Ag paste could be reduced substantially for quantities of 500,000 troy ounces per year needed for producing 10⁸ cells. The formulation and non-metal cost reduces to about one-third of that for 5000 troy ounces. At the present market price of Ag (\$4.15/troy ounce) and at an 80% Ag content of the paste, the paste cost would be \$5.22/troy ounce instead of the price of \$10.00 quoted in our Quarterly Report No. 2 (for ink for 10⁶ cells/year).

Since 90% of the total printing process cost is due to materials cost (if based on 5% front and 100% backside coverage, 12.5 μ m thick), very substantial savings can be achieved by the modified large-scale screen printing process scheme yielding highly conductive and solderable metallization patterns. In Fig. 13 (subsection G below) we show the summary statement for array fabrication using the metallization described above. This process uses parallel-gap welding in the array fabrication rather than the more expensive solder reflow. The array costs are about \$0.9/W, of which only \$0.117/W is due to metallization. This represents a cost reduction in metallization of about 86% for this modified process.

At the outset it was felt that the cost of screen-printed metallization could be reduced substantially by substituting Al for Ag in the printing paste (\$1.90/troy ounce for any base metal vs \$5.22/troy ounce for Ag-based paste). However, due to the lower conductivity of Al, films about twice as thick may be required. The cost difference does not seem to warrant an enthusiastic pursuit of this process due to other difficulties. As

pointed out previously, a considerable development effort would be required to optimize the paste formulation and the process parameters. The lack of solderability of Al could be overcome by screen printing a Ag pad over the Al pattern before firing. The two deposits could then be fired simultaneously to facilitate penetration of the Ag into the Al layer, and to save a processing step. A cost estimate has been computerized based on Ag front side (5% of area) screen printing and firing, followed by Al backside (100% of area) screen printing and drying, and finally depositing by screen printing a solderable Ag pad (1% of area) over the Al-coated backside. The cost is \$0.158/W (see Fig. 11, line 47). The equivalent coverage in the Ag-only case is \$0.135/W. At one-third back coverage, the Ag-only process is slightly more attractive: \$0.06/W vs \$0.087/W, for the Al + Ag process.

The use of solderable base metals, such as Ni or Cu, instead of Ag or Al in the paste formulations is a further alternative we have considered. Similar to the Al-based materials, the apparent initial cost advantages of these are outweighed at present by conductivity differences and a host of technical problems that must first be solved, including formation of good ohmic contacts, sufficiently low specific contact resistance, optimum paste formulation, excessive penetration into the Si substrate, and contamination by impurities and metals (especially Cu).

4. Electroless Nickel Plating

The process of deposition of electroless Ni on presensitized Si surfaces followed by sintering and solder coating is widely used in the fabrication of Si power devices with deep p-n junctions. Good ohmic contacts are formed on both n^+ and p^+ diffused Si. However, to achieve high sheet conductance, good adhesion, and sufficient solderability, a minimum of a second Ni plating is required after sintering. Furthermore, the high-temperature sintering treatment required is difficult to control reliably without penetrating the shallow n-p junction used in solar cell structures. The Ni films formed by electroless plating on Si are generally too thin for conduction lines on solar cells, unless they are thickened by additional electroless or electroplating steps, or by application of a solder coating. An additional negative feature of electroless plating processes is their extreme sensitivity toward

surface contaminants, which is a major cause of frequently encountered plating problems.

Deposition of a single Ni layer on both sides of the cell would require patterning of the front side prior to sintering by either photolithography or by screen printing on organic masking material, followed by chemical etching of the exposed metal and removal of the masking layer. These patterning steps would add significantly to the cost of metallization. An additional layer of Ni could be deposited by selective electroless plating on the pattern. The electroless Ni pattern can be built up by electroplating or by Sn-Pb solder deposition, an expensive process due to high breakage and clean-up operations.

A more attractive possibility is electroless plating of both cell sides followed by screen print masking of 95% of the front side area. The Ni film on both sides of the cell can then be electroplated to any desired thickness. The mask is stripped and the cell briefly immersed in Ni etchant to remove the thin film of the original electroless Ni, while the electroplated metal acts as an etch mask.

Electroless deposition of Ni on the cell backside only would entirely eliminate the need for pattern, but requires adequate protection by masking of the cell front side.

Selective electroless plating of Ni on sensitized and activated areas of the cell constitutes an alternative technique of Ni deposition without subsequent patterning.

The process sequences discussed are all practically feasible in a largely automated operation. However, because of the multiplicity of steps, these processes are not attractive compared with direct screening of contacts. A preliminary analysis yields about \$0.30/W per surface. A detailed report of advanced procedures will appear in the final analysis.

5. Other Metallization Processes

Several other potentially low-cost processes on materials for creating the required metallization patterns on solar cells on a mass production scale have been examined. These include transfer tape techniques, transparent conductors, Schottky barriers, and CVD and MOD films. We consider none of these alternatives economically and/or technically viable at present, for the reasons stated below.

Metallizing transfer tapes consist of a layer of metallic composition of exact thickness temporarily attached to a plastic carrier film. The layer is transferred mechanically by the application of pressure to a substrate where it is fired like screened-on conductor pastes. The application of preshaped metallization patterns of simple geometry is a possibility but would require substrate alignment. However, this technique offers no advantages for our application over the less expensive and direct screen-printing process of conductor patterns.

The application of transparent, electrically conductive thin films as primary metallization could offer interesting possibilities because they could serve as both metallization and anti-reflection coating. However, because the conductivities are low, the principle problem with this approach is that these layers cannot take the place of the first level metallization. A sheet resistivity of $\sim 10^{-2}$ ohm/sq is required. These layers are in the 10- to 100-ohm/sq range. Their only usefulness is then the AR function for which there are simpler techniques.

Such layers can be used, however, not as a metallization substitute but to provide the sheet conductivity normally associated with the heavily doped front layer of the p-n junction itself. The potential for improved performance is under quantitative evaluation. The serious questions of contact resistance will be evaluated experimentally if the theoretical performance warrants.

The possibility of using a semitransparent metal-semiconductor Schottky-barrier contact as primary metallization on single crystal cells was briefly considered. A contact of this type might offer several economical and technical advantages, such as elimination of the need for diffusion to create p-n junctions, and therefore increased cell efficiencies, and reduction of the light absorption losses occurring with other nontransparent contacts used in conventional Si p-n junction solar cells. Fabrication of a Schottky barrier includes a very careful preparation of the polished Si surface and the vacuum deposition by electron-beam evaporation of very thin metal films. For example, thin layers of Pt or of the bimetallic combinations Cr-Au and Cr-Cu have been used in developmental-type devices. In the second case, the chromium forms the Schottky barrier and serves to provide good adhesion to the Si. The thin over-layer of Au or Cu provides electrical conductivity, consistent, of course, with thickness limitations because excessively thick metal layers would absorb

too much light. The metal layer thicknesses are in the range of tens of angstroms and must be precisely controlled. It appears that this could be possible with continuous automated processing. However, processing on a mass production scale under the control necessary to produce these extremely thin films constitutes a difficult step. The major disadvantage of this approach is the extreme sensitivity of Schottky-barrier devices to processing parameters, especially those that relate to the semiconductor surface, which can profoundly affect the electrical performance of the device. There is, however, no point in the use of thin metal films as a primary metallization because the absorption is too high for sheet resistivity in the 10^{-2} ohm/sq range.

The use of a Schottky barrier on single crystal material as a junction formation technique is still under evaluation, and specific cost information for advanced conceptual processes will be given.

Chemical vapor deposition (CVD) of metal films for conductor applications has the principal advantage of requiring much less complex and expensive deposition equipment than physical vapor deposition. Its main disadvantage is the need for a separate patterning process subsequent to film deposition since the process precludes the use of single stencil masks. The most promising method would be pyrolytic decomposition of tri-isobutyl aluminum vapor at 300° to 350°C for producing Al films; this is a large-scale process used for metallizing plastics but has not been investigated for semiconductor device applications as yet. The same is true for low-temperature pyrolysis of highly toxic nickel carbonyl to form films of Ni, or of metal acetyl acetonates for depositing films of Cu, Co, and other metals. A CVD hydrogen-reduction process we have developed for deposition of tungsten or molybdenum films from the fluorides has yielded excellent results for metallizing silicon devices to create highly temperature- and corrosion-resistant structures. However, a secondary metal deposition is needed to achieve solderability or bondability. None of the CVD techniques can be considered viable on a cost basis for the present application.

Metallo-organic deposition (MOD) of metal films is based on depositing a pattern by screen printing or other simple techniques using metallo-organic compounds in homogeneous single phase formulations. Drying and thermal decomposition of the organic components leaves a thin, well-adherent metal film.

Both noble metals and base metals can be deposited. However, the films deposited in a typical single application are only 2000 Å thick; multiple applications with appropriate wafer alignment would be needed to create films of required thickness to provide sufficient current-carrying capacity. There is no advantage of these materials compared with direct application of the screen-printed contacts discussed above.

D. JUNCTION FORMATION STUDIES

1. Materials-Related Choices

Although it is customary to make solar cells on (100) p-type material, it is not clear from experimental work whether (111) crystal will give substantially inferior cells. While surface passivation may well be more readily achieved on (100), the (111) has a superior resistance to cleaving during processing. Thus, it is possible that the slight fall-off in efficiency can be more than compensated for by the higher yield, or thinner Si can be used at a correspondent reduction in cost. (111) wafers 12 to 14 and 14 to 15 mils thick have been received and will be used in experimental work to evaluate these points.

2. Evaluation of Unit Processing Costs

a. Diffusion

Cost estimates of various processes continue to favor POCl_3 as the cheapest source. A solid source diffusion process looked very inexpensive on paper: it consists of using very highly doped Si wafers as diffusion sources and stacking them in the order p+ solar cell, n+ solar cell, p+, etc, in coin fashion. Experimental work indicated that the process was very sensitive to the formation of oxide or nitride films on the target wafer, so much so that even if the high doping level we need can be achieved, the apparatus and precautions necessary to ensure high yield would make it prohibitively expensive.

b. Junction Etching

In the array fabrication process described in this report, the wafers are coin-stacked and submerged into an etch bath. The etch is designed to remove

first the oxide that is usually present on the surface and then to etch the silicon so as to remove the relatively thin undesirable diffused edge. There is always danger that acid will penetrate onto the center of the stack through cracks. This will be extremely sensitive to surface texture and will reduce yields. Alternative methods are under investigation.

c. Ion Implantation

Present equipment used for ion implantation is quite capable of producing the high dose rate required, about $4 \times 10^{15}/\text{cm}^2$, rapidly enough so that the rate of feeding wafers through the machine becomes the limiting factor. Extrapolation to 1980 requires little or no further development in beam current or source capability. Some consideration will have to be given to dissipating heat when deposition is made at higher dose rates but this does not appear to pose a major problem. The present installed capacities are about 220 implanted wafers per hour.

There are two methods of increasing throughput. The first consists of a cassette holding 1200 to 2000 wafers in a vacuum lock chamber. This is used to feed a belt moving wafers through the beam and deposits them in another cassette. Cassettes are changed via a vacuum lock. No snags in design are apparent.

The other method consists of continuously pumping the narrow space over a moving belt track with a series of pumps. Large enough vacuum pumps are available for this type of work. The ultimate vacuum to be achieved is about mid- 10^{-6} torr.

The major advantage of the ion-implantation method is that virtually no wet processing is needed. The process sequence consists of sequentially implanting a thin n^+ layer on one side and a p^+ contact on the other side in such a way that the edges are covered. The wafers are then coin-stacked automatically and heated in a nonoxidizing ambient to drive in the diffusion to form the shallow junction and the back contact simultaneously. It is expected that the ion impact damage can be annealed out at the same time. Calculations of dose requirements and redistribution have been made for beams of various energy from 5 to 40 keV of arsenic, boron, and phosphorus.

The implantation time for 10^{15} ions/ cm^2 is 10 seconds at 750-uA beam current. This time is compatible with the present vacuum lock time requirements.

Experimental work to determine whether the solar cells with an efficiency of over 10% can be obtained is underway.

The effect of eliminating the etch steps associated with gas diffused junction formation is interesting. Figures 13 and 32 (subsection G below) are cost summaries for two processes identical except in junction formation. The ion implantation step plus diffusion saves \$0.12/W in the overall cost even though it is more expensive in junction formation itself. The importance of demonstrating high performance with ion-implanted cells is clear.

3. Vapor Epitaxy

Because of the potential for upgrading the quality of some forms of low grade, single crystal substrate material, vapor epitaxy has been reevaluated. As shown in Fig. 11 (subsection G below) reduction of about a factor of 4 over our original estimate in the first quarterly progress report [5] is now being projected for near term developments. However, at \$0.41/W, the costs are still too high to be considered a useful process. A conceptual design for further cost reduction is underway.

E. SOLAR CELL INTERCONNECTION

There are several methods which can be used to interconnect Si solar cells. Six of these will be discussed in this report, three as baseline methods and three as second priority methods. The three baseline methods are parallel gap welding, reflow soldering, and ultrasonic welding. By far the most widely used method, to date, is reflow soldering. Practically all of the solar cell power supplies in space today were assembled using this technique. The other method used was the parallel gap technique. Ultrasonic welding is still an experimental method in terms of its application to interconnecting solar cells.

1. Parallel Gap Welding

The development of parallel gap welding to interconnect solar cells has been underway for several years. The bulk of the effort has been directed to

5. B. F. Williams, "Automated Array Assembly," Quarterly Report No. 2, ERDA/JPL-954352-76/2, prepared under Contract No. 954352 for Jet Propulsion Laboratory, June 1976.

space applications where the environment could get very warm and compromise the mission due to failure of interconnections in the power supply or where high temperature processing is required after interconnection is complete. Most of the work reported has been done using the Hughes MCW-550 constant voltage power supply and the Hughes Model VTA-66 weld head.

The operating principles of parallel gap welding are illustrated in Fig. 5. Two electrodes each of which is $380 \times 640 \mu\text{m}$ in cross section are brought

Figure 5. Parallel gap welding operation.

into contact with the work piece. Electrical current is drawn through the interconnector and the solar cell metallization both of which are brought to a molten or plastic condition by joule heating. The two metals are then made to flow or fuse together by the forging action of the electrode. The welding schedule required to achieve good bonds between interconnect and metallization requires definition of electrode voltage, pressure, spacing, and welding time. Other important parameters are the materials used, their thickness and surface condition. The important interconnection property which must be maximized by proper choice of welding design parameters in interconnect pull strength. Table 1 shows a preferred parallel gap welded interconnect design which has been described in the literature [6,7].

6. R. V. Elms, Jr., "Solar Array Welding Development," Conference Record of the 10th IEEE Photovoltaic Specialists Conference, November 1973.
7. Hans G. Mesch, "Parallel Gap Welding of Silver Plated Solar Cells," Conference Record of the 10th IEEE Photovoltaic Specialists Conference, November 1973.

TABLE 1. OPTIMUM PARALLEL GAP WELD DESIGN PARAMETERS

Interconnect Material	.001 Kovar
Interconnect Plating	.0002 Silver
Cell Metallization	.00025 Silver
Cell Roughness	250 nm RMS
Electrode Spacing	.010 in.
Electrode Loading	.1-3 lb
Welding Voltage	0.65 V
Weld Time	140 ms
Pull Strength	1.5-6 lb

Typically, the resistance that the welder will see is in the 2 to 3 milliohm range so that the current draw will be around 200 to 300 A. The energy delivered to the weld area will be approximately 25 joules/weld. Existing equipment is capable of delivering about 30 welds/minute at this power although for short bursts (3 to 4 minutes) it could deliver 60 to 100 welds/minute. When one considers the requirement for indexing between welds, the 30 welds/minute seems like a good value.

A typical interconnect design used by AEG-Teflefunken [8] calls for 6 welds/cell (3 on front and 3 on the back). The parallel welds are required to provide redundancy, as well as to reduce series resistance. It is safe to assume that for a large cell (e.g., 3-in. diameter) at least 6 welds will be required, thus making the throughput of the welder 5 cells/minute or 300 cells/hour. A factor which will slow down the throughput of a parallel gap welder is the requirement for dressing the electrodes periodically (after 8 to 12 welds). The Telefunken factory completes all operations under numerical tape control. Assuming that this operation takes 3 seconds after every 9 welds (1-1/2 cells) makes the welding time per cell 13-1/2 seconds for a throughput of 267 cells/hour.

There does not appear to be much information on electrical degradation of the cells as correlated with pull characteristics of the weld joints. It is clear that excessive welding energy or electrode pressure can cause divoting of the silicon under the bond area. It is not clear that microdamage does not exist under good welds. If shallow junction (0.1 to 0.2 μm) cells are used,

8. R. Ruhs et al., "Welding of Solar Cells in Production Line," Conference Record of the 11th IEEE Photovoltaic Specialists Conference, March 1975.

this technique must be carefully examined to determine if it can provide interconnection with high yield, adequate pull strength, and with acceptable tolerances on welding and cell parameters. A specific array fabrication technique using gap welding is described in subsection 7 below.

2. Reflow Soldering

By far the most widely used cell interconnection technique used today is solder reflow. The assembly methodology varies from company to company. In some cases, the cells are hot-tinned; others use plating. Usually flux is required to remove oxides although reflow can be done in a reducing or inert atmosphere. Heating means include furnace, IR lamp, gas stream, heated platens, or resistance heating electrodes.

The choice between soldering and other alternatives requires reconciliation of the fixturing problem inherent in soldering. For instance, in the welding process previously discussed all parts must be held in position for the welding period of 100 ms. The finished assembly advances and only one set of parts must be fixtured at a time. In a typical furnace reflow, the muffle is 14 to 15 feet long and product transit time is 30 minutes (belt speed of 15 in./minute). If the belt is 9 in. wide and 3-in.-diameter cells are being assembled in a rectangular face centered pattern, the throughput of the machine is 900 cells/hour but 450 cells are contained and fixtured within the muffle.

The route to higher throughput is a simple matter of increasing belt size which will increase the amount of fixturing required as well as the complexity of the input-output handling equipment. The advantages of solder reflow are:

- (a) It is a fully developed technology.
- (b) It can accommodate variations in cell parameters.
- (c) It is easily repairable.
- (d) It may be well suited to use with fragile cells.
- (e) It yields as reproducible and high strength interconnect bond.

Its disadvantages are:

- (a) It is more costly considering the cost of the bonding equipment, fixtures, power, and expended gases.
- (b) The resultant product may be more susceptible to environmental damage (i.e., high temperature and corrosion).
- (c) It is not compatible with several candidate subsequent processes by virtue of temperature limitations.

The Second Quarterly gives a specific reflow solder array assembly layout, and gives the cost breakdown. The summary of Fig. 11 (subsection G below) uses these costs.

3. Ultrasonic Welding

Ultrasonic welding of solar cells is still an experimental technique, although the AF HASPS program [9] has resulted in a qualified solar cell array using the technique. The motivation for pursuing the ultrasonic approach is twofold. First, the energy dissipated in making the metallurgical bond is substantially less (by over an order of magnitude) than the thermal alternatives. This makes it more compatible with shallow junction cells by reducing or eliminating semiconductor surface damage during metallurgical bonding. Secondly, the cost of interconnection may be smaller because of lower materials cost and higher throughput of the bonding equipment. Ultrasonic techniques are typically more uniform and controllable than the alternatives.

There are two variations of ultrasonic welding which are applicable to solar panel assembly; spot welding and seam welding. A third variation using ultrasonics is ring welding, which probably is not relevant to the solar cell applications.

Ultrasonic welding is a bonding technique by which similar or dissimilar metals can be bonded by the introduction of elastic vibratory energy at the interface between the metals to be joined. There is no heat involved except that associated with dissipation of the vibratory energy. Figure 6 shows schematically the construction required to deliver the energy to the joint. The transducer generally is a stack of nickel laminations vibrating at 40 to 60 kHz. The engineering design associated with the welding head primarily relates to the coupling of the energy into the weld area. The design of the coupling structure and the reflector has been developed to avoid frequency shift of resonance under load and to minimize dissipation of the vibratory energy in places other than the weldment interface. This development has been successfully completed by Sonobond Corporation for welding aluminum foil to itself or a more massive aluminum housing. It has been completed for welding fine wire to a semiconductor chip. It apparently has not been satisfactorily completed for welding aluminum foil to Si in a reproducible fashion.

9. G. Wolff et al., "Hardened Solar Power System," AFAPL-TR-74-53, Wright-Patterson AFB, Ohio, June 1974.

Figure 6. Transducer-coupling system.

There are two coupling system configurations which show promise for the solar cell application. First, for spot welds, small diameter tips, appropriately shaped and lightly loaded, have repeatably produced satisfactory welds between aluminum foil and Si solar cells with an energy input into the joint of approximately 1 joule for a welding period of appreciably less than 100 ms. Thus, such a bonding approach should be able to proceed at least as fast as the alternative of parallel gap welding with the energy dissipated at the solar surface being 10 to 25 times less. One would expect the interconnect design to be similar for both ultrasonic and parallel gap welding (namely, 3 welds per contact) so that the throughput of an ultrasonic bonder would be expected to be 300 cells per hour.

The alternate ultrasonic coupling system is a rolling member. In a very real sense, this coupling system creates an infinite number of weld spots to create a weld seam. Equipment which seams aluminum foil at 10 ft/minute is in production use. If these parameters could be maintained for bonding aluminum foil to solar cells, the throughput of the bonder could be increased to 1200 3-in. cells per hour, 2400 per hour if a double-headed bonder could be used. The energy density coupled into the silicon surface would be about 2.5 joules on the basis of equivalency to the 0.020 diameter spot previously discussed. The advantages of seam over spot welding are improved electrical conductance, redundancy, bond strength, and high welding throughput.

Each of these techniques has been fully costed out and the results shown in Fig. 11.

In addition to the three baseline bonding techniques already discussed, there are three additional second priority techniques which should be mentioned. These techniques are listed as second priority because there is a question about the reliability or cost effectiveness of the bond created. The three techniques are laser spot welding, thermocompression bonding, and conductive adhesive bonding.

4. Laser Welding

Production machinery to make four laser welds which assemble 1000 miniature relays per hour has been described [10]. The welds are 10 μm in diameter and 5 μm deep and require 1.5 joules per weld. The authors point out that laser welders cost 5 to 10 times equivalent conventional equipment but provide several otherwise unattainable requirements such as minimum deformation of delicate parts, ability to work with exotic materials, and better quality maintenance.

The 5- μm weld penetration is probably unsuitable for shallow junction cells; however, shorter time, higher power pulses reduce this penetration. A throughput of 1000 pieces per hour probably represents a good state-of-the-art estimate for the speed at which the solar cell bonding operations can be completed because of the similarity of silicon handling regardless of what bonding operation is used.

5. Thermocompression Bonding

Thermocompression bonding represents an interesting possibility for the interconnection of solar cells for two reasons. First, the bonding technique is well known in the semiconductor industry and high quality interconnects can be made with high yields on even the most fragile devices. Secondly, automated bonding is now done on multiple leads transported on a film carrier at high speed. Assembly of 14-pin packages at 1000 to 2500 per hour exists today with the possibility of 4000 per hour proposed.

10. Jean-Phillippe Aeschlimann & Pierre Monnier, "Automated Welding of Minute Parts," Laser Focus, March 1976.

There are major obstacles in translating this technology to solar cells, however. The necessity to stress the interconnecting metal interface to a high fraction of yield stress in order to promote diffusion bonding requires that the cell be well supported under the bonder. This usually calls for the semiconductor to be waxed or glued to a pedestal and for the bond to occur on small metal bumps (typically 4-mil² Au) formed on the semiconductor surface. Both of these requirements create cost and throughput problems when the semiconductor is a large area device.

A second obstacle is the cost of the film carrier used to facilitate the material handling. Presently, this is polyamide punched with sprocket and circuit aperture holes and a copper circuit pattern bonded and etched on the surface.

An ongoing NASA program (NAS8-31016) is investigating the feasibility of solar cell to bonding without "bumping." Final results have been reported [11], there can be no question that the technique needs substantial development work to be considered as a reliable production technique.

6. Conductive Adhesives

The same NASA program cited in the previous paragraph is also addressing the question of conductive adhesives for solar cell interconnection. They have had promising results with a Ag-filled conductive epoxy (DuPont 5504). Typically, the pull strength of their best samples was in the 200- to 300-gram range and joint electrical resistance in the 3-milliohm range. When assembled into a solar cell circuit, the resulting performance did not show significant degradation. There was variability in the pull strength of samples tested and a measurable reduction in average pull strength after temperature cycling. There seemed to be a high incidence of bond fractures when a large 72-cell module was temperature cycled. Considering the early status of this developmental effort maybe this should be expected. On the other hand, considering the stresses that can develop at a solar cell interconnection, the relatively poor strength of adhesive joints, and the susceptibility of the result to process variables, one would have to rate conductive adhesives as a second priority interconnection approach when compared with metallurgical processes.

11. "Interconnect & Bonding Technologies for Large Hex. Solar Arrays,"
Final Report NAS8-31016, Lockheed Missile & Space Co., July 26, 1976.

7. Automated Welding Station

There are two basic approaches to high-speed and low-cost interconnection of solar cells. In the Second Quarterly Report [5] we described an automated reflow facility which needs to be very large in order to get accurate buildup of cell temperature at high furnace belt speed. As a result of this large size several disadvantages occur:

- (a) Many cells are in the furnace at any given time and need to be fixtured to maintain necessary physical locations.
- (b) A large amount of power is required to maintain the large furnace volume at temperature.
- (c) A large amount of expendable atmosphere gas is required if reflow is to be completed without solder flux.
- (d) Pre-tinning will be required for most cell contact metal choices.

An alternative to the reflow approach is an automated welding approach using any of the welding techniques previously mentioned such as:

- Parallel GAP
- Ultrasonic
- Thermocompression
- Laser

The advantage of this approach is that only one set of parts must be fixtured at any one time since the parts are bonded in a fraction of a second and are subsequently held in position by virtue of their own strength. Bonding energy is applied very locally, and, therefore, power consumption is very low in this process. Finally, the metallurgical parameters such as oxide removal are much more favorable with welding because of the high temperature and mechanical abrasion and metal forging which occurs during the process.

Figure 7 is a drawing showing an automated welding station which uses several of the material-handling techniques previously discussed integrated together with welding heads to yield a high speed assembly facility. It utilizes parallel cap equipment to do the welding and a combination of existing indexing and wafer handling equipment to accomplish the required material handling. The arrangement of equipment shown in Fig. 7 allows all of the steps required to make a cell-to-cell connection to be done in parallel, resulting in very high throughput for the system.

Figure 7. Automatic welding station equipment.

The basic timing for the system is established by the indexing rate of the rotary table. We have chosen a cycle time of 4.6 seconds (1.6 seconds of travel and 3.0 seconds of dwell) since this coincides with the requirements established for the wafer loader at station 1. The timing for each of the stations and the equipment located there is described in the following table and supporting text.

a. Station 1. Load Position

Station 1 contains a commercially available module, air bearing transport, and a buffer wafer storage cartridge. The sender module and track require 1/10 cfm of nitrogen and a trigger signal from the control module. Maximum index time is 0.4 second and maximum transfer time is 3.0 seconds. The module cost is \$1,000 with an estimated additional \$1,000 required to integrate it into the system.

b. Station 2. Interconnect Formation

This position contains a ribbon feed, interconnect formation and cut-off die set, and interconnect placement module. This position will have a special design but is made up using standard and well known techniques. It is estimated that the station will use 1 cfm of compressed air and 50 W of electrical power. Total cost is estimated at \$15,000.

c. Station 3, Station 4, and Station 8. Parallel Gap Welder

Each station contains a power supply, an auxiliary power pack, a weld head, and pneumatic actuator. It is estimated that each welder, assembled and integrated into the system, will cost \$7,500. Each station will require 200 W of electrical power and consume electrodes for every 150 hours of operation. At a cost of \$50/ect, this amounts to \$0.00055/cell. An ultrasonic weld head could easily be substituted in this position if that becomes appropriate.

d. Station 5. Wafer Turner

The requirement to weld both sides of the cell necessitates a position to turn over the cells in order to present the P contacts to the weld for series connection. The equipment at this station is relatively simple and estimated to cost \$2,000 with minimal power required.

e. Station 6. Pickup Position

Transfer of the cells from the rotary table to the X-Y tables will be accomplished using a available pick and place robot arm. This mechanism will have to be modified for vacuum pickup and operation with the central controller. The cost of this position, integrated with the system, will be \$5,000. Power consumption is 300 W.

f. Station 7. Series Connection Table

Series connection will be on an N/C controlled X-Y table. This table is 8 x 48 in. with 48-in. travel. It moves on ball bushing ways, with precision stepper motor drive. The motion of this table is synchronized with the rotary index table. It indexes in the X-Y directions to accomplish a repeating pattern of four series welds, provides a pause for string pickup after 20 cells are welded, and then makes a quick return to the starting position in 10 seconds. The machine has been quoted at \$10,000 and requires 300 W of input power.

g. Rotary Index Table

Stations 1 through 6 are located around an available index table. The basic table cost is \$2,500 with a power consumption of 500 W. Each position has a vacuum chuck, two locating pins, and a flat finder. The addition of vacuum chuck and flat locator at each position will add \$1,500/position or \$9,000 to the cost. In addition, a vacuum pump and N₂ regulator system will add another \$1,000, making the total cost \$12,500.

h. Microprocessor Controller

The control of the welding system will be accomplished through a microprocessor master controller. This controller will synchronize all of the stations and provide for interlocks between stations. It will automatically reset the system in the event of a malfunction in any operation. In addition, it will provide automatic process monitoring, fast process reconfiguration, and monitor weld quality. This system has not been designed but by similarity, it can be priced at \$15,000.

i. Sensors, Actuators, Assembly and Miscellaneous Hardware

Integration and assembly of the subsystems described are the most difficult to define at this stage but most probably will be the most expensive to accomplish. We are estimating \$20,000 for this part of the system.

Table 2 summarizes the cost and power estimates for this system.

TABLE 2. COST AND POWER SUMMARY

<u>Station</u>	<u>Cost</u>	<u>Power</u>
1	\$ 2,000	
2	15,000	50
3	7,500	200
4	7,500	200
5	2,000	
6	5,000	300
7	10,000	300
8	7,500	200
Rotary Table	12,500	750
Microprocessor	15,000	50
Assembly	<u>20,000</u>	
	\$104,000	<u>2,050 w</u>

j. System Throughput

The time required to produce a 20-cell string is greater than 20 times the process time for a single cell. The timing diagram in Table 3 shows the string assembly step.

TABLE 3. TIMING DIAGRAM

<u>Operation</u>	<u>Time</u>
Interconnect 5 cells @ 4.6 seconds	23.0
Burnish electrodes	4.6
Interconnect 5 cells	23.0
Burnish electrodes	4.6
Interconnect 5 cells	23.0
Burnish electrodes	4.6
Interconnect 5 cells	23.0
Burnish electrodes	4.6
Lift finished string	4.6
Return X-Y table to start	<u>4.6</u>
	119.6 seconds

k. Panel Assembly

The welding station described in this report integrates with a panel assembly area previously described in the Second Quarterly Report and shown in the floor plan of Fig. 8.

Figure 8. Automatic welding station floor plan.

This approach has the great advantage of completing all of the preliminary operations such as positioning, interconnect formation, and P contact bonding off line in parallel fashion. If additional contact preparation steps such as burnishing to improve weldability are needed, they can be added to the rotary table position without affecting station throughput. It is also probable that two rotary positions could be used to supply the final connection on the X-Y table with only nominal increase in station cost.

The critical questions which must be answered relate to the structural and electrical quality of the interconnect bonds which can be made on a "hands off" basis with the cell and contact designs which are necessary for low cost.

F. PACKING FOR SOLAR CELL CIRCUITS

In our previous discussion on panel materials, it was indicated that there is no substantial cost advantage in going to the transparent organic films or coatings for environmental protection of solar cells over the alternative of glass. There is, in fact, good reason to suspect that such systems may compromise circuit life because of corrosion problems caused by vapor transmission to the semiconductor surface. It has been our objective in the past quarter to look for circuit packaging approaches which use glass as the enclosure material and show potential for lower cost.

Three alternatives are being evaluated: tubular enclosure, laminated glass sandwich, and coated substrate. These alternatives are being examined because they represent three form factors which retain the advantages of glass packaging but present options in geometry and assembly methodology which offer economic advantages that must be traded against possible performance loss of system reliability uncertainty.

Table 4 shows a list of commercially available glass of different compositions and geometry that have been considered in this investigation. The comparisons of these materials are made on the basis of the three basic structures being considered which are shown in Fig. 9.

Briefly summarized, the advantages and disadvantages of each of the alternatives are as follows. The tubular format can utilize thinner glass and

(a) TUBULAR CONCEPT

(b) GLASS SANDWICH

(c) COATED SUBSTRATE

Figure 9. Packaging structures.

TABLE 4. PACKAGING MATERIALS

Designation	Material	Material Form	Expansion Coefficient $^{\circ}\text{C} \times 10^7$	Cost \$/lb
Clear Float	Soda Lime	1/4 Sheet	85	0.131
		1/8 Sheet	85	0.138
		1/16 Sheet	85	0.238
R6	Soda Flint-Flint	25 mm Tubing		0.256
R6	Soda Flint-Flint	51 mm Tubing		0.412
N51	Alumina Borosilicate	25 mm Tubing	49	0.420
N51	Alumina Borosilicate	51 mm Tubing	49	1.026
KG33/7740	Low Expansion Borosilicate	25 mm Tubing	32	2.61
KG33/7740	Low Expansion Borosilicate	51 mm Tubing	32	2.83

still satisfy structural requirements for the protective package. Thus, the glass coat in the assembly can be minimized. The disadvantage of this approach is that it is difficult to remove heat buildup at the solar cell surface. The glass sandwich offers a highly reliable total enclosure of the cells from moisture penetration. If front and back sheets can be structurally tied together with the occasional supports shown in Fig. 9, each of the face sheets can be reduced in thickness and thus cost while maintaining the necessary structural integrity. The disadvantage of the approach is potential thermal stress problems. Finally, the coated substrate is the easiest to implement at reasonable cost and reasonable moisture hermeticity. However, it still requires expensive transparent bonding material on the sunlit side and the coated face has questionable durability.

Without regard to the solution, which may have substantial cost impact, to problems presented by the disadvantages cited, Table 5 shows the cost comparisons for the materials shown in Table 4.

The conclusion which can be drawn from this comparison is that some material cost savings can be realized by going either to the glass sandwich or glass tube alternatives. The primary reasons for this are (1) elimination of the expensive transparent adhesive and (2) the use of thinner, cheaper glass

TABLE 5. COST COMPARISONS OF PACKAGING MATERIALS

<u>Item</u>	<u>I</u>	<u>II</u>	<u>III</u>	<u>IV</u>	<u>V</u>	<u>VI</u>	<u>VII</u>
Substrate							
1/16 glass sheet					0.19		
1/8 glass sheet		0.22					
0.005 alum. foil			0.05			0.05	0.05
Cell Adhesive							
RTV615/Primer	0.41			0.41			
RTV 102		0.10	0.10		0.10	0.10	0.10
Window							
1/16 glass sheet					0.19		
1/8 glass sheet		0.22		0.22			
1/4 glass sheet	0.44						
1 in. diam. R6 tubing			.45				
1 in. diam. NSI tubing						0.60	
2 in. diam. R6 tubing							1.07
Assembly Closure							
Conformal coating + 3-mil metal	0.11			0.11			
Edge seal		0.04			0.06	0.06	0.03
End caps			0.06				
Panel Connector	0.09	0.09	0.18	0.36	0.36	0.18	0.13
Aluminum Structural Channel	0.10	0.10	0.10	0.15	0.15	0.10	0.10
Total	1.15	0.77	0.94	1.25	1.05	1.09	1.48

Column Identification:

- I - 1/4 glass with conformal coating 4 x 4 ft module
- II - 1/8 glass window and substrate bonded together 4 x 4 ft module
- III - 1-in.-diameter R6 tubing with aluminum for substrate (48 tubes in module)
- IV - 1/8 glass with conformal coating (4) 2 x 2 ft panels in a 4 x 4 ft module
- V - 1/16 glass window and substrate bonded together into (4) 2 x 2 ft panels in a 4 x 4 ft module
- VI - 1-in.-diameter NSI tubing with aluminum foil substrate (48 tubes in module)
- VII - 2-in.-diameter R6 tubing with aluminum foil substrate (24 tubes in module)

for the window. Additional experimental work is necessary to determine if two 1/8 glass sheets bonded elastically are equivalent to a single 1/4 sheet in response to impact and structural loads. Likewise, the thermal stress problems in the sandwich construction are being studied.

Some preliminary thermal analysis has been completed on the tubular construction. Figure 10 shows four tubular construction alternatives configured to promote heat rejection from the solar cell surface. There is cost associated with alternatives b, c, and d which has not yet been completely evaluated. In addition, alternatives c and d do not have a single value of temperature associated with the construction. In the case of forced convection cooling, the fan power required to maintain the cells at a temperature equivalent to flat plate construction has been calculated (41°C above ambient temperature). This fan power is listed as a fraction of the electrical produced by the panel. In the case of heat pipe cooling the material cost associated with the required heat pipe has been estimated. These temperatures and auxiliary requirements are summarized in Table 6. It would not appear that alternatives c and d would be justified unless a combined thermal and electrical system is built because of the effectiveness of the extended substrate (b) in cooling the structure.

TABLE 6. TEMPERATURE REQUIREMENTS FOR AVAILABLE ALTERNATIVES

<u>Alternative</u>	<u>Temperature</u>	<u>Auxiliary Requirement</u>
a	136°C	
b	71°C	
c	78°C	4.5% of Output Power
d	78°C	\$.77/ft ² for Heat Pipe
Flat Plate Reference	78°C	

Ambient Temp = 37°C.

The additional materials cost associated with the extended foil substrate and the opaque adhesive is \$0.25/ft². This cost amounts to an increase of \$0.03/W for the typical panel. Circulating the air results in

(a) BASELINE ALTERNATIVE

(b) EXTENDED SUBSTRATE ALTERNATIVE

(c) FORCED CONVECTION ALTERNATIVE

(d) HEAT PIPE ALTERNATIVE

Figure 10. Tubular construction alternatives.

about \$0.04/W increase while the heat pipe alternative increases the cost by \$0.1/W. It would seem the extended substrate tube alternative cannot be completely ruled out on a temperature basis.

G. TOTAL ARRAY MANUFACTURING COSTS

1. Example of Cost Analysis Procedure

Figure 11 is the process cost estimate summary for all the processes which have been evaluated. The cost of each process is broken down into:

- MAT'L - Material consumed
- D.L. - Direct labor
- EXP. - Expense items
- P.OH. - Process overhead
- INT - Interest on capital
- DEPR. - Depreciation of capital
- TOTALS - Total cost of one single process assuming 100% yield for all subsequent processes
- INVEST - Capital investment for this process.

In every case the costs are presented as \$/W, with the assumption of the cell performance given at the top of the page. In Fig. 11, the cells are 7.8-cm-diameter wafers, with a power conversion efficiency of 11%.

The definition of labor types, material and expense items, capital costs, and array size can be found in Fig. 12, (general inputs to the analysis). For a definition of all the terms, refer to the Appendix of the Second Quarterly Report [5].

In this section, we will describe one complete manufacturing cost analysis in detail. The total manufacturing sequence is shown in Fig. 13. This "Process Cost Overview" is a 12-step process which begins with 7.8-cm-diameter wafers which cost nothing and results in solar array modules which produce electricity at a cost of \$0.9/peak W AM1. The overall yield of this sequence is 51.1%.

Each of the processes 1 through 12 are taken from the "Process Cost Estimate" summary in Fig. 11. When these processes are taken together as a process sequence as shown in Fig. 13, the manufacturing cost of each step is divided by the product of the yields for all subsequent steps.

PROCESS COST ESTIMATE-\$/WATT										
ASSUMPTIONS: 0.500 WATTS PER SOLAR CELL AND \$ 0.0 FOR 7.8 CM (3") DIAMETER WAFER										
100% YIELD FOR ALL PROCESSES FOLLOWING.										
ITEM	YIELD	PROCESS	MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	TOTALS	INVEST
1	99.0%	SYSTEM "2" WAFER CLEANING	0.0	0.013	0.002	0.009	0.000	0.001	0.024	0.005
2	99.0%	SYSTEM "2" WAFER CLEANING-1	0.0	0.013	0.002	0.009	0.000	0.001	0.024	0.005
3	99.0%	SYSTEM "2" WAFER CLEANING-2	0.0	0.013	0.002	0.009	0.000	0.001	0.024	0.005
4	99.5%	SC-1 CLEANING	0.0	0.007	0.035	0.004	0.001	0.001	0.048	0.010
5	99.0%	PLASMA CLEANING/ASHING	0.0	0.021	0.045	0.026	0.003	0.006	0.100	0.039
6	99.5%	WAFER SCRUBBER	0.0	0.038	0.004	0.022	0.003	0.004	0.071	0.031
7	99.0%	MEGASONIC CLEANING	0.0	0.020	0.008	0.014	0.002	0.002	0.045	0.017
8	95.0%	TEXTURIZING:HYDRAZINE	0.0	0.027	0.020	0.030	0.001	0.002	0.080	0.013
9	95.0%	TEXTURIZING:SODIUM HYDROXIDE	0.0	0.027	0.004	0.030	0.001	0.002	0.064	0.013
10	95.0%	SPIN-ON SOURCE	0.0	0.016	0.006	0.013	0.001	0.002	0.038	0.012
11	95.0%	SPIN-ON SOURCE-1	0.0	0.016	0.006	0.013	0.001	0.002	0.038	0.012
12	95.0%	SPIN-ON SOURCE-2	0.0	0.016	0.006	0.013	0.001	0.002	0.038	0.012
13	99.0%	SPRAY-ON SOURCE	0.0	0.014	0.005	0.017	0.001	0.002	0.039	0.012
14	99.0%	200 DEG. C. BAKE	0.0	0.011	0.000	0.008	0.000	0.000	0.019	0.001
15	99.0%	200 DEGREE C. OVEN BAKE-1	0.0	0.011	0.000	0.008	0.000	0.000	0.019	0.001
16	99.0%	200 DEGREE C. OVEN BAKE-2	0.0	0.011	0.000	0.008	0.000	0.000	0.019	0.001
17	98.0%	DIFFUSION	0.0	0.009	0.004	0.008	0.001	0.002	0.024	0.012
18	98.0%	SILICON SOURCE DIFFUSION	0.0	0.010	0.018	0.009	0.002	0.003	0.041	0.018
19	99.0%	POCL3 DEPOSITION AND DIFFUSION	0.0	0.009	0.028	0.007	0.004	0.006	0.055	0.044
20	99.0%	DOPED OXIDE DEPOSITION	0.0	0.021	0.033	0.021	0.008	0.013	0.096	0.092
21	75.0%	EPITAXIAL GROWTH(A)	0.0	0.100	1.448	0.360	0.150	0.238	2.297	1.666
22	85.0%	CLOSE SPACE EPITAXY(B)	0.0	0.041	0.248	0.028	0.039	0.062	0.418	0.435
23	99.0%	ION IMPLANT(A)	0.0	0.026	0.012	0.030	0.039	0.061	0.168	0.430
24	99.0%	ION IMPLANT-FRONT(A)	0.0	0.026	0.012	0.030	0.039	0.061	0.168	0.430
25	99.0%	ION IMPLANT-BACK(A)	0.0	0.026	0.012	0.030	0.039	0.061	0.168	0.430
26	99.0%	ION IMPLANT(B)	0.0	0.005	0.012	0.017	0.008	0.013	0.055	0.088
27	99.0%	ION IMPLANT-FRONT(B)	0.0	0.005	0.012	0.017	0.008	0.013	0.055	0.088
28	99.0%	ION IMPLANT-BACK(B)	0.0	0.005	0.012	0.017	0.008	0.013	0.055	0.088
29	99.0%	FRONT SIDE RESIST APPLICATION	0.0	0.004	0.071	0.003	0.002	0.004	0.084	0.027
30	99.5%	RESIST REMOVAL	0.0	0.003	0.010	0.003	0.001	0.002	0.018	0.011
31	99.5%	GLASS REMOVAL	0.0	0.008	0.023	0.006	0.001	0.001	0.038	0.008
32	99.5%	GLASS REMOVAL-1	0.0	0.008	0.023	0.006	0.001	0.001	0.038	0.008
33	99.5%	GLASS REMOVAL-2	0.0	0.008	0.023	0.006	0.001	0.001	0.038	0.008
34	99.5%	BACK ETCH	0.0	0.008	0.023	0.006	0.001	0.001	0.038	0.008
35	95.0%	RIM ETCH	0.0	0.007	0.034	0.011	0.002	0.004	0.057	0.028
36	100.0%	POST DIFFUSION INSPECTION	0.0	0.003	0.000	0.002	0.000	0.000	0.006	0.001
37	98.0%	VACUUM EVAPORATION METALLIZATION	0.0	0.095	0.018	0.080	0.030	0.047	0.270	0.328
38	98.0%	TI/AG METALLIZATION-FRONT	0.070	0.025	0.010	0.000	0.034	0.033	0.333	0.383
39	98.0%	TI/AG METALLIZATION-BACK	0.109	0.095	0.018	0.080	0.034	0.055	0.392	0.383
40	98.0%	MAGNETRON SPUTTERING TI/AG:FRONT	0.093	0.040	0.024	0.033	0.051	0.082	0.323	0.572
41	98.0%	MAGNETRON SPUTTERING TI/AG:BACK	0.115	0.040	0.024	0.033	0.051	0.082	0.345	0.572
42	98.0%	MAGNETRON SPUTTERING AL:FRONT	0.011	0.085	0.052	0.071	0.111	0.177	0.508	1.236
43	98.0%	MAGNETRON SPUTTERING AL:BACK	0.011	0.085	0.052	0.071	0.111	0.177	0.508	1.236
44	98.0%	THICK FILM METALLIZING:AUTO	0.0	0.002	0.008	0.008	0.002	0.004	0.024	0.028
45	98.0%	THICK AG METAL-FRONT:AUTO	0.006	0.002	0.008	0.008	0.002	0.004	0.029	0.028
46	98.0%	THICK AG METAL-BACK:AUTO	0.037	0.002	0.008	0.008	0.002	0.004	0.061	0.028
47	98.0%	THICK AL/AG METAL-BACK:AUTO	0.113	0.003	0.016	0.016	0.004	0.007	0.158	0.046
48	99.0%	SILICON NITRIDE PASSIVATION	0.0	0.032	0.007	0.029	0.012	0.020	0.100	0.138
49	95.0%	AR COATING:SPIN-ON(A)	0.0	0.042	0.075	0.039	0.001	0.002	0.159	0.012
50	95.0%	AR COATING:SPIN-ON(B)	0.0	0.029	0.019	0.027	0.001	0.002	0.078	0.012
51	99.0%	AR COATING:EVAPORATE(A)	0.0	0.140	0.028	0.145	0.034	0.055	0.402	0.382
52	80.0%	TEST	0.0	0.012	0.000	0.013	0.005	0.007	0.037	0.051
53	96.0%	ARRAY FAB.:REFLOW SOLDER(A)	0.423	0.054	0.002	0.060	0.010	0.016	0.564	0.111
54	96.0%	ARRAY FAB.:REFLOW SOLDER(B)	0.216	0.054	0.002	0.060	0.010	0.016	0.358	0.111
55	96.0%	ARRAY FAB.:GAP WELDING(A)	0.382	0.044	0.001	0.054	0.011	0.017	0.509	0.121
56	96.0%	ARRAY FAB.:GAP WELDING(B)	0.155	0.044	0.006	0.054	0.011	0.017	0.287	0.121
57	96.0%	ARRAY FAB.:ULTRASONIC(A)	0.378	0.044	0.001	0.054	0.012	0.019	0.508	0.136
58	96.0%	ARRAY FAB.:ULTRASONIC(B)	0.156	0.044	0.001	0.054	0.012	0.019	0.287	0.136

Figure 11. Process cost estimates.

PURCHASED SILICON COST: 0. \$/SHEET.
 2ND & 3RD SHIFT PREMIUM FACTORS:1.10,1.10
 ESE MARKUP-DIRECT,INDIRECT LABOR: 35.0%, 35.0%
 WORKING DAYS PER YEAR:245
 SHEET:7.8 CM (3") DIAMETER WAFER
 WT. OF SHEET: 7.350 G.
 SHEET AREA: 47.80 SQ. CM.
 SOLAR CELLS PER SHEET: 1
 SOLAR CELLS PER ARRAY MODULE: 140
 WATTS PER SOLAR CELL(DEFAULT): 0.50
 ANNUAL PRODUCTION: 50000000. WATTS.
 TAX DEPR. METHOD:SYD
 BOOK DEPR. METHOD:SL
 INTEREST RATE ON BORROWED FUNDS: 9.0%
 PERCENT OF INVESTMENTS FINANCED BY DEBT:100.0%
 DIRECT LABOR TYPES
 HOURLY OPERATOR 4. \$/HR.
 HOURLY INSPECTOR 4. \$/HR.
 INDIRECT LABOR TYPES
 SUPERVISORY 13000. \$/YR.
 ENGR. SUPPORT 17000. \$/YR.
 MACH. ATTENDANT 9400. \$/YR.
 TECHNICIAN 11500. \$/YR.
 CLERICAL 8300. \$/YR.
 QUALITY CONTROL 8300. \$/YR.
 MAINTENANCE 8300. \$/YR.
 HANDLER 8300. \$/YR.
 EXPENSE DEFINITIONS:MATERIAL
 ALUMINUM FINAL ASSEMBLY MATERIAL CONFORMAL COAT+3MIL MET.
 PANEL CONNECTOR AL CHANNEL INK AG
 INK AL INTERCONNECT MATERIAL ELECTRODES
 AG-PLATED CU WIRE PANEL ASSEMBLY MATERIAL SUBSTRATE
 CELL ADHESIVE WINDOW SILVER
 TITANIUM
 EXPENSE DEFINITIONS:DIRECT EXP.
 ACETIC ACID AMMONIA AMMONIA/NITROGEN
 BOATS,LINERS,ETC. DEVELOPER DI WATER
 DIBORANE 5% ELECTRICITY FILAMENTS/INSULATORS
 FILTERS GAS MIXTURE HYDRAZINE
 HYDROCHLORIC ACID HYDROFLUORIC ACID HYDROGEN
 HYDROGEN CHLORIDE HYDROGEN PEROXIDE ION SOURCE GAS
 LIME LIQUID NITROGEN MISCELLANEOUS
 NITRIC ACID NITROGEN NITROGEN CURTAINS
 OXYGEN PHOSPHORUS OXYCHLORIDE PHOTORESIST
 QUARTZ QUARTZ WARE SCREENS
 SILANE 100% SODIUM HYDROXIDE SOLVENT
 SOURCE WAFERS SPIN-ON A/R COATING SPIN-ON SOURCE
 SPRAY-ON SOURCE SQUEEGEES SULFURIC ACID
 SUPPORT & TC SUSCEPTORS TANTALUM PENTOXIDE
 TRANSDUCERS & TUBES TRICHLORSILANE WATER

Figure 12. General inputs.

PROCESS COST OVERVIEW-\$/WATT														
ASSUMPTIONS:		0.500 WATTS PER SOLAR CELL AND \$ 0.0 FOR 7.8 CM (3") DIAMETER WAFER												
STEP	YIELD	PROCESS	MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALV6.	TOTALS	% INVEST	%	
1	99.0%	SYSTEM "Z" WAFER CLEANING	0.0	0.021	0.003	0.014	0.001	0.001	0.039	0.0	0.039	4.4	0.008	2.0
2	95.0%	SPIN-ON SOURCE	0.0	0.025	0.009	0.021	0.002	0.003	0.059	0.0	0.059	6.5	0.018	4.4
3	99.0%	200 DEG. C. BAKE	0.0	0.016	0.000	0.013	0.000	0.000	0.029	0.0	0.029	3.3	0.002	0.4
4	99.0%	POCL3 DEPOSITION AND DIFFUSION	0.0	0.014	0.042	0.011	0.006	0.009	0.082	0.0	0.082	9.1	0.065	15.9
5	99.5%	GLASS REMOVAL	0.0	0.011	0.035	0.008	0.001	0.002	0.057	0.0	0.057	6.3	0.012	2.8
6	95.0%	RIM ETCH	0.0	0.009	0.048	0.015	0.003	0.005	0.082	0.0	0.082	9.1	0.038	9.4
7	100.0%	POST DIFFUSION INSPECTION	0.0	0.004	0.000	0.003	0.000	0.000	0.008	0.0	0.008	0.9	0.001	0.2
8	98.0%	THICK AG METAL-FRONT:AUTO	0.008	0.002	0.011	0.011	0.003	0.005	0.041	0.0	0.041	4.5	0.038	9.3
9	98.0%	THICK AG METAL-BACK:AUTO	0.051	0.002	0.011	0.011	0.003	0.005	0.083	-0.007	0.076	8.4	0.037	9.1
10	95.0%	ANTIREFLECTION COATING:SPIN-ON	0.0	0.038	0.025	0.035	0.001	0.002	0.102	0.0	0.102	11.3	0.016	3.9
11	80.0%	TEST	0.0	0.012	0.001	0.014	0.005	0.008	0.039	0.0	0.039	4.3	0.053	12.9
12	96.0%	ARRAY FABRICATION:GAP WELDING(B)	0.155	0.044	0.006	0.054	0.011	0.017	0.287	0.0	0.287	31.8	0.121	29.6
	61.1%	TOTALS	0.213	0.199	0.190	0.210	0.037	0.059	0.908	-0.007	0.901	100.0	0.410	100.0
			\$	23.49	21.91	20.96	23.13	4.06	6.44	100.00				

The impact of a non-zero cost for the starting Si wafer is shown in Fig. 14. For example, if the starting wafer cost is in fact \$0.15, the cost of the array modules is \$1.39/peak W.

For every one of the processes of Fig. 11, there is input data describing that process. Figures 15 through 27 are the input data sheets for the twelve processes of Fig. 13. From these input sheets come all the data for the subsequent analysis.

3. Output Data

Figure 30 is the summary of the investments. The program has purchased a sufficient number of machines in each category to satisfy the production requirements.

COST/WATT AS A FUNCTION OF STARTING SHEET COST
(PROCESS \$ DOES NOT INCLUDE COST OF 7.8 CM (3") DIAMETER WAFER)

PROCESS YIELD= 61.1%					
SHEET \$	SHEET YIELD LOSS \$	PROCESS \$	TOTAL \$	\$ /WATT	
0.0	0.0	0.45	0.45	0.90	
0.05	0.03	0.45	0.53	1.07	
0.10	0.06	0.45	0.61	1.23	
0.15	0.10	0.45	0.70	1.39	
0.20	0.13	0.45	0.78	1.56	
0.25	0.16	0.45	0.86	1.72	
0.30	0.19	0.45	0.94	1.88	
0.35	0.22	0.45	1.02	2.05	
0.40	0.26	0.45	1.11	2.21	
0.45	0.29	0.45	1.19	2.38	
0.50	0.32	0.45	1.27	2.54	
0.55	0.35	0.45	1.35	2.70	
0.60	0.38	0.45	1.43	2.87	
0.65	0.41	0.45	1.52	3.03	
0.70	0.45	0.45	1.60	3.19	
0.75	0.48	0.45	1.68	3.36	
0.80	0.51	0.45	1.76	3.52	
0.85	0.54	0.45	1.84	3.69	
0.90	0.57	0.45	1.92	3.85	
0.95	0.61	0.45	2.01	4.01	
1.00	0.64	0.45	2.09	4.18	
1.25	0.80	0.45	2.50	5.00	
1.50	0.96	0.45	2.91	5.81	
1.75	1.12	0.45	3.32	6.63	
2.00	1.28	0.45	3.73	7.45	
2.25	1.44	0.45	4.14	8.27	
2.50	1.59	0.45	4.55	9.09	
2.75	1.75	0.45	4.95	9.91	
3.00	1.91	0.45	5.36	10.73	
3.25	2.07	0.45	5.77	11.55	
3.50	2.23	0.45	6.18	12.37	
3.75	2.39	0.45	6.59	13.19	
4.00	2.55	0.45	7.00	14.00	
4.25	2.71	0.45	7.41	14.82	
4.50	2.87	0.45	7.82	15.64	
4.75	3.03	0.45	8.23	16.46	
5.00	3.19	0.45	8.64	17.28	
5.25	3.35	0.45	9.05	18.10	
5.50	3.51	0.45	9.46	18.92	
5.75	3.67	0.45	9.87	19.74	
6.00	3.83	0.45	10.28	20.56	

Figure 14. Cost analysis: Ag screen printing.

WAFERS ARE CLEANED IN SULFURIC/HYDROGEN PEROXIDE MIXTURE
ASSUMPTIONS:

1. MATERIALS CONSUMED RISE LINEARLY WITH SILICON AREA.
 2. LABOR COSTS ARE INVARIANT WITH RESPECT TO SHEET SIZE AND
DEPEND ONLY ON NO. OF SHEETS PROCESSED.
 3. EQUIPMENT COSTS AND FLOOR SPACE ARE LINEARLY RELATED TO TOTAL
SILICON AREA. (MEASUREMENT EQUIPMENT NOT AREA RELATED)
 4. COST OF EQUIPMENT FOR ANY SILICON FORMAT IS ASSUMED DEPENDENT
ONLY ON AREA PER SHEET.
 5. 3" DIAMETER WAFER, 12-14 MILS THICK, (100) ORIENTATION, P-TYPE,
1-5 OHM CM.
 6. COSTS ARE BASED ON FRONT OF WAFER AREA. BACK OF WAFER "FREE".
- YIELD: 99.0% IN:SHEETS OUT:SHEETS
SALVAGE VALUE: 0.0% OF \$ COST OF 7.8 CM (3") DIAMETER WAFER
3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS			
INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME: 6" HOOD EFF.: 95.0% THRUPT: 650. SH/HR
% PROCESSED: 100.0 COST: 9000. MAINT. \$/HR: 0.0 TAX CR.: YES
YEARS OF LIFE-USEFUL: 10 BOOK: 7 TAX: 7 AREA: 100. SQ. FT.

DIRECT LABOR TYPE	INPUT UNITS/HR	PERCENT EFFICIENCY
HOURLY OPERATOR	750.	100.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.050	0.050	0.050
ENGR. SUPPORT	0.025	0.025	0.025
CLERICAL	0.0	0.0	0.0
QUALITY CONTROL	0.0	0.0	0.0
MAINTENANCE	0.050	0.050	0.050

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE	% PROCESSED
ELECTRICITY	0.	0.0	0.000280	AREA	100.0%
SULFURIC ACID	0.	0.0	0.000330	AREA	100.0%
HYDROGEN PEROXIDE	0.	0.0	0.000500	AREA	100.0%
DI WATER	0.	0.0	0.000750	AREA	100.0%

NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 15. System "2" wafer cleaning
input data sheet.

DIFFUSION SOURCE FORMED BY CONTACTING SILICON SURFACE WITH LIQUID.

ASSUMPTIONS:

1. SEE *SYSTEM "Z" WAFER CLEANING*

2. P-TYPE SOURCE:

TEOS (TETRAETHYDORTHOSILICATE) \$.340
ACETIC ANHYDRIDE .160
METHANOL .098
BORIC OXIDE .023

TOTAL \$0.621 PER BATCH

EACH BATCH PROVIDES ABOUT 156 WAFERS, EACH

100 SQ. CM IN AREA. COST PER 100 SQ. CM.: \$.005

N-TYPE SOURCE SAME COST AS P-TYPE SOURCE.

YIELD: 95.0% IN:SHEETS OUT:SHEETS

SALVAGE VALUE: 0.0% OF \$ COST OF 7.8 CM (3") DIAMETER WAFER

3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS

INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME:III SPINNER EFF.: 85.0% THRUPUT: 400. SH/HR
% PROCESSED:110.0 COST: 10000. MAINT. \$/HR: 0.0 TAX CR.:YES
YEARS OF LIFE-USEFUL:10 BOOK: 7 TAX: 7 AREA: 300. SQ. FT.

DIRECT LABOR TYPE INPUT UNITS/HR PERCENT EFFICIENCY
HOURLY OPERATOR 680. 110.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.050	0.050	0.050
ENGR. SUPPORT	0.025	0.025	0.025
CLERICAL	0.0	0.0	0.0
QUALITY CONTROL	0.0	0.0	0.0
MAINTENANCE	0.150	0.150	0.150

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE	% PROCESSED
ELECTRICITY	0.	0.0	0.000400	AREA	110.0%
SPIN-ON SOURCE	0.	0.0	0.005000	AREA	110.0%

NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 16. Spin-on source input data sheet.

WAFERS ARE BAKED IN AIR OVEN AT 200 DEG. C. FOR 1/2 HR.
 ASSUMPTIONS:
 1. SEE "SYSTEM "2" WAFER CLEANING"
 YIELD: 99.0% IN:SHEETS OUT:SHEETS
 SALVAGE VALUE: 0.0% OF \$ COST OF 7.6 CM (3") DIAMETER WAFER
 3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS
 INPUT UNITS AREA(SQ.FT.) INPUT UNITS AREA(SQ.FT.)
 0. 0. 0. 0.
 0. 0. 0. 0.

INVESTMENTS

NAME:200 DEG. C. OVEN EFF.: 90.0% THRUPUT: 1000. SH/HR
 % PROCESSED:100.0 COST: 1000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL: 7 BOOK: 7 TAX: 7 AREA: 100. SQ. FT.

NAME:MECHANICAL STACKER EFF.: 90.0% THRUPUT: 1000. SH/HR
 % PROCESSED:100.0 COST: 2000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL: 7 BOOK: 7 TAX: 7 AREA: 5. SQ. FT.

DIRECT LABOR TYPE INPUT UNITS/HR PERCENT EFFICIENCY
 HOURLY OPERATOR 900. 100.0% 85.0%

INDIRECT LABOR TYPE 1ST SHIFT RATIO 2ND SHIFT RATIO 3RD SHIFT RATIO
 SUPERVISORY 0.100 0.100 0.100
 ENGR. SUPPORT 0.0 0.0 0.0
 CLERICAL 0.0 0.0 0.0
 QUALITY CONTROL 0.0 0.0 0.0
 MAINTENANCE 0.100 0.100 0.100

MATERIAL/EXPENSE NAME PROD. LIMIT FIXED \$ PART VAR. \$ PART BASE % PROCESSED
 ELECTRICITY 0. 0.0 0.000040 AREA 100.0%
 NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 17. 200°C bake input data sheet.

DOPANT SOURCE BY DECOMPOSITION OF POCL₃ IN A DIFFUSION FURNACE
ASSUMPTIONS:

1. SEE "SC-1 CLEANING" ASSUMPTIONS

YIELD: 99.0% IN:SHEETS OUT:SHEETS

SALVAGE VALUE: 0.0% OF \$ COST OF 7.8 CM (3") DIAMETER WAFER

3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS

INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME:DIFFUSION FURNACE EFF.: 85.0% THRUPUT: 300. SH/HR
% PROCESSED:100.0 COST: 32000. MAINT. \$/HR: 0.02 TAX CR.:YES
YEARS OF LIFE-USEFUL:16 BOOK: 7 TAX: 7 AREA: 100. SQ. FT.

DIRECT LABOR TYPE	INPUT UNITS/HR	PERCENT EFFICIENCY
HOURLY OPERATOR	1020.	100.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.050	0.050	0.050
ENGR. SUPPORT	0.025	0.025	0.025
CLERICAL	0.0	0.0	0.0
QUALITY CONTROL	0.0	0.0	0.0
MAINTENANCE	0.0	0.0	0.0
MACH. ATTENDANT	0.100	0.100	0.100

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE	% PROCESSED
ELECTRICITY	0.	0.0	0.001000	AREA	100.0%
PHOSPHORUS OXYCHLORIDE	0.	0.0	0.012500	AREA	100.0%
NITROGEN	0.	0.0	0.000160	AREA	100.0%
OXYGEN	0.	0.0	0.000018	AREA	100.0%
BOATS,LINERS,ETC.	0.	0.0	0.007200	UNIT	100.0%

NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 18. POCl₃ deposition and diffusion input data sheet.

OXIDE IS REMOVED IN HF
 YIELD: 99.5% IN:SHEETS OUT:SHEETS
 SALVAGE VALUE: 0.0% OF \$ COST OF 7.8 CM (3") DIAMETER WAFER
 3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS			
INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME:ETCH STATION EFF.: 90.0% THRUPUT: 1000. SH/HR
 % PROCESSED:100.0 COST: 20000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL: 8 BOOK: 7 TAX: 7 AREA: 20. SQ. FT.

DIRECT LABOR TYPE	INPUT UNITS/HR	PERCENT EFFICIENCY
HOURLY OPERATOR	1250.	100.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.050	0.050	0.050
ENGR. SUPPORT	0.0	0.0	0.0
CLERICAL	0.0	0.0	0.0
QUALITY CONTROL	0.0	0.0	0.0
MAINTENANCE	0.025	0.025	0.025
MACH. ATTENDANT	0.100	0.100	0.100

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE	% PROCESSED
ELECTRICITY	0.	0.0	0.000064	UNIT	100.0%
HYDROFLUORIC ACID	0.	0.0	0.011000	UNIT	100.0%
WATER	0.	0.0	0.000400	UNIT	100.0%

NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 19. Glass removal input data sheet.

RIM IS ETCHED IN HF/HNO3 MIXTURE

ASSUMPTIONS:

1. SEE "SYSTEM "Z" WAFER CLEANING"
2. MATERIALS CONSUMED RISE LINEARLY WITH TOTAL AREA IF ENTIRE SURFACE IS ETCHED; WITH DIAMETER IF RIM ETCH.
3. EQUIPMENT AND FLOOR SPACE STEP FUNCTION OF VOLUME AND NOT AREA DEPENDENT.
4. LABOR COST DEPENDENT ONLY ON NO. OF PIECES, NOT AREA.
5. MATERIAL COST ASSUMES REMOVAL OF 1 MIL FROM ENTIRE SURFACE.
6. ACETIC ACID ADDED AS A STABILIZER FOR HF/HNO3 MIXTURE
7. 1/3 OPERATOR AND 1/5 MAINTENANCE MAN NEEDED FOR AUTOMATIC SYSTEM.

YIELD: 95.0% IN: SHEETS

OUT: SHEETS

SALVAGE VALUE: 0.0% OF \$ COST OF 7.8 CM (3") DIAMETER WAFER

3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS

INPUT UNITS	AREA (SQ. FT.)	INPUT UNITS	AREA (SQ. FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME: ETCH STATION EFF.: 90.0% THRUPT: 4800. SH/HR
 % PROCESSED: 100.0 COST: 26000. MAINT. \$/HR: 0.0 TAX CR.: YES
 YEARS OF LIFE-USEFUL: 8 BOOK: 7 TAX: 7 AREA: 20. SQ. FT.

NAME: CARTRIDGE STACKER EFF.: 80.0% THRUPT: 720. SH/HR
 % PROCESSED: 100.0 COST: 15000. MAINT. \$/HR: 0.0 TAX CR.: YES
 YEARS OF LIFE-USEFUL: 7 BOOK: 7 TAX: 7 AREA: 0. SQ. FT.

NAME: COIN STACKER EFF.: 80.0% THRUPT: 720. SH/HR
 % PROCESSED: 100.0 COST: 25000. MAINT. \$/HR: 0.0 TAX CR.: YES
 YEARS OF LIFE-USEFUL: 7 BOOK: 7 TAX: 7 AREA: 0. SQ. FT.

NAME: ALARM EQUIPMENT EFF.: 0.0% THRUPT: 0. FIXED
 % PROCESSED: 0.0 COST: 5000. MAINT. \$/HR: 0.0 TAX CR.: YES
 YEARS OF LIFE-USEFUL: 7 BOOK: 7 TAX: 7 AREA: 0. SQ. FT.

DIRECT LABOR TYPE	INPUT UNITS/HR	PERCENT EFFICIENCY
HOURLY OPERATOR	11368.	100.0% 85.0%
HOURLY OPERATOR	1728.	100.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.050	0.050	0.050
ENGR. SUPPORT	0.0	0.0	0.0
CLERICAL	0.0	0.0	0.0
QUALITY CONTROL	0.0	0.0	0.0
MAINTENANCE	0.600	0.600	0.600
MACH. ATTENDANT	0.100	0.100	0.100

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE	% PROCESSED
ELECTRICITY	0.	0.0	0.000026	UNIT	100.0%
HYDROFLUORIC ACID	0.	0.0	0.000700	UNIT	100.0%
NITRIC ACID	0.	0.0	0.004400	UNIT	100.0%
DI WATER	0.	0.0	0.000800	UNIT	100.0%
ACETIC ACID	0.	0.0	0.010100	UNIT	100.0%

NOTE: FOR VAR. \$ PART BASE - "UNIT"=PER INPUT UNIT; "AREA"=PER 100 SQ. CM.

Figure 20. Rim etch input data sheet.

AGGREGATE QUALITY CONTROL INSPECTION

ASSUMPTIONS:

1. QUALITY CONTROL SAMPLING
2. YIELD LOSSES INCLUDED WITH APPROPRIATE PROCESSES.
3. VISUAL WAFER INSPECTION & SHEET RESISTANCE TEST.

YIELD:100.0% IN:SHEETS

OUT:SHEETS

SALVAGE VALUE:\$ 0.0

3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS

INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME:VIEW SCOPE EFF.: 95.0% THRUPUT: 65. SH/HR
 % PROCESSED: 1.0 COST: 8000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL:10 BOOK: 7 TAX: 7 AREA: 8. SQ. FT.

NAME:4-POINT PROBE EFF.: 90.0% THRUPUT: 300. SH/HR
 % PROCESSED: 1.0 COST: 5000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL:10 BOOK: 7 TAX: 7 AREA: 8. SQ. FT.

NAME:REICHERT MICROSCOPE EFF.: 95.0% THRUPUT: 65. SH/HR
 % PROCESSED: 0.1 COST: 3000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL:10 BOOK: 7 TAX: 7 AREA: 8. SQ. FT.

DIRECT LABOR TYPE INPUT UNITS/HR PERCENT EFFICIENCY
 HOURLY INSPECTOR 30. 1.0% 85.0%

INDIRECT LABOR TYPE 1ST SHIFT RATIO 2ND SHIFT RATIO 3RD SHIFT RATIO
 ENGR. SUPPORT 0.100 0.100 0.100
 MAINTENANCE 0.025 0.025 0.025

MATERIAL/EXPENSE NAME PROD. LIMIT FIXED \$ PART VAR. \$ PART BASE % PROCESSED
 MISCELLANEOUS 0. 1000.00 0.0 UNIT 100.0%
 NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 21. Post-diffusion inspection input data sheet.

SCREEN PRINTING AND SINTERING CONDUCTIVE NETWORK-ONE SIDE
ASSUMPTIONS:

1. SILICON WAFER, 3" DIA.
 2. METALLIZATION 0.5 MIL THICK (12.5 MICRONS).
 3. METALLIZATION AREA COVERAGE: 100% BACK; 5% FACE.
 4. ELECTRICITY @ \$.025/KWH
 5. AUTOMATED EQUIPMENT (\$98.8K): PRINTER @ \$24.4K, LOADER @ \$10.7K;
DRYER-FURNACE @ \$45K; RELOADER @ \$14.7K; MAGAZINES/TRAYS @ \$4K
- YIELD: 98.0% IN: SHEETS OUT: SHEETS
SALVAGE VALUE: \$ 0.0
3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS

INPUT UNITS	AREA (SQ. FT.)	INPUT UNITS	AREA (SQ. FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME: AUTOMATED SYSTEM EFF.: 85.0% THRUPT: 1800. SH/HR
% PROCESSED: 120.0 COST: 98600. MAINT. \$/HR: 0.0 TAX CR.: YES
YEARS OF LIFE-USEFUL: 15 BOOK: 7 TAX: 7 AREA: 1600. SQ. FT.

DIRECT LABOR TYPE	INPUT UNITS/HR	PERCENT EFFICIENCY
HOURLY OPERATOR	7650.	120.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.125	0.125	0.125
ENGR. SUPPORT	0.025	0.013	0.013
CLERICAL	1.100	1.100	1.100
QUALITY CONTROL	1.500	1.500	1.500
MAINTENANCE	0.350	0.350	0.350

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE	% PROCESSED
ELECTRICITY	0.	0.0	0.001930 UNIT		100.0%
SCREENS	0.	0.0	0.001440 UNIT		100.0%
SQUEEGEES	0.	0.0	0.000152 UNIT		100.0%
SOLVENT	0.	0.0	0.000038 UNIT		100.0%
SUPPORT & TC	0.	0.0	0.000303 UNIT		100.0%

NOTE: FOR VAR. \$ PART BASE - "UNIT" = PER INPUT UNIT; "AREA" = PER 100 SQ. CM.

Figure 22. Thick-film metallizing: auto input data sheet.

SUBPROCESS USED:THICK FILM METALLIZING:AUTO
 SCREEN PRINTING AND SINTERING CONDUCTIVE NETWORK-FRONT
 ASSUMPTIONS:

1. SILICON WAFER, 3" DIA.
 2. AG METALLIZATION,5.0 MICRONS THICK.
 3. AG METALLIZATION AREA COVERAGE: 5% FACE.
 YIELD: 98.0% IN:SHEETS OUT:SHEETS
 SALVAGE VALUE:\$ 0.0
 3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS			
INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE %	PROCESSED
INK AG	0.	0.0	0.002710	UNIT	100.0%

NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 23. Thick Ag metal-front: auto input data sheet.

SUBPROCESS USED:THICK FILM METALLIZING:AUTO
 SCREEN PRINTING AND SINTERING CONDUCTIVE NETWORK-BACK
 ASSUMPTIONS:

1. SILICON WAFER, 3" DIA.
 2. AG METALLIZATION ,5.0 MICRONS THICK.
 3. AG METALLIZATION AREA COVERAGE: 33.3% BACK.
 YIELD: 98.0% IN:SHEETS OUT:SHEETS
 SALVAGE VALUE:\$ 0.120
 3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS			
INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE %	PROCESSED
INK AG	0.	0.0	0.018100	UNIT	100.0%

NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 24. Thick Ag metal-back: auto input data sheet.

SPIN-ON A/R COATING

ASSUMPTIONS:

1. MATERIALS CONSUMED RISE LINEARLY WITH SILICON AREA.
 2. LIQUID SPIN-ON SOURCE(TI02,SI02) AT \$2/OZ. 1 OZ. WILL COVER ONE SIDE OF 250, 3" WAFERS WITH 0.07 MICRONS
 3. SPINNER REQUIREMENTS SAME AS FOR LIQUID DIFFUSION SOURCE
 4. APPLIED AFTER FINAL METALLATION.
 5. OVEN BAKE REQUIRED AT 400 C. FOR 1/2 HR. IN AIR
- YIELD: 95.0% IN:SHEETS OUT:SHEETS
SALVAGE VALUE: 0.0% OF \$ COST OF 7.8 CM (3") DIAMETER WAFER
3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS

INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME:III SPINNER EFF.: 85.0% THRUPUT: 400. SH/HR
X PROCESSED:110.0 COST: 10000. MAINT. \$/HR: 0.0 TAX CR.:YES
YEARS OF LIFE-USEFUL:10 BOOK: 7 TAX: 7 AREA: 300. SQ. FT.

NAME:OVEN EFF.: 95.0% THRUPUT: 800. SH/HR
X PROCESSED:100.0 COST: 1000. MAINT. \$/HR: 0.0 TAX CR.:YES
YEARS OF LIFE-USEFUL: 7 BOOK: 7 TAX: 7 AREA: 100. SQ. FT.

DIRECT LABOR TYPE	INPUT UNITS/HR	PERCENT EFFICIENCY
HOURLY OPERATOR	680.	110.0% 85.0%
HOURLY OPERATOR	760.	100.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.100	0.100	0.100
ENGR. SUPPORT	0.016	0.016	0.016
CLERICAL	0.0	0.0	0.0
QUALITY CONTROL	0.0	0.0	0.0
MAINTENANCE	0.150	0.150	0.150

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE	X PROCESSED
ELECTRICITY	0.	0.0	0.000400	UNIT	110.0%
SPIN-ON A/R COATING	0.	0.0	0.008000	UNIT	110.0%

NOTE: FOR VAR. \$ PART BASE - "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 25. AR coating: spin-on input data sheet.

WAFER ELECTRICAL TEST

ASSUMPTIONS:

1. TEST FOR: OPEN CIRCUIT VOLTAGE; SHORT CIRCUIT CURRENT;
REVERSE BIAS LEAKAGE; FILL FACTOR.
 2. ONLY ELECTRICITY CONSUMED; LINEAR WITH NO. OF PIECES.
 3. EQUIPMENT, FLOOR SPACE RISE LINEARLY WITH # OF PIECES.
- YIELD: 80.0% IN: SHEETS OUT: SOLAR CELLS
 SALVAGE VALUE: 0.0% OF \$ COST OF 7.8 CM (3") DIAMETER WAFER
 3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS			
INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	0.	0.	0.
0.	0.	0.	0.

INVESTMENTS

NAME: TEST EQUIPMENT EFF.: 85.0% THRUPT: 500. SH/HR
 % PROCESSED: 100.0 COST: 50000. MAINT. 1/HR: 0.0 TAX CR.: YES
 YEARS OF LIFE-USEFUL: 10 BOOK: 7 TAX: 7 AREA: 200. SQ. FT.

DIRECT LABOR TYPE	INPUT UNITS/HR	PERCENT EFFICIENCY
HOURLY OPERATOR	1000.	100.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.100	0.100	0.100
ENGR. SUPPORT	0.100	0.100	0.100
CLERICAL	0.0	0.0	0.0
QUALITY CONTROL	0.0	0.0	0.0
MAINTENANCE	0.100	0.100	0.100

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE \$	% PROCESSED
ELECTRICITY	0.	0.0	0.000200	UNIT	100.0%

NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT; "AREA"=PER 100 SQ. CM.

Figure 26. Test input data sheet.

ARRAY FABRICATION:GAP WELDING(B)

ASSUMPTIONS:

1. ASSEMBLY SYSTEM THRUPUT 600 CELLS/HR X .95 EFF X .96 YIELD.
 2. NO REWORK DONE.
 3. PANEL:1/4 GLASS WITH CONFORMAL COATING
 4. PANEL LAYOUT: BASELINE SOLAR CELL MODULE B
- YIELD: 96.0% IN:SOLAR CELLS OUT:ARRAY MODULES
 SALVAGE VALUE:\$ 0.0
 3 SHIFT(S) UTILIZED

PRODUCTION AREA FLOOR SPACE REQUIREMENTS

INPUT UNITS	AREA(SQ.FT.)	INPUT UNITS	AREA(SQ.FT.)
0.	700.	0.	700.
0.	700.	0.	700.

INVESTMENTS

NAME:INTERCONNECT EQUIPMENT EFF.: 95.0% THRUPUT: 600. CELLS/HR
 % PROCESSED:100.0 COST: 104000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL: 7 BOOK: 7 TAX: 7 AREA: 250. SQ. FT.

NAME:PANEL ASSEMBLY EQUIPMENT EFF.: 95.0% THRUPUT: 600. CELLS/HR
 % PROCESSED:100.0 COST: 52000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL:10 BOOK: 7 TAX: 7 AREA: 350. SQ. FT.

NAME:FINAL ASSEMBLY EQUIPMENT EFF.: 95.0% THRUPUT: 600. CELLS/HR
 % PROCESSED:100.0 COST: 15000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL:10 BOOK: 7 TAX: 7 AREA: 500. SQ. FT.

NAME:TEST EQUIPMENT EFF.: 95.0% THRUPUT: 2400. CELLS/HR
 % PROCESSED:100.0 COST: 75000. MAINT. \$/HR: 0.0 TAX CR.:YES
 YEARS OF LIFE-USEFUL:13 BOOK: 7 TAX: 7 AREA: 120. SQ. FT.

DIRECT LABOR TYPE INPUT UNITS/HR PERCENT EFFICIENCY
 HOURLY OPERATOR 223. 100.0% 85.0%

INDIRECT LABOR TYPE	1ST SHIFT RATIO	2ND SHIFT RATIO	3RD SHIFT RATIO
SUPERVISORY	0.100	0.100	0.100
ENGR. SUPPORT	0.0	0.0	0.0
CLERICAL	0.050	0.050	0.050
QUALITY CONTROL	0.0	0.0	0.0
MAINTENANCE	0.334	0.334	0.334

MATERIAL/EXPENSE NAME	PROD. LIMIT	FIXED \$	PART VAR. \$	PART BASE	% PROCESSED
ELECTRICITY	0.	0.0	0.000271	UNIT	100.0%
ELECTRODES	0.	0.0	0.001430	UNIT	100.0%
AG-PLATED CU WIRE	0.	0.0	0.000714	UNIT	100.0%
NITROGEN	0.	0.0	0.002500	UNIT	100.0%
SUBSTRATE	0.	0.0	0.0	UNIT	100.0%
CELL ADHESIVE	0.	0.0	0.025300	UNIT	100.0%
WINDOW	0.	0.0	0.027100	UNIT	100.0%
CONFORMAL COAT+3MIL MET.	0.	0.0	0.006780	UNIT	100.0%
PANEL CONNECTOR	0.	0.0	0.006430	UNIT	100.0%
AL CHANNEL	0.	0.0	0.006630	UNIT	100.0%

NOTE: FOR VAR. \$ PART BASE- "UNIT"=PER INPUT UNIT;"AREA"=PER 100 SQ. CM.

Figure 27. Array fabrication: gap welding input data sheet.

SUMMARY: ALL PROCESSES			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
CONFORMAL COAT+3MIL MET.	MATERIAL	706250.	0.014
PANEL CONNECTOR	MATERIAL	669792.	0.013
AL CHANNEL	MATERIAL	690625.	0.014
INK AG	MATERIAL	2918190.	0.058
ELECTRODES	MATERIAL	148958.	0.003
AG-PLATED CU WIRE	MATERIAL	74375.	0.001
CELL ADHESIVE	MATERIAL	2635416.	0.053
WINDOW	MATERIAL	2822916.	0.056
ACETIC ACID	DIRECT EXP.	1517261.	0.030
BOATS, LINERS, ETC.	DIRECT EXP.	1098027.	0.022
DI WATER	DIRECT EXP.	178898.	0.004
ELECTRICITY	DIRECT EXP.	805376.	0.016
HYDROFLUORIC ACID	DIRECT EXP.	1765923.	0.035
HYDROGEN PEROXIDE	DIRECT EXP.	39146.	0.001
MISCELLANEOUS	DIRECT EXP.	1000.	0.000
NITRIC ACID	DIRECT EXP.	660985.	0.013
NITROGEN	DIRECT EXP.	272080.	0.005
OXYGEN	DIRECT EXP.	1312.	0.000
PHOSPHORUS OXYCHLORIDE	DIRECT EXP.	911210.	0.018
SCREENS	DIRECT EXP.	406903.	0.008
SOLVENT	DIRECT EXP.	10738.	0.000
SPIN-ON A/R COATING	DIRECT EXP.	1206140.	0.024
SPIN-ON SOURCE	DIRECT EXP.	426297.	0.009
SQUEEGEES	DIRECT EXP.	42951.	0.001
SULFURIC ACID	DIRECT EXP.	25836.	0.001
SUPPORT & TC	DIRECT EXP.	85619.	0.002
WATER	DIRECT EXP.	60392.	0.001
TOTAL	MATERIAL	10666522.	0.213
TOTAL	DIRECT EXP.	9516094.	0.190
GRAND TOTAL	ALL EXPENSES	20182608.	0.404

Figure 28. Material/expense summary.

PROCESS:SYSTEM "2" WAFER CLEANING			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	21922.	0.000
SULFURIC ACID	DIRECT EXP.	25836.	0.001
HYDROGEN PEROXIDE	DIRECT EXP.	39146.	0.001
DI WATER	DIRECT EXP.	58719.	0.001
TOTAL	DIRECT EXP.	145622.	0.003
GRAND TOTAL	ALL EXPENSES	145622.	0.003

PROCESS:SPIN-ON SOURCE			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	34104.	0.001
SPIN-ON SOURCE	DIRECT EXP.	426297.	0.009
TOTAL	DIRECT EXP.	460401.	0.009
GRAND TOTAL	ALL EXPENSES	460401.	0.009

PROCESS:200 DEG. C. BAKE			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	2945.	0.000

PROCESS:POCL3 DEPOSITION AND DIFFUSION			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	72897.	0.001
PHOSPHORUS OXYCHLORIDE	DIRECT EXP.	911210.	0.015
NITROGEN	DIRECT EXP.	11663.	0.000
OXYGEN	DIRECT EXP.	1312.	0.000
BOATS,LINERS,ETC.	DIRECT EXP.	1098027.	0.022
TOTAL	DIRECT EXP.	2095109.	0.042
GRAND TOTAL	ALL EXPENSES	2095109.	0.042

PROCESS:GLASS REMOVAL			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	9663.	0.000
HYDROFLUORIC ACID	DIRECT EXP.	1660767.	0.033
WATER	DIRECT EXP.	60392.	0.001
TOTAL	DIRECT EXP.	1730821.	0.035
GRAND TOTAL	ALL EXPENSES	1730821.	0.035

PROCESS:RIM ETCH			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	3906.	0.000
HYDROFLUORIC ACID	DIRECT EXP.	105157.	0.002
NITRIC ACID	DIRECT EXP.	660985.	0.013
DI WATER	DIRECT EXP.	120179.	0.002
ACETIC ACID	DIRECT EXP.	1517261.	0.030
TOTAL	DIRECT EXP.	2407488.	0.045
GRAND TOTAL	ALL EXPENSES	2407488.	0.045

PROCESS:POST DIFFUSION INSPECTION			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
MISCELLANEOUS	DIRECT EXP.	1000.	0.000

Figure 29. Material/expense for each process step.

PROCESS:THICK FILM METALLIZING:AUTO			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	545363.	0.011
SCREENS	DIRECT EXP.	406903.	0.008
SQUEEGEES	DIRECT EXP.	42951.	0.001
SOLVENT	DIRECT EXP.	10738.	0.000
SUPPORT & TC	DIRECT EXP.	85619.	0.002
TOTAL	DIRECT EXP.	1091573.	0.022
GRAND TOTAL	ALL EXPENSES	1091572.	0.022

PROCESS:THICK AG METAL-FRONT:AUTO			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
INK AG	MATERIAL	386752.	0.008

PROCESS:THICK AG METAL-BACK:AUTO			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
INK AG	MATERIAL	2531439.	0.051

PROCESS:ANTIREFLECTION COATING:SPIN-ON			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	60307.	0.001
SPIN-ON A/R COATING	DIRECT EXP.	1206140.	0.024
TOTAL	DIRECT EXP.	1266447.	0.025
GRAND TOTAL	ALL EXPENSES	1266447.	0.025

PROCESS:TEST			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	26042.	0.001

PROCESS:ARRAY FABRICATION:GAP WELDING(B)			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
ELECTRICITY	DIRECT EXP.	28229.	0.001
ELECTRODES	MATERIAL	148958.	0.003
AG-PLATED CU WIRE	MATERIAL	74375.	0.001
NITROGEN	DIRECT EXP.	260417.	0.005
CELL ADHESIVE	MATERIAL	2635416.	0.053
WINDOW	MATERIAL	2822916.	0.056
CONFORMAL COAT+3MIL MET.	MATERIAL	706250.	0.014
PANEL CONNECTOR	MATERIAL	669792.	0.013
AL CHANNEL	MATERIAL	690825.	0.014
TOTAL	MATERIAL	7748331.	0.155
TOTAL	DIRECT EXP.	288646.	0.006
GRAND TOTAL	ALL EXPENSES	8036976.	0.161

Figure 29. (Continued).

INVESTMENT SUMMARY

PROCESS:SYSTEM "2" WAFER CLEANING						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
6" HOOD	46	414000.	59143.	37260.	0.	98.X
\$/WATT		0.008	0.001	0.001	0.0	
PROCESS:SPIN-ON SOURCE						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
III SPINNER	90	900000.	128571.	81000.	0.	99.X
\$/WATT		0.018	0.003	0.002	0.0	
PROCESS:200 DEG. C. BAKE						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
200 DEG. C. OVEN	30	30000.	4286.	2700.	0.	97.X
MECHANICAL STACKER	30	60000.	8571.	5400.	0.	97.X
TOTALS		90000.	12857.	8100.	0.	
\$/WATT		0.002	0.000	0.000	0.0	
PROCESS:POCL3 DEPOSITION AND DIFFUSION						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
DIFFUSION FURNACE	102	3264000.	466286.	293760.	11961.	100.X
\$/WATT		0.065	0.009	0.006	0.000	
PROCESS:GLASS REMOVAL						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
ETCH STATION	29	580000.	82857.	52200.	0.	98.X
\$/WATT		0.012	0.002	0.001	0.0	
PROCESS:RIM ETCH						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
ETCH STATION	6	120000.	17143.	10800.	0.	99.X
CARTRIDGE STACKER	45	675000.	96429.	60750.	0.	99.X
COIN STACKER	45	1125000.	160714.	101250.	0.	99.X
ALARM EQUIPMENT	1	5000.	714.	450.	0.	0.X
TOTALS		1925000.	275000.	173250.	0.	
\$/WATT		0.038	0.005	0.003	0.0	
PROCESS:POST DIFFUSION INSPECTION						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
VIEW SCOPE	4	32000.	4571.	2880.	0.	98.X
4-POINT PROBE	1	5000.	714.	450.	0.	90.X
REICHERT MICROSCOPE	1	3000.	429.	270.	0.	39.X
TOTALS		40000.	5714.	3600.	0.	
\$/WATT		0.001	0.000	0.000	0.0	
PROCESS:THICK FILM METALLIZING:AUTO						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
AUTOMATED SYSTEM	38	3754400.	536343.	337896.	0.	99.X
\$/WATT		0.075	0.011	0.007	0.0	

Figure 30. Summary of investments.

INVESTMENT SUMMARY

PROCESS: ANTIREFLECTION COATING: SPIN-ON						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
III SPINNER	76	760000.	108571.	68400.	0.	99.X
OVEN	31	31000.	4429.	2790.	0.	99.X
TOTALS		791000.	113000.	71190.	0.	
\$/WATT		0.016	0.002	0.001	0.0	
PROCESS: TEST						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
TEST EQUIPMENT	53	2650000.	378571.	235500.	0.	98.X
\$/WATT		0.053	0.008	0.005	0.0	
PROCESS: ARRAY FABRICATION: GAP WELDING (B)						
INVESTMENT	UNITS	\$TOTAL	\$ DEPR.	\$ INTEREST	\$MAINT.	USAGE
INTERCONNECT EQUIPMENT	32	3328000.	475429.	299520.	0.	97.X
PANEL ASSEMBLY EQUIPMENT	32	1664000.	237714.	149760.	0.	97.X
FINAL ASSEMBLY EQUIPMENT	32	480000.	68571.	43200.	0.	97.X
TEST EQUIPMENT	8	600000.	85714.	54000.	0.	97.X
TOTALS		6072000.	867428.	546480.	0.	
\$/WATT		0.121	0.017	0.011	0.0	
GRAND TOTALS		20480400.	2925771.	1843235.	11961.	
\$/WATT		0.410	0.059	0.037	0.000	
TOTAL AREA:		179858. SQ. FT.				

Figure 30. (Continued).

Similarly, the labor summary of Fig. 31 identifies the yielded labor requirements of each step. The fractional persons/shift results from the program's adding people to satisfy the throughput requirements. Obviously these need to be integers.

PROCESS:SYSTEM "Z" WAFER CLEANING						
DIRECT LABOR TYPE		PERSONS/SHIFT		TOTAL \$ COST	LABOR O.H.	
HOURLY OPERATOR		43.7		1027700.	428209.	
		\$/W		0.021	0.009	
INDIRECT LABOR TYPE		PERSONS/SHIFT		TOTAL \$ COST	LABOR O.H.	
SUPERVISORY		2.2,	2.2,	2.2	85205.	35502.
ENGR. SUPPORT		1.1,	1.1,	1.1	55711.	23213.
MAINTENANCE		2.2,	2.2,	2.2	54400.	22667.
TOTALS		5.5,	5.5,	5.5	195315.	81381.
		\$/W		0.004	0.002	
PROCESS:SPIN-ON SOURCE						
DIRECT LABOR TYPE		PERSONS/SHIFT		TOTAL \$ COST	LABOR O.H.	
HOURLY OPERATOR		52.5		1234374.	514323.	
		\$/W		0.025	0.010	
INDIRECT LABOR TYPE		PERSONS/SHIFT		TOTAL \$ COST	LABOR O.H.	
SUPERVISORY		2.6,	2.6,	2.6	102340.	42642.
ENGR. SUPPORT		1.3,	1.3,	1.3	66914.	27881.
MAINTENANCE		7.9,	7.9,	7.9	196020.	81675.
TOTALS		11.8,	11.8,	11.8	365274.	152198.
		\$/W		0.007	0.003	
PROCESS:200 DEG. C. BAKE						
DIRECT LABOR TYPE		PERSONS/SHIFT		TOTAL \$ COST	LABOR O.H.	
HOURLY OPERATOR		34.2		805460.	335609.	
		\$/W		0.016	0.007	
INDIRECT LABOR TYPE		PERSONS/SHIFT		TOTAL \$ COST	LABOR O.H.	
SUPERVISORY		3.4,	3.4,	3.4	133558.	55649.
MAINTENANCE		3.4,	3.4,	3.4	85272.	35530.
TOTALS		6.8,	6.8,	6.8	218830.	91179.
		\$/W		0.004	0.002	
PROCESS:POCL3 DEPOSITION AND DIFFUSION						
DIRECT LABOR TYPE		PERSONS/SHIFT		TOTAL \$ COST	LABOR O.H.	
HOURLY OPERATOR		29.9		703593.	293164.	
		\$/W		0.014	0.006	
INDIRECT LABOR TYPE		PERSONS/SHIFT		TOTAL \$ COST	LABOR O.H.	
SUPERVISORY		1.5,	1.5,	1.5	58334.	24306.
ENGR. SUPPORT		0.7,	0.7,	0.7	38141.	15892.
MACH. ATTENDANT		3.0,	3.0,	3.0	84359.	35150.
TOTALS		5.2,	5.2,	5.2	180834.	75348.
		\$/W		0.004	0.002	

Figure 31. Labor summary for each process step.

PROCESS: GLASS REMOVAL					
DIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
HOURLY OPERATOR	24.2			568391.	236830.
	\$/W			0.011	0.005
INDIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
SUPERVISORY	1.2,	1.2,	1.2	47124.	19635.
MAINTENANCE	0.6,	0.6,	0.6	15043.	6268.
MACH. ATTENDANT	2.4,	2.4,	2.4	68149.	28395.
TOTALS	4.2,	4.2,	4.2	130317.	54299.
	\$/W			0.003	0.001

PROCESS: RIM ETCH					
DIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
HOURLY OPERATOR	2.6			62187.	25911.
HOURLY OPERATOR	17.4			409106.	170461.
TOTALS	20.0			471293.	196372.
	\$/W			0.009	0.004
INDIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
SUPERVISORY	1.0,	1.0,	1.0	39074.	16281.
MAINTENANCE	12.0,	12.0,	12.0	299367.	124736.
MACH. ATTENDANT	2.0,	2.0,	2.0	56507.	23545.
TOTALS	15.0,	15.0,	15.0	394948.	164562.
	\$/W			0.008	0.003

PROCESS: POST DIFFUSION INSPECTION					
DIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
HOURLY INSPECTOR	9.5			223863.	93276.
	\$/W			0.004	0.002
INDIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
ENGR. SUPPORT	1.0,	1.0,	1.0	48542.	20226.
MAINTENANCE	0.2,	0.2,	0.2	5925.	2469.
TOTALS	1.2,	1.2,	1.2	54467.	22694.
	\$/W			0.001	0.000

PROCESS: THICK FILM METALLIZING: AUTO					
DIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
HOURLY OPERATOR	8.9			208588.	86912.
	\$/W			0.004	0.002
INDIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
SUPERVISORY	1.1,	1.1,	1.1	43234.	18014.
ENGR. SUPPORT	0.2,	0.1,	0.1	7689.	3083.
CLERICAL	9.8,	9.8,	9.8	242909.	101212.
QUALITY CONTROL	13.3,	13.3,	13.3	331239.	138016.
MAINTENANCE	3.1,	3.1,	3.1	77289.	32204.
TOTALS	27.5,	27.4,	27.4	702360.	292530.
	\$/W			0.014	0.006

Figure 31. (Continued).

PROCESS:ANTIREFLECTION COATING:SPIN-ON					
DIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
HOURLY OPERATOR	44.4			1043374.	434739.
HOURLY OPERATOR	36.1			848677.	353616.
TOTALS	80.4			1892050.	788355.
	\$/W			0.038	0.016
INDIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
SUPERVISORY	8.0,	8.0,	8.0	313733.	130722.
ENGR. SUPPORT	1.3,	1.3,	1.3	65643.	27351.
MAINTENANCE	12.1,	12.1,	12.1	300459.	125191.
TOTALS	21.4,	21.4,	21.4	679835.	283265.
	\$/W			0.014	0.006

PROCESS:TEST					
DIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
HOURLY OPERATOR	26.1			612745.	255310.
	\$/W			0.012	0.005
INDIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
SUPERVISORY	2.6,	2.6,	2.6	101603.	42335.
ENGR. SUPPORT	2.6,	2.6,	2.6	132866.	55361.
MAINTENANCE	2.6,	2.6,	2.6	64870.	27029.
TOTALS	7.8,	7.8,	7.8	299338.	124724.
	\$/W			0.006	0.002

PROCESS:ARRAY FABRICATION:GAP WELDING(B)					
DIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
HOURLY OPERATOR	93.5			2198188.	915912.
	\$/W			0.044	0.018
INDIRECT LABOR TYPE	PERSONS/SHIFT			TOTAL \$ COST	LABOR O.H.
SUPERVISORY	9.3,	9.3,	9.3	364496.	151873.
CLERICAL	4.7,	4.7,	4.7	116358.	48483.
MAINTENANCE	31.2,	31.2,	31.2	777272.	323864.
TOTALS	45.2,	45.2,	45.2	1258126.	524219.
	\$/W			0.025	0.010
TOTAL:DIRECT				9946241.	4144266.
\$/WATT				0.199	0.083
TOTAL:INDIRECT				4479642.	1866397.
\$/WATT				0.090	0.037

Figure 31. (Continued).

In addition to the cost breakdown by cost type (Materials & Expense, Investments, Labor) there is also a "Cost Summary" for each step. These are summarized in Fig. 13, the "Process Cost Overview," and are not shown to save space.

4. Discussion

From the beginning of this program, our strategy has been to try to identify processes whose intrinsic material and expense costs are low. Automation of such processes is expected to result in the lowest final cost for the array module.

For the process defined in Fig. 13, the

Material and expense	= \$0.404/W.
Direct labor	= \$0.19/W
Process overhead	= \$0.21/W
Interest and depreciation	= \$0.09/W.

(Process overhead is not simply a multiple of the Direct Labor Content but is calculated for each process from the explicit input data in Figs. 15 through 27.)

It should be clear that to attain an overall array module manufacturing cost significantly below \$0.5/W, the cost of material and expense items must be further reduced.

Figure 28, the "Material/Expense Summary," for the entire sequence, provides some insight into the problem. \$0.15/W is due to panel materials themselves. The panel costs shown are from column I of Table 5. Alternative panel designs are discussed in that section of the report.

Further significant material/expense items are acids. Figure 32 is a process cost overview for a sequence which uses ion implantation as the junction formation step and for the back doping, thereby potentially eliminating the glass removal step and the rim etch associated with the POCl_3 diffusion step. The material/expense summary in Fig. 33 shows the effect. The material/expense cost has been reduced \$0.09/W to \$0.31/W. Full documentation, such as Figs. 14 through 31, is of course available for this sequence as well.

ASSUMPTIONS: 0.500 WATTS PER SOLAR CELL AND STEP YIELD PROCESS													0.0 FOR 7.6 CM (3") DIAMETER WAFER				
			AT*L.	D. L.	EXP.	P. OM.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	X INVEST	X				
1	99.0%	SYSTEM "Z" WAFER CLEANING	0.0	0.019	0.003	0.013	0.001	0.001	0.036	0.0	0.036	4.6	0.008	1.4			
2	99.0%	ION IMPLANTATION-FRONT	0.0	0.007	0.018	0.026	0.011	0.018	0.080	0.0	0.080	10.2	0.125	23.3			
3	99.0%	ION IMPLANTATION-BACK	0.0	0.007	0.017	0.025	0.011	0.018	0.079	0.0	0.079	10.1	0.124	23.0			
4	98.0%	DIFFUSION	0.0	0.013	0.006	0.012	0.001	0.002	0.034	0.0	0.034	4.4	0.016	2.9			
5	100.0%	POST DIFFUSION INSPECTION	0.0	0.004	0.000	0.003	0.000	0.000	0.008	0.0	0.008	1.0	0.001	0.1			
6	98.0%	THICK AG METAL-FRONT:AUTO	0.008	0.002	0.011	0.011	0.003	0.005	0.041	0.0	0.041	5.2	0.038	7.0			
7	98.0%	THICK AG METAL-BACK:AUTO	0.051	0.002	0.011	0.011	0.003	0.005	0.083	-0.007	0.076	9.7	0.037	6.9			
8	95.0%	ANTIREFLECTION COATING:SPIN-ON	0.0	0.038	0.025	0.035	0.001	0.002	0.102	0.0	0.102	13.0	0.016	2.9			
9	80.0%	TEST	0.0	0.012	0.001	0.014	0.005	0.008	0.039	0.0	0.039	5.0	0.053	9.8			
10	96.0%	ARRAY FABRICATION:GAP WELDING(B)	0.055	0.044	0.006	0.054	0.011	0.017	0.287	0.0	0.287	36.7	0.121	22.5			
	66.6%	TOTALS	0.213	0.149	0.097	0.204	0.048	0.077	0.789	-0.007	0.782	100.0	0.539	100.0			
			X	27.05	18.91	12.31	25.01	6.15	9.76	100.00							

Figure 32. Process cost overview for sequence with ion implantation.

SUMMARY: ALL PROCESSES			
ITEM NAME	TYPE	TOTAL \$	\$/WATT
AG-PLATED CU WIRE	MATERIAL	74375.	0.001
AL CHANNEL	MATERIAL	690625.	0.014
CELL ADHESIVE	MATERIAL	2635416.	0.053
CONFORMAL COAT+3MIL NET.	MATERIAL	706250.	0.014
ELECTRODES	MATERIAL	148958.	0.003
INK AG	MATERIAL	2918190.	0.058
PANEL CONNECTOR	MATERIAL	669792.	0.013
WINDOW	MATERIAL	2822916.	0.056
BOATS, LINERS, ETC.	DIRECT EXP.	198050.	0.004
DI WATER	DIRECT EXP.	53805.	0.001
ELECTRICITY	DIRECT EXP.	1570101.	0.031
FILAMENTS/INSULATORS	DIRECT EXP.	591356.	0.012
HYDROGEN PEROXIDE	DIRECT EXP.	35870.	0.001
LIQUID NITROGEN	DIRECT EXP.	295678.	0.006
MISCELLANEOUS	DIRECT EXP.	1000.	0.000
NITROGEN	DIRECT EXP.	272940.	0.005
SCREENS	DIRECT EXP.	406903.	0.008
SOLVENT	DIRECT EXP.	10738.	0.000
SPIN-ON A/R COATING	DIRECT EXP.	1206140.	0.024
SQUEEGEES	DIRECT EXP.	42951.	0.001
SULFURIC ACID	DIRECT EXP.	23674.	0.000
SUPPORT & TC	DIRECT EXP.	85619.	0.002
WATER	DIRECT EXP.	59136.	0.001
TOTAL	MATERIAL	10666522.	0.213
TOTAL	DIRECT EXP.	4853962.	0.097
GRAND TOTAL	ALL EXPENSES	15520484.	0.310

Figure 33. Material/expense summary for sequence with ion implantation.

The remainder of our program will be to complete the conceptual design of process steps which have the potential, from a materials/expense point of view, to reach an array module manufacturing cost substantially below \$0.50/W. Experimental verification, to the extent possible within the scope of this program, is being provided for uncommon processes.

SECTION IV

CONCLUSIONS

A review of the quality of the various possible forms of the starting silicon material leads to the conclusion that wafers from Czochralski-pulled ingots are the only form of silicon which will be available for automated array processing for the next several years.

A new calculational procedure has been developed and tested for the optimization of performance of both the front and back contact metallizations. For the front contact, all four principal sources of loss are included; appropriate constraints are imposed, arising from both general principles of contact design and the physical limitations of specific technologies; the optimum grid line spacing is found; and the total power output is evaluated. The chief technical uncertainty is found to be the metal-Si contact resistivity ρ_c and a general criterion can be stated that ρ_c must be $\lesssim 10^{-2}$ ohm-cm². If this condition is met, a number of cost-effective options for both front and back contacts appear to offer satisfactory performance.

The survey of present-day contact and interconnect metallization technology for silicon devices has been completed. The evaluation of the various processes has been treated from the viewpoints of technical applicability to silicon solar cells, manufacturing feasibility on a large scale (10^6 to 10^8 cells per year), production cost, and device reliability. Detailed cost analyses of selected processes have been conducted using computer techniques. From a quite thorough analysis, screen-printed Ag contacts appear the most cost effective.

A further analysis of panel material costs is presented, and glass panels of three configurations considered to be the best choices are described. A complete description of the cost analysis procedure for one particular solar array module manufacturing sequence is given. This sequence, using gas diffusion junction formation technology, screen-printed Ag contacts, spin-on AR coating, gap welding for interconnects, and a glass plate-conformal coating-metal foil moisture barrier panel, produces panels at a cost of \$0.9/W.

The basic materials costs of the process sequences developed and studied are beginning to approach interesting values. The lowest cost projected to date for material and expense items for array module manufacturing is \$0.31/W.

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APPENDIX A

MANHOUR AND COST SUMMARY

Manhour and cost summary charts are shown in Figs. A-1 and A-2, respectively.

Figure A-1. Manhour summary chart.

Figure A-2. Cost summary chart.

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