PHASE I OF THE AUTOMATED ARRAY ASSEMBLY TASK
OF THE LOW COST SILICON SOLAR ARRAY PROJECT

Technical Quarterly Report No. 3

M. Coleman

October 1976

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Semiconductor Group
Motorola, Incorporated
Phoenix, Arizona

MASTER
ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
Division of Solar Energy

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Motorola Report No. 2258/3

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October 1976

JPL CONTRACT NO. 954363

By

M. Coleman

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ABSTRACT

A matrix of possible process steps is presented. Each process is evaluated by suitability criteria and categorized with respect to future usefulness. From the processes which have a high probability of incorporation into a future manufacturing factory, a possible process sequence is chosen. Studies of detailed cost analysis and factory projections have been initiated. Reliability considerations are discussed for module interconnections and encapsulant materials.

TABLE OF CONTENTS

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
1.0	Summary Statement	4
2.0	Introduction	4
3.0	Technical Discussions	5
3.1	Processing Matrix Evaluation	5
3.1.1	Starting Condition of Silicon Surface	7
3.1.1.1	Sawed Surface (Category 1)	7
3.1.1.2	Sawed and Etched Surface (Category 4)	15
3.1.1.3	Lapped and/or Polished Surface (Category 1)	15
3.1.1.4	Cleaved Surface (Category 2)	16
3.1.1.5	As-Grown Sheet Surface (Category 2)	16
3.1.1.6	Texture-Etched Surface (Category 4)	17
3.1.2	In-Process Surface Cleaning or Etching	17
3.1.2.1	Wet Chemical Cleaning or Etching (Category 4)	18
3.1.2.2	Plasma Cleaning or Etching (Category 3)	18
3.1.2.3	Vacuum Baking and Reverse Sputtering (Category 1)	18
3.1.2.4	Texture-Etching (Category 1)	18
3.1.2.5	Brushing or Scrubbing (Category 4)	19
3.1.2.6	Gas Stream Drying (Category 4)	19
3.1.2.7	Gravity (Centrifuge) Drying (Category 4)	19
3.1.3	Lifetime Enhancement and Preservation (Category 3)	19
3.1.3.1	Literature Survey of Gettering	20
3.1.3.2	Gettering Bibliography	23
3.1.4	Junction Formation	25
3.1.4.1	Epitaxy (Category 1)	25

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
3.1.4.2	Diffusion (Category 4)	25
3.1.4.3	Ion Implantation (Category 4)	26
3.1.4.4	Alloy (Category 1)	26
3.1.5	Contact Metallization	27
3.1.5.1	Vacuum Deposition (Category 1)	27
3.1.5.2	Plating (Category 4)	28
3.1.5.3	Chemical Vapor Deposition (Category 1)	28
3.1.5.4	Printed (Silk Screened) (Category 4)	28
3.1.5.5	Lamination (Category 2)	29
3.1.5.6	Solder Coating (Category 4)	29
3.1.6	Antireflection (AR) Coating	29
3.1.6.1	Vacuum Deposition (Category 4)	29
3.1.6.2	Chemical Vapor Deposition (Category 4)	30
3.1.6.3	Direct Growth (SiO_2) (Category 1)	30
3.1.6.4	Plasma Deposition (Category 2)	30
3.1.6.5	Spin-On or Spray-On Deposition (Category 3)	30
3.1.7	Annealing	31
3.1.7.1	Resistance Furnace Heating (Category 4)	31
3.1.7.2	Direct Radiant Heating: High Temperatures (Category 2) Low Temperatures (Category 4)	31
3.1.7.3	Laser and Electron-Beam Heating (Category 3)	32
3.1.7.4	RF Heating (Category 1)	32
3.1.8	Patterning	32
3.1.8.1	Photolithography (Category 4)	32
3.1.8.2	Shadow Masking: Metallization (Category 1) Ion Implantation (Category 4)	33
3.1.9	Interconnection	33

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
3.1.9.1	Solder Reflow (Category 4)	33
3.1.9.2	Thermal Compression and Ultrasonic Lead Bonding (Category 1)	34
3.1.9.3	Welding (Category 3)	34
3.1.9.4	Filled Adhesives (Category 2)	34
3.1.9.5	Clamped Connectors (Category 1)	35
3.1.10	Category 4 Processes	35
3.2	Process Sequencing and Solar Cell Fabrication	36
3.3	Analysis of Processing Costs	37
3.4	Encapsulation Design	38
3.4.1	Moisture Resistant Metallization	39
3.4.2	Redundant and Parallel-Oriented Interconnection	39
3.4.3	Moisture Ingression Testing	40
3.4.4	Protective Coatings for Metal Encapsulant Parts	41
4.0	Conclusions	42
5.0	Recommendations	42
6.0	Current Problems	42
7.0	Work Plan Status	43
8.0	List of Action Items	43

1.0 SUMMARY STATEMENT

Studies on design improvement, process adaptation, process sequencing optimization, analysis of processing costs, solar cell fabrication, encapsulation design, and encapsulation have progressed during this quarter according to plan.

The processing matrix presented in Technical Quarterly Report No. 1 has been evaluated and is presented here. Processes with a high possibility of inclusion in a future manufacturing process sequence are identified and one possible process sequence has been chosen. A literature survey on gettering processes has been performed. Detailed cost analysis of individual processes has been initiated as well as a study of future factory requirements. Reliability considerations for cell and interconnect metallizations are discussed as well as redundant and parallel-oriented interconnection schemes. A corrosion resistant material coating for steel is also presented. An accelerated moisture ingress-ion test for modules is discussed.

2.0 INTRODUCTION

Phase I of the Automated Array Assembly Task, LCSSAP, is concerned with a comprehensive assessment of the improvements in existing technology that may be needed to develop, within a period of no more than 10 years, an industrial capability for low cost, mass production of very durable silicon solar photovoltaic modules and arrays.

This program incorporates solar cell design, process adaptation, process sequencing optimization, technology assessment, solar cell fabrication, encapsulation, and cost analysis in an interrelated way such that the final choice for particular solar cell automated process sequences will be realistic, and that any recommendations for specific additional studies to improve particular process steps will have an (estimated) high probability of success in a (promising) given process sequence.

3.1 PROCESSING MATRIX EVALUATION

A matrix of processing operations was presented in Technical Quarterly Report #1. In that report, processes were placed in four general categories of projected usefulness, based upon knowledge and information available at that time.

During the past six months, many of these processes have been evaluated, either directly in the laboratory or through indirect methods such as literature surveys, vendor contacts, and detailed discussions with process engineers in the Motorola manufacturing and research areas (for both discrete and integrated circuit products). Among the evaluation factors are:

- . Performance
- . Controllability
- . Amenability to automation
- . Cost
 - Labor
 - Material
 - Capital Equipment
- . State of readiness
- . Reliability considerations
- . Amenability of future sheet (ribbon) geometries

These criteria were applied to both the process itself and to the resulting solar cell. A poor rating in either case would result in an overall poor rating. Performance of surface lapping silicon, for example, is judged favorably as an isolated process step, but lapped silicon is rated poorly as a starting surface for solar cell performance. It must be understood that process steps do not stand on their merits as individuals, but

on their ability to contribute synergistically to a process sequence. Each step must, then, be evaluated first, by itself, and second, as a member of a process sequence.

Detailed cost studies have not been performed at this time on each of the processing steps in the matrix. Rather, cost evaluation is of a qualitative nature, reflecting only estimated and relative costs of competing processes. While qualitative, it is believed that most cost evaluations are accurate enough to make good judgements. The capital cost of a vacuum system for metal evaporation is obviously much greater than a metal plating hood, for example.

The only other criterion which may not be self-explanatory is that involving sheet geometries. This requires an evaluation of a process step's suitability for application to a sheet which may have both irregular shape and is non-planar in nature. The sheet may, for example, be a ribbon which varies in edge shape, has surface ripples, and is warped. Some processes are relatively insensitive to this while others become virtually useless. Such as-grown sheet is considered as having more severe geometrical problems than large area sliced sheets which may also be utilized and must be considered at this time.

Based upon recent experience and updated evaluations, a newly defined set of categories has been designated to reflect current evaluations of projected usefulness. The categories are as follows:

Category 1: Processes which are judged unlikely to be utilized in any recommended process sequence.

Category 2: Processes which appear to require a major technological advancement to ensure usefulness. Technology in these areas must be continually monitored to assess future applicability.

Category 3: Processes which appear potentially promising, but which have required evaluations or equipment not available during the time-frame of this contract. Additional efforts should be expended on these processes.

Category 4: Proven processes which have a high chance of successful incorporation into future process sequences.

The evaluations of each process step are summarized in Table I. Each criterion is rated for each process step by the following method:

H = High (best on all criteria except cost, where high is worst)

M = Moderate

L = Low

U = Unknown or insufficient data to make evaluation

Blank = Not meaningful evaluation

Many of the comments presented here have already been presented in earlier reports, but are reiterated for the sake of completeness.

3.1.1 STARTING CONDITION OF SILICON SURFACE

The starting condition of the silicon surface plays a critical role in subsequent processing steps and in cell efficiency.

3.1.1.1 SAWED SURFACE (CATEGORY 1)

It is unlikely that silicon will be utilized in the as-cut condition. Although this form of silicon is the cheapest available today, near-surface damage (and possible contamination from the saw blade and coolant) can badly degrade the crystal properties upon subsequent processing. Heating of the sawed surface can result in polygonization or recrystallization, converting

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	LABOR	MATERIAL	CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
1. Starting Material Surface										
a. Sawed	L	H	M	L	H	M	H	H	U	1
b. Sawed and etched	M	H	M	L	M	M	H	H	U	4
c. Lapped	L	H	M	M	M	H	H	H	U	1
d. Polished	M	H	M	H	H	H	H	H	U	1
e. Cleaned	U	U	U	U	L	U	L	U	U	2
f. As grown sheet	U	U	H	U	L	U	L	U	-	2
g. Texture-etched	H	H	H	L	L	L	H	H	H-U	4

H = High

M = Moderate

L = Low

U = Unknown or
insufficient data
to make evaluationBlank - Not meaningful
evaluation¹Qualitative or
preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	LABOR	MATERIAL	CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
2. In Process Cleaning or Etching										
a. Wet Chemical	H	H	H	L	M	M	H	H	H	4
b. Plasma	M	M	M	L	L	H	L	U	H	3
c. Vacuum Baking	M	H	L	M	L	H	H	H	L	1
d. Reverse Sputtering	H	M	L	M	L	H	M	H	L	1
e. Texture Etching	H	H	H	-	L	L	H	H	H	4
f. Brushing	H	H	H	L	L	M	H	H	U	4
g. Gas Stream Drying	H	H	H	L	L	L	H	H	H	4
h. Gravity (centrifuge) Drying	H	H	M	L	L	M	H	H	L	4

H = High
 M = Moderate
 L = Low
 U = Unknown or Insufficient data to make evaluation
 Blank - Not meaningful evaluation
¹Qualitative or preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	LABOR	COST ¹	MATERIAL	CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
3. Lifetime Enhancement & Preservation											
a. Complexing and Removal	M	M	M	M	M	M	M	M	U	U	3
b. Temperature - time profiling	M-U	H	H	L	L	L	H	H	U	U	3
c. Leaching	M-U	M	H	L	L	L	M	M	U	U	3
d. Precipitation (damage sites)	M-U	M	M	L	L	L	M	M	U	U	3
4. Junction Formation											
a. Epitaxy	M	L	M	M	M	M	H	M	M	M	1
b. Diffusion	M	H	M	M	M	M	M	H	H	H	4
c. Ion Implantation	H	H	H	M	L	L	H	M	H	H	4
d. Alloy	L	L	M	M	M	M	H	L	M	M	1

H = High

M = Moderate

L = Low

U = Unknown or insufficient data to make evaluation

Blank - Not meaningful evaluation

¹ Qualitative or preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	LABOR	COST ¹		STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
					MATERIAL	CAPITAL				
5. Metallization										
a. Vacuum	H	M	M	M	M	H	H	H	M	1
b. Plating	H	H	H	L	M	L	M	H	H	4
c. Chemical Vapor Deposition	L	M	M	M	H	M	L	U	M	1
d. Printed	M	H	H	L	M	M	L	U	M	4
e. Lamination	U	U	H	L	M	M	L	U	M	2
f. Solder Coating	H	H	H	L	L	M	H	H	H	4

H = High

M = Moderate

L = Low

U = Unknown or
insufficient data
to make evaluationBlank - not meaningful
evaluation¹Qualitative or
preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS

	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	LABOR	MATERIAL	CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
6. Antireflection Coating										
a. Vacuum Deposition	H	H	M	M	M	H	H	M	M	4
b. Chemical Vapor Deposition	H	H	M	L	M	M	H	H	H	4
c. Direct Growth (SiO_2)	L	H	H	L	L	M	H	H	H	1
d. Plasma Deposition	U	M	M	M	M	H	L	U	M	2
e. Spin-on or Spray-on Deposition	M	M	H	M	M	M	M	U	M	3

H = High

M = Moderate

L = Low

U = Unknown or
Insufficient data
to make evaluation

Blank - Not meaningful
evaluation

¹Qualitative or
preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	LABOR	COST		STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
7. Annealing Sources										
a. Resistance Furnace	H	H	H	L	L	M	H	H	H	4
b. Radiant	M	M	H	L	H	M	M	M	M	2/4
c. Laser	U	H	H	L	L	H	L	U	H	3
d. Electron Beam	U	H	M	M	L	H	L	U	U	3
e. RF	M	M	M	L	L	H	M	M	M	1
8. Patterning										
a. Photolithography	H	H	H	M	M	H	H	H	H	4
b. Metal Shadow Masking	M	M	M	M	H	M	H	H	M	1
c. Ion Implantation Shadow Masking	G	G	G	K	K	K	G	G	N	4

H = High

M = Medium

L = Low

U = Unknown or
Insufficient Data
to make evaluationBlank - Not meaningful
evaluation1 Qualitative or
preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	LABOR	COST ¹			STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
9. Interconnection											
a. Solder reflow	H	H	H	L	L	M	H	H	H	H	4
b. Thermal Compression Bonding	M	H	M	M	L	M	H	M	L	L	1
c. Ultrasonic	M	M	M	M	L	M	H	M	L	L	1
d. Welding	H	M	M	M	L	M	H	H	M	M	3
e. Filled Adhesives	M	H	H	L	H	M	L	U	M	M	2
f. Clamped Connections	M	M	L	M	M	M	L	U	L	L	1

H = High

M = Moderate

L = Low

U = Unknown or
insufficient data
to make evaluationBlank = Not meaningful
evaluation¹Qualitative or
preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

the area in which the p-n junction is to be formed into a polycrystalline region. Heating may also propagate surface damage far into the bulk, resulting in a heavily dislocated, low lifetime material. All of these factors can degrade efficiency in a severe, uncontrolled manner.

One possible exception to this conclusion exists, however. Severe surface damage may be utilized to getter undesirable impurities from the bulk silicon below. High temperature annealing of a sawed surface may produce this desirable result. Subsequent to annealing, an undamaged silicon surface could be revealed by etching the sawed surface, hopefully removing both the damage and the impurities. There is at this time insufficient information available to draw useful conclusions; additional studies should be undertaken.

3.1.1.2 SAWED AND ETCHED SURFACE (CATEGORY 4)

This is the best candidate broadly available today. Etching is utilized to remove the sawing damage and contamination. Etching wafers can leave surfaces that contain only gradual undulations of a magnitude so small that no pattern having linewidths of interest to solar cell production should experience any masking difficulties because of surface non-planarity. Thus, apart from the future realization of direct sheet growth, this combination produces the cheapest material suitable for solar cells and has indeed been used to manufacture solar cells. Sawing kerf and material removed by etching are major drawbacks, however.

3.1.1.3 LAPPED AND/OR POLISHED SURFACE (CATEGORY 1)

Lapping produces a matte appearing surface on a silicon wafer. It will be a flat surface, and, if done carefully, both sides of a wafer can be made plane and parallel by lapping them both. Lapping doesn't necessarily produce

a surface having less damage than careful sawing, but a sawed surface will not be as flat as a lapped surface. This process is slow, batch orientated, and labor intensive, and hence, is too expensive for ultimate solar cell use.

Polishing is a process like lapping in which successively finer grit media are used to end up with a mirror-flat scratch-free surface. This degree of smoothness is necessary in order to obtain, by photographic means, the very fine line geometries utilized on many semiconductor devices and integrated circuits. However, solar cell geometries are about an order of magnitude coarser, so polished surfaces are not required for solar cell processing even where patterning is done photographically. Furthermore, polished surfaces typically contain more mechanical crystal damage than etched surfaces, making them potentially less satisfactory for solar cell use.

Both lapping and polishing are too costly for incorporation into a process sequence to make inexpensive solar cells.

3.1.1.4 CLEAVED SURFACE (CATEGORY 2)

Direct cleaving of silicon wafers or sheets from crystals would eliminate kerf losses and could produce smooth surfaces. To date, however, no process has been developed for cleaving wafers from a boule with anything approaching a satisfactory yield. If a major breakthrough in this area could be realized, it would be very cost competitive. No work appears to be currently underway in this area, however.

3.1.1.5 AS-GROWN SHEET SURFACE (CATEGORY 2)

This is the responsibility of several contractors in LSSA Task.II. Breakthroughs in technology are still required to make as-grown sheet practical in the large scale necessary. However, judging by the progress made to date

and the potentialities of the process, it must be assumed that the probability of success is high. The various processes being studied all have the possibility of providing as-grown surfaces suitable for efficient solar cell processing. Also, since the as-grown sheet processes have the inherent possibility of providing silicon with little or no waste, they must be considered as prime contenders for the ultimate source of silicon solar cell substrates.

3.1.1.6 TEXTURE-ETCHED SURFACE (CATEGORY 4)

Texture-etching has been shown to be a repeatable and uniform process on (100) oriented silicon surfaces. Texture-etching can be performed on any of the previously discussed silicon surface conditions. Costs of texture-etching are equal to or less than other silicon etching, producing silicon costs only marginally above those of present sawed and etched wafers. For this cost, a surface with distinct optical advantages and attendant efficiency increases is produced. The textured surface is dramatically different in nature from polished or etched surfaces now used widely in the semiconductor industry. This requires certain modifications of other processes in a process sequence utilizing textured surfaces. These modifications are easily achieved.

The main caveat which must be kept in mind is that texture-etched surfaces currently require (100) oriented surfaces. If future sheet processes cannot produce (100) surfaces, texture-etching will become unimportant. If, in the future, a choice must be made between two sheet growth processes of otherwise similar properties, the advantage will lie with the sheet process which can be texture-etched.

3.1.2 IN-PROCESS SURFACE CLEANING OR ETCHING

Any solar cell manufacturing process will require cleaning steps at some stages. Further, most manufacturing sequences will require etching steps.

3.1.2.1 WET CHEMICAL CLEANING OR ETCHING (CATEGORY 4)

Processes in this category are widely utilized in the semiconductor industry with a high degree of success. Only one major concern exists: unwanted contamination from wet chemicals. For any given process sequence and for each different manufacturing area, control limits will have to be defined for possible contaminants. At this time, no difficulties are seen in this area.

3.1.2.2 PLASMA CLEANING OR ETCHING (CATEGORY 3)

This is a dry process incorporating an RF field to excite a plasma. The energetic plasma is then used to remove material from the surface, either by bombardment of inert energetic plasma ions or by ions liberated from molecules injected into the plasma. Plasma processing technology and equipment have been available for several years, but only limited acceptance has been granted by the semiconductor industry until quite recently. While informal reports show a high future promise, direct evaluation has not yet been possible under this contract.

3.1.2.3 VACUUM BAKING AND REVERSE SPUTTERING (CATEGORY 1)

While results are reportedly adequate, the capital costs are prohibitive for further consideration.

3.1.2.4 TEXTURE-ETCHING (CATEGORY 4)

Rather than texture-etching as a pre-processing step, it can be incorporated within a process sequence. The previous discussion is applicable here.

3.1.2.5 BRUSHING OR SCRUBBING (CATEGORY 4)

As reported in Technical Quarterly Report No. 2, this process has been determined as technically acceptable. The effect on thin, irregular sheet geometries is unknown, however.

3.1.2.6 GAS STREAM DRYING (CATEGORY 4)

Wet chemistry steps require a subsequent drying operation. Drying by a gas flow has been one of the standards in the industry. It is forgiving of shape and is the prime contender for sheet geometries.

3.1.2.7 GRAVITY (CENTRIFUGE) DRYING (CATEGORY 4)

For round wafers, centrifuge or "spin" drying has become another of the semiconductor industry standards. In that industry, wafers are thicker and smaller than those likely to be utilized for future solar cells. This technique may require special adaptation for very large area, thin solar cell substrates such as long ribbons.

3.1.3 LIFETIME ENHANCEMENT AND PRESERVATION (CATEGORY 3)

Solar cell processing may require minority carrier lifetime improvement of the starting material, and must incorporate special precautions (and possibly specific techniques) to preserve lifetime during processing. Such processes fall into four general categories of lifetime enhancement: Complexing and removal of impurities, temperature-time profiling, leaching, and precipitation of impurities on damage sites or defects.

A literature survey on gettering of impurities in silicon has been performed. The initial observations to be made are that a variety of gettering

processes are available and that the area of impurity gettering is complex and not developed to its full potential. In short, these processes all fall precisely within the definition of Category 3. A brief review of the technique is given here, followed by a bibliography of gettering references.

3.1.3.1 LITERATURE SURVEY OF GETTERING

In the original investigations¹ into the removal of metallic impurities from silicon, the basic approach was to grow or deposit some type of oxide layer onto the surface of the silicon. The basic idea was that at high temperatures, the metallic impurities would diffuse to the surface and become trapped in the oxide layer. Various oxides were used including phosphorus -, boron -, vanadium -, and lead - silicon oxides. It was found that phosphorus glass did the best job.

Since then, studies^{3,10,13} have shown that the metallic impurities are not gettered into the phosphorus glass, but instead are gettered to the heavily doped silicon under the glass. Apparently, the mechanism is one of increased solubility of the metallic impurities in the phosphorus-doped silicon. Removal of impurities from the silicon, thus, requires removal of not only the oxide layer, but the surface layer of silicon itself.

Normally, in bipolar processing, phosphorus gettering is used to getter metallic impurities away from the active devices to an unused portion of the wafer (i.e., the isolation diffusion or the back of the wafer). In MOS processing, a phosphorus glass is deposited on top of the passivation oxide to getter sodium impurities from the gate oxide¹¹. However, this glass appears to do little gettering of metallic impurities from the bulk of the silicon.

It has also been shown that a preoxidation gettering of the backside of the wafer will reduce the generation of oxide-induced stacking faults¹⁴ (OISF). It is believed that OISF act to precipitate metallic impurities and thus degrade device characteristics. It is also believed that OISF are sites of enhanced phosphorus diffusion, and thus cause emitter-collector piping defects in bipolar devices.

It has been found that the use of various chlorine compounds during oxidation will getter both metallic impurities from the bulk silicon^{4,7,8} and sodium impurities from the oxides that are grown^{5,6,9,12}. Chlorine gettering can be used only during oxidation because it could otherwise cause extreme etching and pitting of the silicon⁴. Chlorine gas has been used with some success, but may cause etching of the silicon. Hydrogen chloride has been the most successful gettering compound.

The mechanism is believed to be the diffusion of metallic impurities to the surface, followed by formation of volatile metallic chlorides at the surface which are then carried away by the gas flow. The gettering effect improves with increasing temperature (especially above 1000°C) and increasing amounts of HCl. The limit to the amount of HCl used occurs when significant etching of the silicon begins along with condensation of hydrochloric acid droplets in the cooler portions of the furnace tube. Thus, the optimum mixture of HCl is about 5-10% HCL by volume in dry O₂.

It has also been discovered that the use of HCl will clean the furnace tube of metallic impurities, and thus reduce contamination from that source to virtually nil⁶. The process used is 10% HCl in dry oxygen 1150°C for 6 hours.

It should be noted that the use of HCl with steam instead of dry O₂ will still getter Na from the oxides thus grown, but will not as effectively getter the metallic impurities from the bulk. It is believed that the

accelerated oxidation of metallic impurities in steam inhibits the formation of volatile metal chlorides.

It is well known that various types of crystallographic defects in silicon will tend to precipitate metallic impurities. This principle has been used to getter impurities by deliberately introducing defects in the back of the wafer and thus removing the metallic impurities from the active device regions. It should be emphasized that this method does not remove the metallic impurities from the wafer, but merely moves them around. Methods of introducing defects include mechanical abrasion and ion implantation of Ar, O, P, Si, As, or B. As was suggested earlier, sawing damage may also be an appropriate starting point.

Boron diffusions have been used to getter metallic impurities from silicon, but are not as effective as phosphorus³. The mechanism is apparently the formation of metal precipitates, rather than any increased solubility or pairing.

Some gettering action has also been observed with the use of a Si_3N_4 layer¹⁸. Gettering can also be achieved through the appropriate use of controlled heating and cooling rates, and the temperature range of controlled heating and cooling. These cycles apparently function through a precipitation process, removing impurities from electrically active sites.

Since solar cell efficiency is extremely dependent upon lifetime, gettering cycles to improve or preserve lifetime seem appropriate for future incorporation into solar cell process sequences. The exact choice (or choices) will require further experimental work, however.

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3.1.4 JUNCTION FORMATION

The most complex and critical steps in solar cell processing involve junction formation. In order to stay within the design requirements of an efficient solar cell, the junction depth must be controlled to be consistently in the vicinity of 0.2 micrometers.

3.1.4.1 EPITAXY (CATEGORY 1)

Motorola has long and continuing experience in an automated silicon epitaxial line. Silicon deposition is accomplished in RF-heated, cold-walled chambers by chemical vapor deposition at temperatures near 1100°C. Present and projected state-of-the-art has shown accurately controlled deposition of silicon at thicknesses at or below 0.25 micrometers to be impractical. Thickness is difficult to control. Interdiffusion of impurities is high at deposition temperatures, resulting in further control difficulties and degrading performance. Projected yields and resulting costs make this method unlikely.

The only foreseen possibility is a low temperature plasma-aided or vacuum-aided deposition. At this time, these processes are considered speculative.

3.1.4.2 DIFFUSION (CATEGORY 4)

Diffusion is a generic term utilized to describe a broad variety of doping techniques. Diffusion is normally accomplished by a source deposition and a high temperature redistribution, either sequentially or simultaneously. All diffusion processes have the feature of rather isotropic diffusion of dopant into exposed surfaces, with first order junction depth control being accomplished by time and temperature. Control of surface concentration is commonly obtained by utilizing solid solubility of an impurity in silicon to

establish a controlled impurity source in the silicon, and then, with the external source removed, diffusing further from the "constant quantity" source in the silicon surface region. Depositions of source by CVD and by vapor transport have been successfully performed to make high efficiency solar cells. Spin-on sources appear potentially viable, but direct experimental data on solar cell structures is currently lacking.

3.1.4.3 ION IMPLANTATION (CATEGORY 4)

Ion implantation of the dopant, unlike diffusion, is not isotropic, but is unidirectional, with depth dependent upon implantation energy. Ion implantation can be performed with extremely pure, mass analyzed dopants, avoiding any undesired contamination. Surface concentration can be controlled by ion dose. The main drawback to ion implantation is the high capital cost. For solar cell applications, throughput is dependent primarily on ion beam current. Machine technology has progressed to the point of producing sufficiently high dopant ion beam currents to be a serious contender for solar cell processing. Still greater beam currents appear feasible; this could help meet the longer range LSSA Project cost goals.

3.1.4.4 ALLOY (CATEGORY 1)

This original technique for P-N junction formation was largely discarded by the industry due to lack of control and its intractability for anything but simple patterning. For solar cell use, the alloying material would have to be removed, exposing the (liquid phase epitaxy) regrown region below. Since the surface region is grown from solution, its impurity profile may not be controlled as desired to produce a drift aiding field. There appears to be no new development on the horizon to create renewed interest in alloying for solar cell P-N junction formation.

3.1.5 CONTACT METALLIZATION

Metallization is the interface between the silicon and the module and, as such, determines both module performance and module reliability. On one hand, solar cell contact metallization must cover the minimum possible area while achieving minimum resistance. On the other hand, the metallization must provide excellent mechanical adherence to the cell in environments which contain moisture and mechanical stresses. The technique of placing metal on the silicon surface and the metallization system must face these criteria as well as those already stated.

3.1.5.1 VACUUM DEPOSITION (CATEGORY 1)

Vacuum deposition is the predominant metallization method utilized in the semiconductor industry. A metal (or layers of metals) for most semiconductor devices and integrated circuits is deposited by evaporation or sputtering onto the entire wafer surface and subsequently patterned into small geometries in a photolithography (photoresist) step. Solar cell metallization, on the other hand, employs a large geometry pattern with coarse lines (by comparison). Some patterns can be made amenable to evaporation through a mask, thus eliminating the photoresist step. Totally redundant multiple contacts cannot however, be patterned through a metal mask if all metallization lines are to be directly interconnected on the cell surface. (Portions of the masking pattern would be unsupported and would fall out.) Both evaporation through a mask and photolithographic removal are very wasteful of material and provide high material costs, typically utilizing no more than 5% of the metal consumed. Further, both processes utilize further chemicals, for etching the excess metal, either from the wafer or the mask. The capital cost of the vacuum equipment is the highest of possible metal deposition techniques. It is not believed to be a viable contender for future application.

3.1.5.2 PLATING (CATEGORY 4)

Plated contacts which satisfy all criteria have been produced in the Motorola Solar Energy Department Laboratory. Based upon this direct information, plating is considered to have the highest probability of future usage of all metal processes. Plated contacts are amenable to automation. Costs for materials are moderate, but labor and capital costs are low. Above all, plating is the most forgiving process of all metal processes to surface and geometrical irregularities.

3.1.5.3 CHEMICAL VAPOR DEPOSITION (CATEGORY 1)

Chemical vapor deposition of metal contacts requires the decomposition of a metal-bearing gaseous compound. Primary candidates are all metal-organic compounds, which are generally highly expensive. It is doubtful that cost savings over established vacuum technology can be realized. Metallization by means of chemical vapor deposition will be considered only via an evolution of potentially useful new systems and raw materials costs.

3.1.5.4 PRINTED (SILK SCREENED) (CATEGORY 4)

A metallization capable of being painted directly onto the solar cell surface could be the long term cheapest metallization technique. Printed or silk screened contacts appear to have high potential but still may not be competitive with plated contacts. While no formal reports have been presented, present printed contacts are assumed to have adhesion problems. Additionally, printed contacts require that a carrier or binding material be used. Following printing, contacts from printing must be "fired" or heat treated to promote electrical contact and physical adhesion. The binder must then be removed or must be inert with respect to the silicon so that junction quality is preserved. Printing may be difficult on warped and rippled sheet surfaces.

In spite of these present difficulties, it is assumed that viable systems are forthcoming and this technique must be kept with high priority.

3.1.5.5 LAMINATION (CATEGORY 2)

The attachment of pre-shaped metallization patterns by lamination is also potentially attractive. Further developments are necessary before it can be considered viable. Potential problems are similar to those facing paint-on metallization. No lamination research is currently believed to be underway.

3.1.5.6 SOLDER COATING (CATEGORY 4)

In many cases, solar cell metallization systems will be composed of a base metal system for electrical and mechanical contact to the silicon surface, and a solder coating which will be thick enough to act as the primary current-carrying metal. Sophistication of processing already exists in the solder coating areas, and little development work is required provided that the surface of the underlying metallization is amenable to controllable solder coating.

3.1.6 ANTIREFLECTION (AR) COATING

A necessity for achieving the maximum efficiency from a solar cell is a high quality antireflection coating system. In some cases, this antireflection coating can be used for P-N junction passivation.

3.1.6.1 VACUUM DEPOSITION (CATEGORY 4)

The same basic comments made for metal vacuum deposition apply here, except that it is seldom required to pattern the AR film since it is generally applied after metallization (a mask may be used to prevent AR film deposition on the bonding pad areas). Film thickness control is critical.

While suitable technology is now available, other methods appear to be cost preferable. On the other hand, it is the best current method for some materials.

3.1.6.2 CHEMICAL VAPOR DEPOSITION (CATEGORY 4)

Chemical vapor deposition of silicon nitride has been performed in Motorola's laboratories. Silicon nitride is highly compatible with silicon and solar cell processing, forming excellent P-N junction passivation. The index of refraction of Si_3N_4 is less than ideal ($n \approx 2.0$) for plane surfaces but has provided near 1% total reflection from a coated textured surface. The material and equipment costs are considerably less than other contenders.

3.1.6.3 DIRECT GROWTH (SiO_2) (CATEGORY 1)

The index of refraction is essentially equal to all of the proposed encapsulant materials, making purposeful growth of SiO_2 as an AR coating unnecessary unless bare cells are utilized. If it forms a better surface material for encapsulant bonding it may be reconsidered, but this event is considered unlikely.

3.1.6.4 PLASMA DEPOSITION (CATEGORY 2)

Deposition of antireflection dielectric coatings can be performed by plasma-aided CVD reactions at much lower temperatures than are possible by thermally activated CVD. This area needs technological advancement prior to serious consideration for the LSSA Project.

3.1.6.5 SPIN-ON OR SPRAY-ON DEPOSITION (CATEGORY 3)

Antireflection coating compounds can be applied in the same manner as photoresist, followed by a bake cycle to either complete chemical reactions

and/or to drive off solvents. This technology merits serious consideration at this time, but adequate compounds and equipment have not been sought at this time.

3.1.7 ANNEALING

All solar cell manufacturing process sequences require some high temperature annealing.

3.1.7.1 RESISTANCE FURNACE HEATING (CATEGORY 4)

This is the almost universal semiconductor industry tool. The major problem in operation is energy consumption. In a continuous, automated environment, however, the energy dissipation per unit area of silicon should be capable of appreciable reduction from current practices. Uniformity and control exist now, even for large area sheets, and the technology is proven.

3.1.7.2 DIRECT RADIANT HEATING:

HIGH TEMPERATURES (CATEGORY 2)

LOW TEMPERATURES (CATEGORY 4)

This technique has had only limited application in semiconductor technology for high temperatures and has several inherent problems. The life of high intensity radiant sources is short, and output is somewhat variable during that lifetime. Uniformity of heating requires reflective surfaces which can also degrade with use. When used for high temperature (where radiant energy absorption is good) heating of silicon, direct radiant heating of large areas to a specific temperature is hard to control. Major technological advances are required for high temperature applications.

Low temperature applications, such as for solder reflow or photoresist baking, on the other hand, are well developed and are considered viable at this time.

3.1.7.3 LASER AND ELECTRON-BEAM HEATING (CATEGORY 3)

These emerging technologies show promise of excellent control and good efficiency. Application to semiconductor technology has been, however, limited, and requires further study before conclusions can be drawn. E-Beam heating is being explored by another contractor under LSSA Task IV.

3.1.7.4 RF HEATING (CATEGORY 1)

RF heating is broadly used in silicon epitaxy, since high temperatures can be achieved in a "cold-wall" (and thus noncontaminating) system. Heating of the silicon is indirect, however, in that a conducting susceptor is first heated by the RF field; this susceptor, in turn, conductively heats the silicon. This process is energy inefficient. A cold-wall system is not considered necessary for solar cell processing.

3.1.8 PATTERNING

Metallization, antireflection coatings, and dielectric layers for diffusion masks may require patterning in any given solar cell fabrication process.

3.1.8.1 PHOTOLITHOGRAPHY (CATEGORY 4)

Photolithography can be accomplished by either contact printing (direct mask contact to the silicon) or by projection or proximity (out-of-contact) masking techniques. Both proximity and projection require sophisticated optics, but can give nearly infinite mask life and well defined patterns on irregular surfaces. Both are far preferable, thus, to contact printing. In any case, mask alignment to the silicon substrate should be primarily mechanical, as

opposed to optical, and realignments should be avoided if possible because they tend to be expensive. Exposure will continue to be by ultraviolet or visible light unless some technological breakthrough occurs in either laser, E-beam, or X-ray exposure. Application is expected to be limited to dielectric patterning.

3.1.8.2 SHADOW MASKING:

METALLIZATION (CATEGORY 1)

ION IMPLANTATION (CATEGORY 4)

This technique is too wasteful of material to be utilized for metallization of solar cells. On the other hand, planar P-N junctions can be formed by shadow masking during ion implantation with excellent results and low cost. If planar junctions are utilized with ion implantation, masking will definitely be done by this technique.

3.1.9 INTERCONNECTION

Interconnections of solar cells into modules pose some stringent requirements for performance and reliability. The interconnection scheme must not contribute a substantial series resistance, or potential performance of the cells can be seriously degraded. Experience derived from the semiconductor industry would suggest that metallurgical interactions are the most likely failure mechanisms. These can lead to reduced output, for example, as a result of increased series resistance, or interference with the optical path, or, perhaps more commonly, opened circuit connections.

3.1.9.1 SOLDER REFLOW (CATEGORY 4)

The most widely used and probably the most cost effective solar cell interconnection scheme utilizes solder reflow. The technology is ready and has proven reliability.

3.1.9.2 THERMAL COMPRESSION AND ULTRASONIC LEAD BONDING (CATEGORY 1)

Though widely used in the semiconductor industry, thermal compression bonding is useful mainly on small diameter (less than about 100 μ m) wires where compression deformation requires low pressures compared to the fracture strength of silicon. Where millimeter sized bonds are required, this process is expected to be too damaging to the substrate to warrant further consideration.

Ultrasonic bonding is a low pressure process which utilizes ultrasonic energy to smear metal surfaces together, thereby establishing intimate contact for a metallurgical bond. It is not area limited, as is thermal compression bonding, but can damage substrates. It is an unlikely future choice.

3.1.9.3 WELDING (CATEGORY 3)

Welded contacts are potentially as viable as those made by solder reflow. Welding, however, requires higher temperatures than soldering and can result in damage to the solar cell. Further detailed study is required before recommendation for future use can be made.

3.1.9.4 FILLED ADHESIVES (CATEGORY 2)

Metallic filled adhesives for bonding wires to solar cell metallizations have had little or no application. Filled adhesives are used in the semiconductor industry for relatively large area bonding (e.g., die attach). These materials have poorer electrical conductivities than metals, and the better ones (e.g., gold filled) are expensive. In a solar panel, where thermally or mechanically induced tensile stresses on the interconnect wires may be expected, the reliability of filled adhesive bonds is questionable. However, this field is continually changing, and should continue to be monitored.

3.1.9.5 CLAMPED CONNECTORS (CATEGORY 1)

A direct clamping to the cell metallization is possible, especially if metal smearing at the contacts can be achieved without damage to the cell itself and pressure can be maintained in the package. Without such smearing, moisture ingress to the contacts would increase resistance and reduce module reliability. Tooling would be expected to be complex to provide smearing without fracturing cells, with little assurance of control or reliability. This process is deemed unlikely to succeed.

3.1.10 CATEGORY 4 PROCESSES

The processes which at this time appear to have a very high probability of incorporation into a future production process are tabulated here as a separate group.

1. Starting Condition
 - a. Sawed and Etched Surfaces
 - b. Texture-Etched Surfaces
2. In-Process Surface Cleaning or Etching
 - a. Wet Chemical
 - b. Texture-Etching
 - c. Scrubbing
 - d. Gas Stream Drying
 - e. Gravity (Centrifuge) Drying
3. Junction Formation
 - a. Ion Implantation
 - b. Diffusion
4. Metallization
 - a. Plating
 - b. Printing
 - c. Solder coating

5. Antireflection Coating
 - a. Vacuum Deposition
 - b. Chemical Vapor Deposition
6. Annealing
 - a. Resistance Furnace Heating
 - b. Low Temperature Radiant Heating
7. Patterning
 - a. Proximity Photolithography
 - b. Projection Photolithography
 - c. Ion Implantation Shadow Masking
8. Interconnection
 - a. Solder Reflow

3.2 PROCESS SEQUENCING AND SOLAR CELL FABRICATION

Selecting from this group of Category 4 process steps, a process sequence has been chosen for immediate study. While the process sequence is amenable to either P- on -N or N- on -P cells, the process is outlined for the N- on -P cell. The sequence, starting with a sawed and etched wafer containing no residual sawing damage, is as follows:

1. Perform P+ diffusion over entire wafer, simultaneously growing layer of SiO_2 . This forms the back surface field.
2. Apply photoresist to one side, remove SiO_2 on opposite side, remove photoresist.
3. Texture etch exposed silicon surface.
4. Deposit silicon nitride (CVD) over wafer surfaces.
5. Pattern metal grid into silicon nitride on textured surface using

photolithographic techniques, simultaneously cleaning dielectric from back surface.

6. Ion implant front (textured) surface with N-type dopant to form N-P junction. Ions are mechanically shadow masked from wafer edge to form planar junction.
7. Anneal wafers to activate ions. P-N junction in metal grid openings is deeper than beneath nitride.
8. Plate and sinter metallization.
9. Solder coat

This processing sequence produces a planar, shallow high quality P-N junction in a textured surface. The silicon nitride is a cheap and adequate antireflection coating. The cell has a back surface field and is solder coated. The single alignment for photolithographic patterning of the silicon nitride can be performed mechanically and requires no realignment. The P-N junction beneath the metal is deeper than the active area, allowing sintering of metal contacts for high adhesion.

The process is amenable to any silicon shape and degree of surface waviness, warp, etc., by utilizing projection photoresist exposure and by subsequent plating of contacts. In short, the process is most forgiving for the silicon geometrical variations possible from sheet growth.

Solar cells are being fabricated with this process to empirically evaluate its usefulness.

3.3 ANALYSIS OF PROCESSING COSTS

Following the qualitative cost analysis presented in Section 3.1, a detailed cost analysis is now underway. The approach taken by Motorola has

been to first evaluate processes from a technical feasibility standpoint, to select from these a group of likely candidates for future incorporation into a manufacturing process, and to perform detailed cost studies on these selected processes. Cost studies will be performed in detail on Category 4 processes.

An additional analysis is now underway to define facility and energy requirements for a factory to process solar cells. The factory design is obviously process-dependent and volume-dependent. The present analysis considers a fully integrated factory which starts with metallurgical grade silicon and ends with completed modules. Chemicals and materials for module pieceparts are the only externally supplied inputs to the factory. The analysis will consider equipment, process chemicals and supplies, warehousing, power conditioning and HVAC, pure water, waste disposal and reclamation, exhaust scrubbing, administration offices, cafeterias, rest rooms, parking, shipping, receiving, and maintenance.

3.4 ENCAPSULATION DESIGN

It is anticipated that the most common failure modes for solar cell modules will be one of two types:

1. Failure of a solar cell interconnect within the package, as a result of strains due to thermal stresses or mechanical motion, or as a result of chemical corrosion.
2. Localized interference of the optical path, e.g., due to coverage by a leaf, localized debris, or wildlife.

There is a trade-off between the solar cell durability in harsh environments and the encapsulation requirements to protect the cell from these environments. This trade-off must be considered in terms of a minimum twenty year service life for the encapsulated cell.

3.4.1 MOISTURE RESISTANT METALLIZATION

Semiconductor industry experience on reliability and failure modes indicates that the solar cell metallization and interconnect system can be expected to be the most vulnerable region to failure resulting from package moisture ingress. Absolute exclusion of moisture from a solar cell module for a period of twenty years would require hermetic seals, and hence would place severe economic strains on the encapsulation system. A far preferable solution would be a moisture resistant cell metallization and interconnect system.

Some current solar cell metallization systems, such as the titanium-silver, have already shown reliability problems in moist ambients and would require special protection techniques to achieve a twenty year minimum service life. This is not unexpected from experience by the semiconductor industry. Design choices for future solar cells should be based on metallization system reliability in moist ambients, and the final choice may be dictated primarily by this criterion.

It is not just moisture, but the combination of moisture and contaminants in the environment surrounding the metallization and contact (including applied or generated electric fields and contact potentials) that must be considered. Even gold, which is considered to be quite inert, has been shown to exhibit severe degradation via electrochemical attack in plastic-encapsulated integrated circuits.

3.4.2 REDUNDANT AND PARALLEL-ORIENTED INTERCONNECTION

The failure modes discussed above are most severe for series interconnected solar cells and suggest the future use of both redundant cell contacts and parallel-oriented cell interconnections.

Solar cell interconnect failures will be considerably reduced as a result of improved metallurgy and package design (and mounting). However, in aiming towards a mean-time-before-failure, MTBF, of 20 years, it must be expected that some interconnect failures will occur in a large array. In a series-connected panel, failure of an interconnect internal to the package (open circuit to either side of a solar cell) will cause entire module failure (open circuit). The use of redundant contacts to each solar cell will greatly reduce the magnitude of the effect of a single contact failure on the module performance. Instead of an open circuit, the output current will be reduced by some nominal factor (e.g., 10%, but dependent upon detailed cell design) if a single front surface contact opens.

Shadowing by relatively small objects is perhaps the most objectionable failure mode of the series-connected solar cell panel. Although intermittent, shadowing by leaves, debris, or wildlife on the external surface of a module will cause failure: almost total open circuit if an entire cell is shadowed, and reduced current output if the cell is only partially shadowed.

These types of failures may be alleviated by incorporating redundancy within a module through the use of a parallel or series-parallel cell interconnection schemes. Such schemes increase module (and system) reliability while insuring at least equivalent total system performance.

Any encapsulation design, thus, should avoid simple series interconnection and incorporate some degree of parallel interconnections.

3.4.3 MOISTURE INGRESSION TESTING

A stress testing method for measuring moisture ingress into potential encapsulation designs and materials has been investigated. The technique involves impregnation of color-indicating-dessicant materials into mock-ups of module designs. In a preliminary test, a color indicating dessicant was

impregnated into a silicone potting compound in dummy modules with a glass cover and a stainless steel backplate. The modules were then boiled in water for times up to two weeks, periodically inspecting the dessicant. An approximate value for both interfacial and bulk moisture ingression can be obtained merely by visual inspection. This technique is being utilized to evaluate encapsulation designs and materials.

3.4.4 PROTECTIVE COATINGS FOR METAL ENCAPSULANT PARTS

A metal back plate may be utilized in encapsulating solar cells. It must be corrosion-resistant to achieve the twenty year life expectancy of the module. Both aluminum and stainless steel are possible materials, with stainless steel having more suitable thermal expansion properties.

In order to reduce the overall cost of encapsulating solar cells, it would be desirable to utilize a cheaper material than stainless steel. Use of cold roll steel will result in a savings of 5X (i.e., St.St. = $60¢/\text{ft}^2$ - cold roll = $12¢/\text{ft}^2$). These prices reflect the cost of sheets 15 - 18 mils thick. It appears that cold rolled can be used if properly protected from the environment. A material, Rilsan Nylon II, has been used for approximately 25 years to coat items such as gas cylinders, underground piping, ship parts and outdoor furniture. It apparently has excellent wear properties for these and other applications. Application of the material is achieved by electrostatic spraying or fluid bed dipping followed by a heat treatment to fuse the powder. Electrostatic spraying can provide layers of approximately 3 mils while fluid bed applications have a minimum thickness of 8 - 10 mils. Material cost of $2\frac{1}{2}¢/\text{mil}/\text{ft}^2$ result in 7¢ for the electrostatic process and 18¢ - 25¢ for the fluid bed process. Application costs range from 2 to 5 times material cost. Electrostatic spraying of nylon on cold rolled steel could reduce costs without degrading life. Furthermore, numerous colors can be applied thereby improving reflecting and radiating qualities of the package.

Samples of this material will be obtained for evaluation.

4.0 CONCLUSIONS

A matrix of processing steps has been evaluated and individual process placed in four categories of projected usefulness. Of the forty-nine processes evaluated, fifteen are dropped from further consideration, six need technological advances before further evaluation, nine must be studied further to determine usefulness, and nineteen are deemed likely to be included in a future manufacturing process. Four of the processes earmarked for further study are gettering processes. A literature survey on gettering has been performed, and a bibliography is included in this report.

A process sequence has been chosen for initial fabrication of solar cells. The process includes texture etching, ion implantation, silicon nitride, and plated contacts.

Reliability considerations for solar cell modules dictate a moisture resistant cell metallization and a redundant, parallel-oriented interconnection scheme. A protective coating for steel makes it competitive with stainless steel with respect to corrosion. A stress test to study moisture ingression into modules is presented.

5.0 RECOMMENDATIONS

No specific recommendations are given this month.

6.0 CURRENT PROBLEMS

No specific problems have occurred to the date of this report.

7.0 WORK PLAN STATUS

The work plan is on schedule.

8.0 LIST OF ACTION ITEMS

No items requiring unusual action have come to light during this report period.

9.0 NEW TECHNOLOGY

There have been no reportable "New Technology" items uncovered during this period.

10.0 MILESTONES

Status of the program is shown on the Milestone Prediction and Accomplishment Chart, Figure 10-1.

MILESTONE PREDICTION AND ACCOMPLISHMENT CHART

MOTOROLA PROJECT No. 2258

JPL CONTRACT No. 954363

MILESTONE PREDICTION AND ACCOMPLISHMENT CHART

2 of 2

MOTOROLA PROJECT No. 2258

JPL CONTRACT No. 954363

STUDIES	MONTHS	F	M	A	M	J	J	A	S	O	N	D	J	F	M
Study X															
Development of Automation Concepts	Sched Act														
Study XI															
Baseline Cost Estimate		▲													
Program Plan			▲												
Financial Management and Cost Reports			▲	▲	▲	▲	▲	▲	▲	△	△	△	△		
Monthly Technical Progress Reports			▲		▲	▲		▲	▲		△	△			
Quarterly Reports				▲		▲			▲						
Final Report													△		△
Design Workbook															△
Progress Meetings		▲		▲		▲		▲		△		△			
Task Integration Meetings			▲			▲				△					
Workshop									△						

Legend: Scheduled △ Completed ▲

Date: 30 September 1976