LASER MICROFABRICATION TECHNOLOGY AND ITS APPLICATION TO HIGH SPEED INTERCONNECT OF GATE ARRAYS

Anthony F. Bernhardt, Bruce M. McWilliams, Fred Mitlitsky and John C. Whitehead

Lawrence Livermore National Laboratory, Livermore, CA

I. Introduction

A goal of the LLNL Laser Pantography (LP) program has been demonstrating processes in which a computer-steered and computer-modulated laser beam directly deposits or removes material onto or from a substrate such as a silicon wafer [1]. Substantial advantages could accrue from a fully developed set of such processes, including:

- Lower cost for prototyping and low volume manufacturing. The costly tooling phase and complex wafer processing sequence of conventional IC fabrication are eliminated, making limited-volume manufacturing less expensive.
- Faster fabrication. We estimate that two-level interconnect for very-large-scale integrated (VLSI) circuits can be fabricated on thirty-six hour time scales, with actual laser writing time of about one hour per interconnect level per die.
- On-line repair. Because LP is a serial process, defects observed during fabrication (for example, a shorted interconnecting structure) can be repaired under computer control.
- Customized computers. With simpler, faster, and more efficient manufacture, it becomes economically practical to fabricate computers customized for specific applications, even if only a few are built.

II. Laser Deposition Processes

A variety of laser-induced interconnection schemes has been studied [3]. These fall into two broad classes: photolytic and pyrolytic. The photolytic processes are based on local laser-induced photodecomposition reactions occurring either at the substrate and/or in the gas phase. The pyrolytic processes are based on chemical vapor deposition reactions which occur at the laser heated substrate.

Our research deals exclusively with pyrolytic processes. Some of the considerations of this choice include:

Heat Transfer. Using pyrolysis, very rapid deposition rates are obtained due to the high working temperature at the laser-heated spot on the surface. Such high temperatures ($\geq 1400^\circ\text{K}$) do not thermally compromise nearby structures due to the three-dimensional nature of the heat transfer to the substrate. (For example, when a one micron spot on the surface of a silicon wafer is heated to 1400°K the temperature three microns away is less than 500°K , as shown in Figure 2, falling even more dramatically than it would in most materials due to the temperature dependence of conductivity and diffusion constant in silicon.)

*This work was performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract No. W-7405-Eng-48.

Gas Transport. Gas transport to and from the reaction zone is also three dimensional. Thus, the high reaction rate allowed by high local surface temperature is complemented by rapid transport of reactant to the reaction zone and removal of product from it. At higher pressures, convection begins to dominate the mass transport, allowing still higher reaction rates than would be predicted based on the simple diffusion model in which rates saturate [3], [4].

Spatial Selectivity. Pyrolytic processes are capable of producing features which are comparable to or even smaller than the focal spot size of the laser [5]. Features are so well-defined due to the exponential nature of the reaction rate with temperature and to the localization of the heat at the point where the laser is absorbed. Since the gas is transparent to the laser, there is no restriction on gas pressure or on the length of gas through which the laser passes.

IC Compatible Chemistry. An extensive literature exists on CVD of materials used in the semiconductor industry. Although literature is more scarce at the elevated temperatures we use, most essential information, such as activation energy, is available.

Good Material Properties. LP is self-annealing, since the materials are hot when deposited. In the case of silicon, high levels of dopants are dissolved at the deposition temperature and frozen in as the material cools, so its conductivity is high.

III. Experimental Methods

Scanning a focused argon-ion laser beam (5145Å) with precisely computer-controlled intensity and position across a wafer is realized with the optical system displayed in Figure 1. The wafer is housed in a reaction vessel, into which reactant gases are introduced. Two acousto-optic (A/O) crystals deflect the beam in orthogonal directions, to allow short distance (0.5 mm) translation of the laser focus without mechanical moving elements. Relay optics image the deflected beam through a microscope objective, which focuses the beam to an approximately one micron scanning spot on the wafer within the roughly 500 x 500 micron scan field of the A/O deflectors. The reaction vessel is mounted on a motorized x-y stage to move the wafer between the 500-micron scan windows. A separate A/O device is used to control the laser power incident on the substrate. During laser writing, the deposition and etching microreactions are followed through the optical microscope/vidicon incorporated in the optical system. The apparatus and associated software are described in more detail elsewhere [1].

The maximum laser scanning speed within each A/O scanning window is about 100 mm/sec. In practice, the maximum useful scan rates are determined by the rate of the local surface chemistry, and are 1-10 mm/sec. Beam acceleration, deceleration and fly-back are limited only by the time required for the sound field to propagate across the diameter of the laser in the A/O crystal. The translation stages are capable of moving at several centimeters per second, but acceleration and deceleration times restrict the time to move from one window to the next. In gate array interconnect experiments discussed below, <25% of the elapsed time was consumed by translation stage motion and settling. At higher circuit densities, the translation stage motion should account for an even smaller fraction of process time.

One difficulty of writing on a gate array is the rapid change of thermal conductivity encountered at vias or metal features compared with that on areas of oxide. Although the apparatus is capable of very rapidly changing the laser intensity to compensate for such changes in the thermal landscape, registration and position tolerances must be very tight to avoid mistakes at edges of vias, etc.

We have largely avoided the thermal discontinuity problem by coating the surface of the wafer with a thin layer of amorphous silicon (a-Si) [2]. Amorphous silicon has absorption depth of $\sim 1000\text{\AA}$ at $5145\text{\AA}$ laser beam wavelength and is a good electrical insulator. In addition, even if the SiO_2 surface could be heated directly (e.g., with a CO_2 laser), many metals do not readily stick to glass, whereas a-Si adheres well to both SiO_2 and to many metals.

IV. Polysilicon Deposition

Polysilicon can be deposited by pyrolysis of either silane or disilane in the following reactions:

The addition of phosphine or diborane to the reaction gas produces doped polysilicon via the decomposition reactions:

Literature on CVD of silicon [6] suggests that the disilane reaction proceeds significantly faster than the silane reaction, and this turns out to be true for the high-temperature laser deposition process too. Figure 3 shows lines of polysilicon deposited from three mixtures of silane and disilane onto a silicon wafer covered with 1 micron of thermal SiO_2 and $1000\text{\AA}$ of a-Si. The reaction rate in pure silane is so slow that only the thinnest layer can be deposited at a writing speed of 1 mm/s and focal spot size of about 1 micron. The addition of 10% disilane dramatically increases the silicon deposition rate. With a majority of disilane (67%) in the gas, however, the morphology of the deposited line changes to one which does not have either good mechanical or electrical properties.

The majority of our polysilicon laser deposition work was done with a gas mixture composed of 25% disilane, 74% silane, and on the order of 1% dopant (see below). It should be noted, however, that the silane played little role in the deposition kinetics and was, in a number of experiments, replaced with hydrogen with no apparent affect. Figure 4 shows line area as a function of laser power for various gas pressures. For the ~ 1 micron laser spot there is a threshold for deposition of about 20 mW. As the laser power increases, line thickness and width increase. Line aspect ratio appears to be related to the thermal conductivity of the substrate layers and to the laser spot size. Typical width-to-depth aspect ratios for polysilicon on a-Si on 1 micron of SiO_2 are between 3:1 and 5:1.

Two processes apparently limit the laser power which can be applied to the substrate.

The first is a hydrodynamic one: in the absence of reactant gas the a-Si layer melts and the molten center is drawn to the cool sides [7]. The deposition process competes with the melt-flow process so that at 2190 Torr a laser power of 80 mW could be used to deposit heavy lines while at 990 Torr damage began closer to 40 mW. The second process, which may be associated with the first, is the onset of gas phase decomposition accompanied by particulate formation which litters the area all around the line. The tendency for the gas to "explode" increases with disilane concentration and is reduced when H₂ is substituted for silane in the standard mixture.

For laser direct-write deposition to be practical, there must be a reasonable range of laser power in which the process will work well. The combination of gas mixture and a-Si surface described here provides a range of about 50% in laser power in which lines of acceptable morphology are written.

Using a thicker layer (1500Å) of a-Si and 1000 Torr of the 25% disilane/silane mixture, thicker lines are deposited, as shown in Figure 5, and line area is observed to be essentially independent of doping.

The resistivity of laser-deposited polysilicon lines for diborane and phosphine dopant gases at higher laser powers is comparable to that of the best doped polysilicon produced by conventional CVD processes, ~3 mΩ-cm.

V. Nickel Deposition

Nickel is deposited by the decomposition of Ni(CO)₄ [2]:

Lines of nickel have been laser-written on semiconductor substrates under conditions very similar to those used for polysilicon. The amount of material deposited is also similar.

The substrates used were silicon wafers with 1 micron oxide and 2000Å a-Si. The submicron diameter Ar⁺ laser spot was scanned at speeds ranging from 0.2 mm/sec to over 10 mm/sec. Beam power measured immediately before the final microscope objective was varied from 20 mW to 50 mW.

Nickel carbonyl has a vapor pressure of about 315 Torr at room temperature. At power levels between 70 and 100 mW, the growth of material becomes unstable sometimes, causing nickel to be scattered over ~1 mm radius, including the vertical direction. These are not self-sustaining gas phase reactions, since lines can be deposited on another part of the wafer without any apparent depletion of the reactant gas. The explosive behavior suggests there is a limit to how fast the material can smoothly grow, and that this limit is not due to gas transport. In an attempt to suppress this process we added N₂ or CO diluent to the gas. N₂ seemed to have little effect on either deposition or homogeneous decomposition. The CO significantly raised the laser power threshold for "explosion" but reduced the deposition rate.

Figure 6 shows the morphology of nickel lines deposited on 2000Å of a-Si on 1 micron thermally deposited SiO₂. Figure 7 shows that line width is approximately independent of writing rate between 0.2 and 10 mm/s while thickness falls from 1.5 μm to 0.2 μm at 50

mW laser power and from $0.4\text{ }\mu\text{m}$ to $0.07\text{ }\mu\text{m}$ at 20 mW laser power. The gas is 100 Torr of $\text{Ni}(\text{CO})_4$.

The nickel line resistivity varies from $\sim 16\text{ }\mu\Omega\text{-cm}$ at low laser power to about $\sim 12\text{ }\mu\Omega\text{-cm}$ at high laser power. Bulk nickel has a resistivity of $6.9\text{ }\mu\Omega\text{-cm}$.

VI. Laser-Interconnection of Gate Arrays

For laser interconnection studies, we used commercial 1000 gate CMOS die. This gate array is designed for single level 5 micron-wide metallization with underlying polysilicon tunnels for routing. As supplied by the vendor, wafers are covered with approximately one micron of aluminum-silicon alloy which is then patterned using conventional photolithography to leave I/O pads with interconnected drivers, power distribution, plugs in contact vias, and a few simple logic gates interconnected at the periphery for test purposes.

Our most rigorous test of the laser interconnect process is a chip composed of one 16-stage counter and five 16-stage shift registers. The basic building block of each circuit is a D flip-flop implemented with transmission gates. Figure 9 shows an SEM of a piece of a shift register interconnected with boron-doped polysilicon deposited at transverse laser velocity of 1 mm/s and power of 100 mW. (This circuit was also successfully written in phosphorous-doped polysilicon.) As mentioned above, line dimensions vary as the thermal conductivity of layers under the line changes. Thus, the laser-deposited lines in Figure 9 narrow as the line passes over an aluminum power bus or into a via. The insulating nature of the a-Si mitigates changes in thermal conductivity to the extent that it is not necessary to increase the laser power when traversing such features.

The counter and one of the shift registers were wired to output buffer ports at each stage to monitor sequential operation by electrical probing after laser interconnection. Figure 10 shows the state of every second stage of the shift register, for the input pattern frequency of 1 MHz. The bottom trace (pin 80) in the input test vector. Oscilloscope traces of the counter output at various stages are given in Figure 11. The clock rate is 1 MHz. These results demonstrate essentially ideal operation of this laser-wired 1260 inverter circuit. The total time elapsed in writing this circuit was 6 minutes.

In summary, we have used LP to interconnect a variety of functioning digital logic circuits of roughly 1000 gate complexity in doped polysilicon. Recent results for the direct writing of high quality nickel lines at mm/sec scan rates suggest that this process may be useful for gate array interconnection.

ACKNOWLEDGEMENTS

David Askenas, Steve Farmwald, Jim Kaschmitter, Loren Kohnfelder, Harlan Lau, Jerrold Rittmann, and David B. Tuckerman made major contributions to equipment and software used in the work reported. Lowell L. Wood and A. Carl Haussmann have been instrumental in making this effort possible. The work was sponsored by DoE (through LLNL's IR&D Program) and DoD (through the VHSIC Program Office under Contract No. FY1175-85-N-5695, monitored by J. P. Letellier). John C. Whitehead was supported by the Fannie and John Hertz Foundation. Fred Mitlitsky was aided by Prof. Richard M. Osgood, Jr. and the Columbia University Electrical Engineering Department.

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FIGURE CAPTIONS:

- Figure 1. Laser direct-write apparatus.
- Figure 2. Temperature falls rapidly as a function of distance from a hot spot on a half-space of crystalline silicon, so that the deposition process need not damage devices.
- Figure 3. Polysilicon line morphology and size changes dramatically as the disilane fraction of the gas changes: a) 100% SiH_4 , b) 10% Si_2H_6 , 90% SiH_4 , c) 67% Si_2H_6 , 33% SiH_4 .
- Figure 4. Polysilicon line area is a strong function of both laser power and gas pressure. The threshold of 20 mW is close to the melt threshold of a-Si. Laser power is limited in this case by separation of the molten a-Si, exposing the underlying oxide faster than Si can be deposited from the gas.
- Figure 5. Somewhat thicker a-Si (1500Å) permits deposition of larger lines at higher laser powers. Line area is essentially independent of doping.
- Figure 6. Laser-deposited nickel lines are very smooth as deposited. They tend to be wider than polysilicon lines similar thickness.
- Figure 7. Nickel line width is independent of writing rate between 0.2 and 16 mm/s. Only line thickness changes.
- Figure 8. SEM of a section of a shift register interconnected in B dopes polysilicon. Write rate is 1 mm/s at 100 mW laser power.
- Figure 9. Shift registers are tested at 1 MHz with the input test pattern on the bottom trace (pin 80).
- Figure 10. Two counter outputs are shown together with the input waveform (bottom trace).

A

B

C

4 μ m

4 μm

4 μm

TIMING DIAGRAM

MAG: 1

CURSOR SEQ: 54

C - N = +4.800µS

DELTA TIME: 0N

SRCH = XXX XXX XXX XXX

T C

POD CH NAME

2A 6 PIN 56

2A 6 PIN 55

2A 5 PIN 59

2A 4 PIN 63

2A 3 PIN 67

2A 2 PIN 71

2A 1 PIN 76

2A 0 PIN 80