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ORNL/TM-5643
(Vol. 6 of ORNL/TM-5638)

ORELA Data Acquisition System Hardware

Vol. 6: Eight-Stage Stacking Buffer Memory
(Q-5066)

R. E. Wintenberg
J. W. Reynolds

OAK RIDGE NATIONAL LABORATORY

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Printed in the United States of America. Available from
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road, Springfield, Virginia 22161
Price: Printed Copy \$4.00; Microfiche \$3.00

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ORNL/TM-5643
(Vol. 6 of ORNL/TM-5638)

Contract No. W-7405-eng-26

INSTRUMENTATION AND CONTROLS DIVISION

ORELA DATA ACQUISITION SYSTEM HARDWARE

Vol. 6: Eight-Stage Stacking Buffer Memory
(Q-5066)

R. E. Wintenberg and J. W. Reynolds

Date Published: January 1977

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ORNL/TM-5639 (Vol. 2 of ORNL/TM-5638)	Four-Channel Priority Multiplexers (Q-5036-1, -3, -12 through -25, and -29)
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ORNL/TM-5645 (Vol. 8 of ORNL/TM-5638)	Instruction Manual for the Ground Isolation Driver and Receiver Cards on the Quiet Ground System at ORELA

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ABSTRACT

A Stacking Buffer Memory for de-randomizing data on high data rate experiments at ORELA is documented by a description of operation, mechanical details of design, and a detailed theory of operation illustrated through six examples of operation.

1. INTRODUCTION

A Stacking Buffer Memory^{1,2,3} is used to de-randomize input data for certain time-of-flight experiments at ORELA. In particular, the instrument represented by ORNL Instrumentation and Controls Division Drawing Series Q-5066* (see Table 1) is an eight-stage, 30-bit per stage, first-in/first-out register memory with asynchronous simultaneous input and output at a maximum of 5×10^5 events/sec. It is contained in a three-wide Nuclear Instrument Module with three electronic sub-sections: the memory containing latch registers for temporary storage of eight 30-bit events, a control section to keep track of the empty and full latch registers, and an interface control to synchronize the asynchronous input and output transfers to an internal 1-MHz crystal-controlled clock. The minimum time for repeated synchronization and transfers is 2 μ sec. A block diagram of the module is given in Fig. 1. The 30 data bits in an event are transferred to the SEL 810B computer via the Four-Channel Priority Multiplexer^{4,5} as two 16-bit words. The multiplexer hardware adds two channel-identification bits to the first word.

2. DESCRIPTION OF OPERATION

Each event presented to the buffer by the signal Exp. Data Ready, see Fig. 1, is stored in a memory register, a series of 30 latches; and a register control flip-flop also stores a 1 to indicate the full condition of one memory register. A busy signal, Buffer Busy, is produced for 1.4 μ sec after each event is received, or a positive dc level will be present if the Buffer Full condition (meaning all eight memory stages contain data) is the result of the input transfer. In addition, a

*The authors wish to acknowledge the contribution of A. Richard Smith, Jr., a summer trainee from Houghton College, Houghton, N.Y. 14744, for his translation of the logic design to the detailed 7400 series logic diagrams.

Table 1. Drawing list for a Stacking Buffer Memory

ORNL I&C Division Drawing Series Q-5066

Number	Subtitle
-1	Interfacing Control Logic
-2	Memory Registers 1 thru 4 Logic
-3	Memory Registers 5 thru 8 Logic
-4	Three-Wide NIM Backplate
-5	Metalphoto Panel
Q-2928-11	ORELA Data Acquisition, BTC, Multiplexer, and I/O Bus Scaler Cable Connectors
Q-2800-4	Standard Nuclear Instrument Modules, Module Assembly
Q-2800-5A	NIM System AEC Standard, Connector Assemblies
Q-2800-5B	Standard Nuclear Instrument Modules, Connector Wiring, 42-Position Series "M" Connector

300- μ sec-wide Buffer Data Accepted pulse is generated at the end of any busy period. The input device must use either or both signals to hold the input data constant during the Buffer Busy time; otherwise, erroneous data may be stored.

The first event is stored in Memory Register 8 by passing it through the open gates at the input to the output of each memory register. If no data is transferred from the buffer during the input of eight events, the eighth event will be stored in Memory Register 1. The eight events can be accepted in a minimum time of 16 μ sec, i.e., two clock periods for each event. Events are transferred out of Memory Register 8 through the use of two control signals: Buffer Data Ready and Data Accepted to and from the input device respectively. Buffer Data Ready initiates the output transfer which is completed when Data Accepted is returned by the input device. Then Data Accepted causes register control flip-flop 8 to reset to the empty state. The empty condition is then transferred on each succeeding clock cycle to register control flip-flop 7, 6, etc., as required by the degree of fullness of the Stacking Buffer Memory. If data transfers are attempted during Buffer Busy, data will be lost.

An internal manual RESET by a push-button switch or an external RESET pulse will force all eight register control flip-flops to the empty state.

3. MECHANICAL DETAILS

The front panel, see Dwg. No. Q-5066-5,^{*} has five test points and a ground reference, four channel indicators, a RESET push-button switch, and two coaxial connectors: RESET and BUFFER BUSY. The test points, labeled on Dwg. No. Q-5066-1, are the following:

- TP1 Exp. Data Ready
- TP2 Data Accepted
- TP3 Channel Busy
- TP4 Buffer Data Accepted
- TP5 Buffer Data Ready.

The channel indicators are used to indicate which multiplexer channel in the SEL 810B Data Collection Equipment Cabinet is connected to an experimenter. (The computer software must be given this channel number during setup for data acquisition.) See Dwg. No. Q-5066-1, location E9 for the wiring of the channel indicators.

The rear panel, see Dwg. No. Q-5066-4, has three connectors: input, output, and power. The power connector is an AEC NIM System Standard Connector Assembly PGM per Dwg. Nos. Q-2800-5A and -5B. The power wiring is on Dwg. No. Q-5066-1, at location E6. The input and output connectors have 75 pins, with 37 twisted pairs and a drain wire for the cable shield. Tables 2 and 3 list the input and output connections. A connector parts list is given in Table 4; assembly details can be found on Dwg. No. Q-5066-1, location G6.

A Stacking Buffer Memory is connected between an experimenter's input device and a Multiplexer Input Ground Isolation chassis⁶ connected to a Four-Channel Priority Multiplexer, as shown on Dwg. No. Q-5066 1. The 37-pair connecting cables are wired per Dwg. No. Q-2928-11, "ORELA Data Acquisition, BTC, Multiplexer, and I/O Bus or Scalar Cable Connectors."

The chassis is assembled in a three-wide Nuclear Instrument Module. See Dwg. No. Q-2800-4, "Standard Nuclear Instrument Modules, Module Assembly" for the basic chassis. Assembly details can be obtained from ORNL Photo Nos. 0291-72, 0293-72, and 0294-72.

^{*} See Sect. 5, Engineering Drawings, for the Q-drawings cited in this volume.

Table 2. Stacking Buffer Memory input connections

Pin+	Pin-	Function	Pin+	Pin-	Function
101 ^a	201	MPXR Control	308 ^b		
102 ^a	202	MPXR Interrupt	408 ^b		
103	203	System Tag, Bit 2	309	409	Second Word, Bit 0
104 ^c	204	First Word, Bit 3	310	410	Second Word, Bit 1
105 ^c	205	First Word, Bit 4	311	411	Second Word, Bit 2
106 ^c	206	First Word, Bit 5	312	412	Second Word, Bit 3
107 ^c	207	First Word, Bit 6	313 ^b		
108	208	First Word, Bit 7	501	601	Second Word, Bit 4
109	209	First Word, Bit 8	502	602	Second Word, Bit 5
110	210	First Word, Bit 9	503	603	Second Word, Bit 6
111	211	First Word, Bit 10	504	604	Second Word, Bit 7
112	212	First Word, Bit 11	505	605	Second Word, Bit 8
113 ^b			506	606	Second Word, Bit 9
301	401	First Word, Bit 12	507	607	Second Word, Bit 10
302	402	First Word, Bit 13	508	608	Second Word, Bit 11
303	403	First Word, Bit 14	509	609	Second Word, Bit 12
304	404	First Word, Bit 15	510	610	Second Word, Bit 13
305	405	Exp. Data Ready	511	611	Second Word, Bit 14
306 ^d	406	Buffer Data Accepted	512	612	Second Word, Bit 15
307 ^d	407	Buffer Busy	513	(Shield)	

^aOutput from the computer.

^bNot used.

^cThese inputs are used for experimenter tags.

^dOutput from the buffer.

4. DETAILED THEORY OF OPERATION

The theory of operation for the Stacking Buffer Memory (SBM) is presented below by six examples, each with an associated timing diagram. They are: (1) input of a word with the buffer empty, (2) input of a word with one word in the buffer, (3) multiplexer channel goes not-busy with one word in the buffer, (4) multiplexer channel goes not-busy with more

Table 3. Stacking Buffer Memory output connections

Pin+	Pin-	Function	Pin+	Pin-	Function
101 ^a	201	MPXR Control	308		Channel 3 Indicator
102 ^a	202	MPXR Interrupt	408		Channel 2 Indicator
103	203	System Tag, Bit 2	309	409	Second Word, Bit 0
104 ^b	204	First Word, Bit 3	310	410	Second Word, Bit 1
105 ^b	205	First Word, Bit 4	311	411	Second Word, Bit 2
106 ^b	206	First Word, Bit 5	312	412	Second Word, Bit 3
107 ^b	207	First Word, Bit 6	313		Channel 1 Indicator
108	208	First Word, Bit 7	501	601	Second Word, Bit 4
109	209	First Word, Bit 8	502	602	Second Word, Bit 5
110	210	First Word, Bit 9	503	603	Second Word, Bit 6
111	211	First Word, Bit 10	504	604	Second Word, Bit 7
112	212	First Word, Bit 11	505	605	Second Word, Bit 8
113 ^c		Channel 0 Indicator	506	606	Second Word, Bit 9
301	401	First Word, Bit 12	507	607	Second Word, Bit 10
302	402	First Word, Bit 13	508	608	Second Word, Bit 11
303	403	First Word, Bit 14	509	609	Second Word, Bit 12
304	404	First Word, Bit 15	510	610	Second Word, Bit 13
305	405	Buffer Data Ready	511	611	Second Word, Bit 14
306 ^d	406	Data Accepted	512	612	Second Word, Bit 15
307 ^d	407	Channel Busy	513	(Shield)	Channel Indicator Gnd

^aOutput from the computer.

^bThese inputs are used for experimenter tags.

^cNot used.

^dOutput from the multiplexer.

than one word in the buffer, (5) input of a word simultaneously with output when one word is stored in the buffer, and (6) input of a word simultaneously with output when more than one word is stored in the buffer. References below to locations on Drawing Series Q-5066 indicate sheet and area. For example, the abbreviation [2D6/1] means sheet 2, area D6 through D1.

Table 4. Connector parts list for a Stacking Buffer Memory

Description	Part Number ^a	ORNL Stores Number	Quantity
MCB, male block	202515-5	06-867-2123	1
GP-1, guide pin	200833-4	06-867-2065	1
GS-1, guide socket	203964-4	06-867-2066	2
GGP, ground guide pin	202514-1	06-867-2067	1
HM, module connector hood	202394-2	06-867-2070	1
Contact, pin	201330-1	06-867-2013	
Chassis 75 Male			
Block, pin, 75	201311-3	06-867-2138	1
Contact, pin	201330-1	06-867-2013	75
Pin hood, 75	201368-4	06-867-2074	1
Corner guide, pin	201046-2	06-867-2056	2
Corner guide, socket	203966-2	06-867-2058	2
Jackscrew, fixed, male	200874-2	06-867-2144	1
Jackscrew, fixed, female	200875-2	06-867-2145	1
Chassis 75 Female			
Block, socket, 75	201310-3	06-867-2139	1
Contact, socket	201328-1	06-867-2023	75
Corner guide, pin	201046-2	06-867-2056	2
Corner guide, socket	203966-2	06-867-2058	2
Jackscrew, fixed, male	200874-2	06-867-2144	1
Jackscrew, fixed, female	200875-2	06-867-2145	1

^aAMP Inc., Harrisburg, Pennsylvania.

The extremes of timing for the Ready latch [1B3] due to synchronization of the asynchronous Exp. Data Ready signals with the internal 1-MHz crystal clock are shown in Fig. 2. The 1-μsec width should occur about 97% of the time.

Fig. 2. Extremes of Ready latch timing.

4.1 Example 1A, Input Transfer with the Buffer Empty and a Busy Multiplexer

Data is transferred when the SBM is empty and the multiplexer channel is busy. See Fig. 3 for a timing diagram.

Data is placed on the input lines [2D6/1], then Exp. Data Ready [1B1] is generated by the input device. The input data ripples through the latches (Integrated Circuit Type SN7475N) of Memory Registers 1 through 7 to the latches in Memory Register 8 (MR8) [3D6/2]; all latches now have the same data. Note that all of the Control flip-flops [column 7 on sheets 2 and 3] are set to the cleared state, $\overline{C1}$, $\overline{C2}$, etc.; therefore, the Gate signals [column 6 on sheet 3] to the SN7475N latches are positive. If the latch clock (Gate) signal is positive, the data on the D input of the SN7475 latch [2A5] is present on the Q output of the latch. A negative clock signal will retain the data that was present at the time of the transition from high to low.

Exp. Data Ready, sharpened to 30 nsec in a Schmitt triggered one-shot multivibrator 101[1A3], sets a Ready latch, which enables the Clock 1 Ready latch through inverter 104-4. Setting the Ready latch also triggers a 1.4- μ sec Buffer Busy pulse [1B9]. The input data should be held constant until Buffer Busy, a positive pulse or dc level, goes to ground. The trailing edge of the Buffer Busy signal triggers a 300-nsec Buffer Data Accepted pulse. Either Buffer Busy, Buffer Data Accepted, or both can be used by the input device to control the input data.

The leading edge of Clock 1 [1C3] from the 1-MHz crystal clock [1C2] causes a 30-nsec-wide pulse in Schmitt trigger A3 [1B4]. The 30-nsec pulse then completes the setting of the Clock 1 Ready latch [1B4], thereby generating a Clock 1 Data Ready to the control logic [2D8]. The Ready and Clock 1 Ready latches are reset on the trailing edge of the Clock 1 pulse that set the Clock 1 Ready latch. The result is a Clock 1 Data Ready pulse with a width of 100 to 125 nsec. The width is dependent upon when the Exp. Data Ready occurs with respect to the 30-nsec window at the leading edge of Clock 1.

The Clock 1 Data Ready pulse ripples through eight OR gates, with a typical total delay of 76 nsec, to AND gate 125-3 [3B8]. The trailing

Fig. 3. Timing diagram for input transfers with a busy multiplexer and buffer empty, example 1A, or one word in buffer, example 1B.

edge of the 60-nsec-wide output pulse from NAND gate 125-3 sets C8, (SN 74107 Master-Slave flip-flop) via inverter 118-5. Note that NAND gate 125-3 also controls the NAND gates to Control flip-flops C7, C5, C3, and C1 directly and to Control flip-flops C6, C4, and C2 via NAND gate 120-3 [3C8].

The set side of C8 enables flip-flop C7 for setting and causes the Gate 8 signal to the clock inputs of the latches in MR8 to go low, thereby retaining the incoming data. The reset output of the same flip-flop, called Buffer Loaded [1D6], simultaneously triggers the Schmitt triggered one-shot multivibrator 127 [1D7] to generate a 6- μ sec-wide Buffer Data Ready signal [1D9] to the Four-Channel Priority Multiplexer at the SEL 810B computer. The multiplexer channel returns a Channel Busy signal [1D10] in about 1 μ sec because of ground isolation circuit and cable delays. (Channel Busy, TP3, is not used by the SBM control.) The SBM control now waits until a Data Accepted signal is returned by the multiplexer-computer (example IB) or until more data arrives (example IIA).

4.2 Example IB, Input Transfer with One Word in the Buffer and a Busy Multiplexer

Data is transferred when the SBM contains one word with the multiplexer channel busy. See Fig. 3 for a timing diagram.

This example operates exactly as example IA, except that the pulse from NAND gate 125-3 [3B8] is routed through NAND gate 120-3 [3C8] to set C7 on the trailing edge of the pulse. Flip-flop C7 has its steering controlled by the set output of C8. The resulting high condition of the C7 output will cause the Gate 7 signal to the clock inputs of the latches in Memory Register 7 to go low. The 30 data bits of the second event are now stored in MR7. The C7 output via two inverters for timing adjustment, also steers Control flip-flop 6 to obtain a set condition on the next Clock 1 Data Ready through NOR gate 125-1. The C7 output is also routed to NOR gate 120-4, thereby enabling NAND gates 120-3 and 125-3, via NOR gate 125-4, to allow Buffer Clock 1 to control the ripple of a vacant storage location toward MR1.

In similar fashion Memory Registers 6, 5, 4, 3, 2, and 1 will successively store data. When C1 is set, the negative level from $\overline{C1}$, Buffer Full, will hold the Buffer Busy signal [1B9] in the positive or on state. Further data should not be sent to the SBM until a Buffer Data Accepted signal occurs. A Buffer Data Accepted signal is not returned to the experimenter's input device when MR1 stores data. It is delayed until storage space becomes available as a result of data being unloaded from the buffer. See example IIB.

4.3 Example IIA, Output Transfer Completed with One Word in the Buffer

The multiplexer channel goes not-busy with one word in the SBM. See Fig. 4 for a timing diagram.

A Data Accepted pulse [1D1] is received coincident with the return of the Channel Busy signal to ground. The Data Accepted pulse is sharpened to a 30 μ sec-wide pulse in a Schmitt triggered one-shot multivibrator A2 [1D3]. The 30- μ sec pulse sets an Accepted latch. Clock 2, lagging behind Clock 1 by 250 μ sec and occurring within 1 μ sec after Data Accepted, together with the negative output of the Accepted latch set a second latch, Accepted & Clock 2, which causes the signal Reset 8 [1E4]. Both latches are reset on the trailing edge of Clock 2, a 125- μ sec-wide pulse.

The signal Reset 8 then resets C8 [3B7], whose C8 output enables Control flip-flop 7 for resetting (it is already reset) and opens Gate 8 to the clock inputs of the latches of MR8. The SBM, with all Control flip-flops reset, then waits for the next Exp. Data Ready (example IA).

4.4 Example IIB, Output Transfer Completed with n Words in the Buffer

The multiplexer channel goes not-busy with more than one word in the SBM. See Fig. 5 for a timing diagram.

This example operates exactly as example IB to the point where Control flip-flop 8 [1B7] is reset and Gate 8 goes positive. At the trailing edge of the next Clock 1 pulse, 750 μ sec after Clock 2, C8

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Fig. 4. Timing diagram for example IIA, output transfer completed with one word in the buffer.

Fig. 5. Timing diagram for example IIB, output transfer completed with n words in the buffer and example IIIA, output and input transfers with one word in the buffer.

is set, which causes Gate 8 to go to ground (closed), and C7 [1C7] is reset, which causes Gate 7 to go positive or open. Each successive Clock 1 pulse will cause a pair (7 and 6, 6 and 5, 5 and 4, 4 and 3, etc.) of Control flip-flops to set and reset, with their corresponding gate signals going closed and open respectively. In this manner, the contents of each memory register are shifted to the one below it. A maximum of 7.75 μ sec, including synchronization with data accepted, is required to empty MR1 if all of the registers contained data.

4.5 Example IIIA, Output and Input Transfers with One Word in the Buffer

A data word is transferred into the Stacking Buffer Memory with one word already in the buffer, at the same time that a word transfer out is completed. See Fig. 5 for a timing diagram.

The incoming data word would ripple through the memory registers and appear on the output of MR7. There are two possible timing sequences, which are dependent upon whether Clock 1 or Clock 2 occurs first.

Case 1. If Clock 2 occurs first, the timing would follow example IIB, Fig. 5, except that Controls 6 and 7 and Gates 6 and 7 would be at a constant ground and positive level respectively.

Case 2. If Clock 1 occurs first, the timing differences would be those shown on Fig. 5 by dotted lines on the signals Controls 7 and 8 and Gates 7 and 8.

4.6 Example IIIB, Input Transfer with n Words in the Buffer While Stored Data is Rippling Down to Memory Register 8 for Output

A data word is transferred into the SBM when n words are stored, with data rippling down as a result of data transfer out of the buffer.

It is assumed that n is less than or equal to 6; that is, at least MR1 is free and one vacant storage location is rippling toward MR2. This would be a normal condition, since the multiplexer computer response to a Buffer Data Ready signal occurs within 10 to 50 μ sec. The exact minimum time is dependent upon the activity of the data acquisition computer; while the maximum time is dependent upon the number of experiments connected (a maximum of four) and their data rates.

Transfer of the data word into the computer would follow the timing diagram of example IIA, Fig. 3. The interesting case is the ripple of the vacant location into MR2 when it is coincident with loading data into MR1, as shown in Fig. 6. The relative timings of the Control 1 and 2 and Gate 1 and 2 signals are dependent upon the delay times through the logic and will be different for each pair of Control flip-flops.

Also included in the lower half of Fig. 6 is the timing following a Data Accepted pulse that occurs between Clock 1 and Clock 2, with the resultant ripple up of the vacant storage location through Memory Registers 7, 6, 5, etc.

5. ENGINEERING DRAWINGS

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Reference Drawings

(The following related drawings are not included here due to space limitations, but are available from the authors.)

- Q-2800-4 — Standard Nuclear Instrument Modules, Module Assembly
- Q-2800-5A — Standard Nuclear Instrument Modules, Connector Assemblies
- Q-2800-5B — Standard Nuclear Instrument Modules, Connector Wiring
- Q-2928-11 — ORELA Data Acquisition, BTC, Multiplexer, and I/O Bus or Scaler Cable Connectors
- Q-5066 — (see list of Table 1)

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Fig. 6. Timing diagram for example IIIB, input transfer with n words in the buffer while stored data is rippling down to Memory Register 8 for output.

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