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DIP COATING PROCESS

Silicon Sheet Growth Development for the Large-Area
Silicon Sheet Task of the Low-Cost Silicon Solar Array Project.
Quarterly Report No. 5, December 18, 1976—March 21, 1977

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MASTER

March 31, 1977

Work Performed Under Contract No. NAS-7-100-954356

Honeywell Corporate Research Center
Bloomington, Minnesota

ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
Division of Solar Energy

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Silicon Sheet Growth Development for the
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Quarterly Report No. 5,

by

J. D. Zook, J. D. Heaps
R. B. Maciolek, B. Koepke,
C. D. Butter and S. B. Schuldt

Period Covered 12/18/76 - 3/21/77

Published March 31, 1977

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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the U. S. Energy Research and Development Administration, Division of Solar Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by ERDA and forms part of the ERDA Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

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ABSTRACT

Ceramic substrates can be coated with a thin layer of large-grain polycrystalline silicon by a dip-coating process. The silicon-on-ceramic (SOC) material appears to be quite promising as a low-cost cell material but requires somewhat special fabrication procedure since the contacts to both the n- and p- layers are now made on the front surface.

Solar cells have been made on SOC material and on single-crystal control samples. Photodiodes 0.01 to 0.1 cm² made on substrates coated with vitreous carbon prior to dip coating with silicon showed the best efficiency of SOC material to date, namely over 6 percent uncorrected and about 12 percent inherent efficiency.

Etching procedures have indicated that the dislocation density varies from almost 10⁷ cm⁻² to almost dislocation-free material, assuming that all etch pits are due to dislocations. EBIC measurements procedures were also improved, and it was found that diodes appear to be fairly uniform in EBIC response.

A new SOC coating facility is being designed which will coat larger substrates in a continuous manner. The purpose is to minimize the contamination problem by reducing the contact area of the substrate with molten silicon. By having much larger throughput, it will also demonstrate the scale-up potential of the silicon-on-ceramic process. Portions of the new facility are under construction.

An attempt has been made to model the economics of a large-scale facility for coating ceramic panels with silicon. A first iteration based on available parameters estimates showed that major cost items were poly Si (\$2.90 per square meter), labor and burden (\$2.50 per square meter), and the ceramic substrate (\$2.50 per square meter), for a total price of about \$11 per square meter.

SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

During this quarter, significant advances in solar cell fabrication have been made. The silicon-on-ceramic (SOC) material requires somewhat special fabrication procedure since the contacts to both the n- and p- layers are now made on the front surface. The electrical contact to the lightly doped p-type base region had been a problem, and this has been solved by the use of sputtered platinum silicide (PtSi) contacts. Techniques for evaluating contacts on test samples and in actual cells have been developed and showed that PtSi had the lowest contact resistivity of the techniques tested. Low-cost alternatives will be pursued. The contact between silicon and vitreous carbon can also be low-resistance, but tends to be nonuniform in contact resistivity.

Solar cells have been made on SOC material and on single-crystal control samples. Aluminum doping is found to produce cells comparable to the usual boron-doped material. Control cells 1cm^2 made with PtSi contacts had uncorrected efficiencies over 8 percent. Small SOC photodiodes made on substrates coated with vitreous carbon (Vitregraf) showed the best efficiency of SOC material to date, namely over 6 percent uncorrected and about 12 percent inherent efficiency.

Several improvements have been made in the silicon dip-coating facility. Etching procedures have indicated that the dislocation density varies from almost 10^7 cm^{-2} to almost dislocation-free material. The analysis assumes that all etch pits are due to dislocations, and the validity of this assumption is under investigation. EBIC measurement procedures were also improved, and it was found that diodes appear to be fairly uniform in EBIC response. Chemical analyses have not detected definite impurities, but the IMMA system appears to offer the required sensitivity to detect trace "impurities of interest."

The microstructure of Coors S1SI mullite has been compared to McDanel MV20 mullite. Acid leaching of the mullite was found to dissolve the glassy phase, and this reveals the acicular

morphology of the mullite crystallites. EDAX analysis of the leached phased showed some reduction of the impurities, especially K and Ti. Chemical analysis, however, showed no significant difference in impurity content of the leached and unleached material.

A new SOC coating facility is being designed which will coat larger substrates in a continuous manner. The purpose is to minimize the contamination problem by reducing the contact area of the substrate with molten silicon. By having much larger throughput, it will also demonstrate the scale-up potential of the silicon-on-ceramic process. Portions of the new facility are under construction.

An attempt has been made to model the economics of a large-scale facility for coating ceramic panels with silicon. A first iteration based on available parameters estimates showed that major cost items were poly Si (\$2.90 per square meter), labor and burden (\$2.50 per square meter), and the ceramic substrate (\$2.50 per square meter), for a total price of about \$11 per square meter.

INTRODUCTION

This research program commenced October 21, 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 10 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. If a coating method for producing silicon on ceramic (SOC) can be shown to produce solar cell-quality sheet silicon, it offers an outstanding cost-effective way to produce inexpensive, large-area solar cells.

The SOC approach has excellent scale-up potentialities. With the dip coating method it is possible to coat several wide, large-area substrates in one dipping. Another method we are pursuing is to silicon-coat, in a continuous manner, large-area substrates. The investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

Since the inception of this program, an experimental dip coating facility was designed and constructed. In this facility a variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25cm^2 in area have been achieved with single crystal grains as large as 4mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and rate at which the substrate is withdrawn from the melt.

The solar cell potential of this (SOC) sheet silicon, to date, remains promising. Photodiodes have been fabricated that, without the benefit of an antireflecting coating and minimized series resistance, demonstrated a measured conversion efficiency of >6 percent. After correction for the absence of an antireflection coating and allowing for excess series resistance, which results from the fabrication geometry, these dip-coated layers show an inherent conversion efficiency of ~ 12 percent. To date 1cm^2 solar cells have been fabricated with open-circuit voltages and short-circuit current densities of 0.4 volts and $17\text{mA}/\text{cm}^2$ respectively.

The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The aluminum and other impurities of the substrate are believed to adversely affect solar cell conversion efficiency. A special type of graphite coating on the substrate has shown a potential for inhibiting this dissolution of mullite. Should these coatings prove to satisfactorily isolate the substrate from the melt in a cost-effective manner, improved solar cell performance should be forthcoming.

An alternative solution to this dissolution problem, which will be investigated, is to limit the contact area and contact time between the ceramic and the molten silicon. This approach is being pursued by designing and constructing a second silicon coating facility. This additional facility is being designed to coat in a continuous manner one face of long, large-area substrates. The design will restrict the contact area of the ceramic with molten silicon and should completely eliminate progressive contamination of the melt. Further, it will permit a study of possible continued grain growth by accommodating the use of longer substrates. Finally it will reveal problems that are likely to be encountered in a scale-up process.

The balance of this document will report the progress achieved during the past quarter year of effort.

TECHNICAL DISCUSSION

SILICON FILM GROWTH MECHANISMS. (R. Maciolek, C. Knudson, S. Marquardt, D. Sauve)

Apparatus and Procedure

During the first quarter of 1977 several changes were made in the dip-coating system with the objective of improving precision, reliability, ease of operation and coating quality. A 2cm-diameter viewing port was installed in the top of the apparatus to make possible the direct observation of the melt and dipping process. Previously the process had been observed using a mirror which suffered from thermal distortion and which, in time, was obscured by vapor deposited material. Several modifications were also made in the temperature control system and dipping mechanism.

A subsequent run failed to show any significant improvement in coating quality that could be attributed to the temperature control system or dipping mechanism modifications. The new view-port was successful, as gas flow across the inside surface of the glass provided a clear view throughout the run.

A total of 16 substrates was coated during the run. One of the substrates was made of a new mullite composition prepared by the Coors Porcelain Company. The rest were McDanel MV20 mullite prepared by the Honeywell Ceramic Center. Melt temperature was held constant during the course of the experiment. The three parameters varied were insertion rate, soak time and withdrawal rate (see Table 1).

The leading edge of about half of the coatings spalled off. The occurrence of spalling did not seem to correlate well with changes made in the time-dependent parameters but rather with the amount of the graphite applied before dipping; i.e., an excess of graphite resulted in spalling. Excess in this case being that which could be easily brushed or wiped off after applying the graphite to the ceramic surface. The structural and semiconductor properties of these films are presently being characterized. A portion of these films will be sent to JPL as per contractual agreement.

Table 1. Coating Parameters (Run No. 50)

Sample	Insert (mm/sec)	Soak (sec)	Withdraw (mm/sec)
MR118	0.50	30	0.5
MR119	0.75	15	0.75
MR120	0.5	30	0.5
MR121	0.75	15	0.75
MR122	0.75	15	0.75
MR123	0.75	15	0.75
MR124	0.75	15	0.75
MR125	0.75	15	0.75
MR126	1.0	45	1.0
MR127	0.75	15	0.75
MR128	1.0	30	0.75
MR129	1.0	45	50.0
MR130	1.0	45	0.75
MR131	3.0	45	2.0
MR132	10.0	15	7.5
MCI ^a	0.75	45	0.75

^a Coors mullite

An unfortunate accident occurred which contaminated the inside of the melt chamber and prevented any further dipping experiments from being conducted during this quarter. However, while the apparatus was being disassembled, the opportunity was taken to revamp the temperature control system and pulling mechanism.

It was decided that a poor impedance match between the Honeywell Dialatrol and the power supply controls was responsible for the unsatisfactory control. That system was discarded in favor of a properly matched one consisting of a Honeywell Deviation Set Point amplifier and a Honeywell Electr-O-Volt controller.

The cable-type dipping mechanism, which did not operate as smoothly as desired, was replaced with a ball screw drive mechanism. Both the temperature control system and the drive mechanism have been satisfactorily used in Czochralski-type crystal growth apparatus used in the Honeywell Research Center for the growth of high-quality optical and electro-optic crystals.

Structural Characterization

The crystallographic texture of silicon on ceramic was determined by x-ray diffraction using the Laue method. Laue shots of individual grains were taken on samples MR45 and MR62. The surface of the coating was found to be predominately (331) with a growth direction of (211). This texture permits a (111) twin plane to occur perpendicular to the substrate and propagate as the grain grows. This texture is similar to that observed in EFG ribbon silicon¹.

The nature of the interface between the silicon coating and the hot-pressed stoichiometric, mullite prepared by American Lava was studied using scanning electron microscopy. Figure 1 is a scanning photomicrograph of the interface which showed extensive separation between the silicon and ceramic. The silicon obviously does not adhere well to the smooth surface of this dense ceramic. No signs of residual graphite or silicon carbide particles could be found at the interface.

Dislocation density of the silicon coating was investigated using the etch pit technique. Figures 2 and 3 are optical photomicrographs of the etched as-grown surface of sample MR114. Note that certain areas between twin boundaries are dislocation free. The dislocation count obtained from this surface was $\sim 9 \times 10^6 \text{ cm}^{-2}$. Figures 4 and 5 show optical photomicrographs of polished and etched cross sections of sample MR114 taken parallel and perpendicular to the pulling direction, the dislocation counts from these two surfaces were $\sim 8 \times 10^6$ and $\sim 6 \times 10^6 \text{ cm}^{-2}$ respectively.

¹ L.C. Garone, C.V. Hari Rao, A.D. Morrison, T. Svek and K.V. Ravi, Appl. Phys. Let. 29, 511 (1976).

Figure 1. SEM micrograph (500X) of silicon-ceramic interface; ceramic (lower portion) is hot-pressed mullite.

Figure 2. Optical micrograph (100X) of etched as-grown surface, sample MR114, showing dislocation etch pits; etch: Dash; time: 2 min, 45 sec.

Figure 3. Micrograph at 500X of same area as Figure 2; dislocation count $\sim 9 \times 10^6 \text{ cm}^{-2}$.

Figure 4. Optical micrograph (500X) of polished and etched cross section of silicon coating, sample MR114, taken parallel to pulling direction; etch: Sirtyl; time: 15 sec; dislocation count $\sim 8 \times 10^6 \text{ cm}^{-2}$.

Figure 5. Optical micrograph (500X) of polished and etched cross section of silicon coating, sample MR114, taken perpendicular to pulling direction; etch: Sirtyl; time: 15 sec; dislocation count $\sim 6 \times 10^6 \text{ cm}^{-2}$.

Substrate Carbonization

The search to find an alternative method of applying the carbon coating to the ceramic continued. Four different graphite coating compounds and one carbon coating compound were purchased from DYLON Industries, Cleveland, Ohio. These coatings are water soluble, have the consistency of latex paint and can be brushed, sprayed or swabbed on according to the manufacturer. The graphite coatings were grades AE, TE, AG and SA. The carbon coating is designated grade DS. The coatings were applied to glass microscope slides, both diluted and undiluted, to assess their thickness, coverage and surface finish. The graphite coatings dried to dull matte finishes and did not cover the surfaces uniformly when diluted with equal amounts of water. The carbon coating dried to a shiny surface and covered well even when diluted with an equal amount of water. The coating thickness and electrical resistivity of these coatings will be measured next quarter.

MATERIAL EVALUATION AND DIODE FABRICATION (D. Zook, T. Schuller, R. Hegel, C. Knudsen, A. Peterson)

Chemical Characterization

During this quarter we received the report on the neutron activation analysis service performed by General Activation Analysis, Inc., of San Diego.

Samples were prepared from the top edge of the melt (first to solidify) for melts 16, 27 and 28, and a multi-element survey was performed. The result was that no impurities were detected in melts 16 and 28, whereas, in sample 27 Mn, Sm, Na, La, Eu and Br were detected at the ppma level, as shown in Figure 6. This finding makes sense since melt 27 was one in which MV20 mullite had been dipped for over an hour. Melt 16 was boron-doped with no dipping, and melt 28 was a contamination check with no boron doping or dipping. The disappointing aspect of this is that the elements of interest, namely Al, B, P, Fe, Ti and V, cannot be detected in Si at the ppma level by this technique.

SILICON SAMPLE 27 FOR J DAVID ZOOK HONEYWELL DEC 1976

ELEMENT	CONCENTRATION (PARTS PER MILLION)	PRECISION (+ OR -)
MN	.092600	.019000
SM	.060300	.012000
NA	.685000	.140000
LA	.051700	.012000
EU	.000912	.000340
BR	.052400	.013000

ELEMENT	UPPER LIMIT (PARTS PER MILLION)	ELEMENT	ELEMENT	ELEMENT			
AG	< 3.500000	FE	< 190.000000	NB	< 1100.000000	SI	<.....
AL	<.....	GA	< .100000	ND	< .990000	SM	<.....
AR	< .340000	GD	< 1.100000	NE	<.....	SN	< 75.000000
AS	< .039000	GE	< 12.000000	NI	< 21.000000	SR	< 3.400000
AU	< .001100	HF	< .140000	O	<.....	TA	< .047000
BA	< 7.200000	HG	< .075000	OS	< .170000	TB	< .030000
BR	<.....	HO	< .014000	P	<.....	TE	< 3.400000
CA	< 5500.000000	I	< 1.400000	PB	< 5900.000000	TH	< .180000
CD	< .670000	IN	< .004100	PD	< .120000	TI	<.....
CE	< .720000	IR	< .001500	PR	< .720000	TL	< 2700.000000
CL	< 2.300000	K	< 5.000000	PT	< .330000	TM	< .100000
CO	< .290000	KR	< 13.000000	RB	< 6.900000	U	< .057000
CR	< 1.700000	LA	<.....	RE	< .009100	V	< 4700.000000
CS	< .350000	LU	< .012000	RH	<.....	W	< .028000
CU	< .120000	MG	< 71000.000000	RU	< 1.600000	XE	< 2.800000
DY	< .250000	MN	<.....	S	<.....	Y	< 480.000000
ER	< .380000	MO	< .530000	SR	< .023000	YB	< .058000
EU	<.....	N	<.....	SC	< .018000	ZN	< 5.100000
F	< 45000.000000	NA	<.....	SE	< .510000	ZR	< 37.000000

..... INDICATES THE UPPER LIMIT COULD NOT BE COMPUTED

GENERAL ACTIVATION ANALYSIS, INC
11575 SORRENTO VALLEY ROAD # 214
SAN DIEGO, CALIFORNIA 92121
PHONE 714/755-5121

Figure 6. Multi-element survey of Melt 27 by neutron activation analysis.

The final report on the ion microprobe work done by McCrone Associates of Chicago, Ill., was also received. In contrast to the preliminary results reported earlier in which Al concentration correlated well with the resistivity and the total exposure time of the melt to the ceramic, the final report showed about the same impurities in two samples differing in resistivity by a factor of six, and in the standard (boron-doped) single-crystal sample from Dow Corning. We regretfully conclude that the early results were fortuitous and that the results are very subject to contamination from handling or from the system.

A one-day visit was made to Applied Research Laboratories in Sunland, Ca., who generously arranged a demonstration of their IMMA and QMAS machines. During this day, analysis of a single-crystal Al-doped sample from Westinghouse (brought by M. Leipold of JPL), a sample of MV20 ceramic, a B-doped single crystal from Honeywell, and samples of MR45 and MR47 were analyzed. The analysis for Al in the QMAS systems turned out to be impossible because of an anomalous lineshape problem that caused the Si 28 channel to give an output in the adjacent Al 27 channel in the ppm range. The impurities C, Ca, Na, Mg, Al, P, K, Ti, and Fe consistently showed up in both the single-crystal control samples and in the SOC samples. The Ti 48 line could actually be an O_3^+ line. Again, the control samples frequently indicated more impurities than the SOC sample.

A day of analysis on SIMS was also donated by Physical Electronics, Inc. Their system uses a quadrupole mass spectrometer to analyze scattered ions. Unfortunately, the sensitivity was not adequate to detect the impurities in our sample.

We conclude that at this stage the IMMA is the only known technique capable of detecting trace impurities in our SOC samples. In the ARL system flatness of the sample did not appear to be a problem. However, the techniques and procedures must be developed to reduce contamination to an absolute minimum. Samples for this analysis should be as large as possible and should be handled an absolute minimum. The samples should be profiled to eliminate surface contamination. In the present case, profiling showed a high surface concentration of Al in all samples. In sputtering the sample some of the sputtered surface material will be deposited on adjacent areas, so that the final analysis should consist of static spot inside a rastered region. We plan to continue with further work on the IMMA system.

An effort was made to purify the ceramic prior to coating with silicon by leaching with concentrated HF, on the hypothesis that the impurities segregate in the glassy (liquid-like) phase of the ceramic during the sintering process. The HF is indeed found to bleach the ceramic to a very white color, and we expected that the iron content of the bleached region would be significantly reduced. However, emission spectrographic analysis (a semiquantitative method) as described in the last quarterly report showed no significant differences in the iron, titanium and vanadium content of the leached and unleached MV20. On the other hand, the EDAX analysis indicated no detectable change in iron but an apparent reduction in titanium and potassium. The latter is not readily detected in emission spectroscopy. The reason for the discrepancy in the Ti analysis is not clear at this time.

EBIC Measurements

Further EBIC measurements were carried out during this quarter, and several problems were identified. The main problem is related to the E-beam charging of an oxide at the surface of some samples which causes an inversion layer, effectively enlarging the diode. It is hoped this can be avoided in point-by-point measurements of EBIC by looking at a virgin area and approaching the diode from a distance. Thus, even if inversion occurs at the point of measurement, these inversion regions are not connected to each other nor to the diode, so that no current is induced in the diode.

Such point-by-point measurements have been made using a Keithley 602 electrometer to measure the current, spending about 30 seconds at each point. Diffusion lengths varying between $6\mu\text{m}$ and $25\mu\text{m}$ have been determined in this way.

One problem pointed out by JPL was that the EBIC image in our first measurements was inadequate. The operational amplifier used in the EBIC mode of the SEM has since been changed. This resulted in a significant improvement in the signal-to-noise ratio, so that the EBIC images can be shown at high contrast. Figure 7 shows the contrast available in a diode that has a fairly low J_{SC} of 12.4 mA/cm^2 . The previous system was capable only of low-contrast images, but, with the new amplifier, considerable structure can be seen in the diode region. It is apparent that some grain boundaries act as recombination centers, and others do not. Most of the features appear only at

(a) Secondary

(b) Medium contrast

(c) High contrast

Figure 7. EBIC images (36X); 23kV, diode R78A-33-4; data taken 2/21/77; $L_D = 6.0$ and $9.0 \mu\text{m}$ measured at right edge.

high contrast. This was verified by a line scan of the video signal using the electrometer and a chart recorder. For the most part, the diodes are quite uniform in EBIC response.

The diode shown in Figure 7 was also used for point-by-point diffusion-length measurements at the right edge, as shown in Figure 8. Although the EBIC current was not stable, readings could be made. Scan A near a dark region of the EBIC image gave a fairly good exponential corresponding to a diffusion length of $6\mu\text{m}$, whereas Scan B near a bright region gave an average diffusion length of $9\mu\text{m}$. In this particular experiment there were no appreciable beam charging effects as previously observed. However, on a subsequent measurement on diodes 7 and 8 on the same substrate, the charging effects were observed. We plan to try to isolate the reason for these.

Spectral Response Measurements

The spectral response of several cells has been measured using a Perkin-Elmer 112 spectrometer and a Xenon lamp source. The short-circuit current of the cells was compared with that of a calibrated silicon UV-enhanced photocell. The measured response shows a falloff in quantum efficiency at long wavelengths ($>0.8\mu\text{m}$) associated with the finite diffusion length. The drop in quantum efficiency at the short wavelength ($<0.45\mu\text{m}$) is due to surface recombination. Thus we expect these measurements to be useful in isolating the reasons for cell performance.

Reflectivity Measurements

To correct for reflectivity losses in calculations of inherent efficiency of solar cells, it is necessary to know the reflectivity of silicon averaged over the solar spectrum. It is therefore of interest to measure reflectivity of our SOC material. For this purpose a Cary 14 spectrophotometer with reflectivity attachment was used. Three samples were measured: (1) a polished wafer with HF etch only; (2) a polished wafer that had been etched for 8 minutes in a 3:2:1; acetic:nitric:HF etch to remove any polishing damage; and (3) a SOC sample (MR107) that had an HF etch only.

Figure 8. EBIC measurements on diode R78A-33-4; the insert shows the scanned region at 360X (reduced to 65 percent of original size for reproduction purposes).

The shape of the reflectivity spectrum between 300nm and 1200nm for all samples was essentially identical. The polished samples had the highest reflectivity, while the etched sample was a factor of 0.983 lower. The SOC samples had an average value that was 0.859 lower than the polished sample. There were slight deviations from proportionality, but these were in a direction to be explained by the fact that there was more scattering by the etched and SOC samples.

In fact, the variations between the samples can be almost certainly attributed to the variations in surface flatness, which causes small angle scattering. An antireflection layer on the sample would reduce the small-angle scattering losses by the same extent as the specular reflection, so we feel the usual assumption of 40 percent reflectivity is applicable to our SOC cells as well as to our comparison (etched) single-crystal cells for calculating inherent efficiency calculations.

Sheet Resistivity Measurements

A simple but important characterization of the sheet silicon is the sheet resistivity, which is the bulk resistivity divided by the thickness. We measure this by the four-point probe method.

An important question is whether the graphite layer under the silicon affects the resistivity measurement. We have previously discussed this question with regard to the rubbed-on graphite coatings. The present discussion serves to include data on the vitreous graphite layers. The results are summarized in Table 2.

Table 2. Typical Carbon Sheet Resistivities

Sheet Type	As Deposited (ohms/□)	After Etching To Remove SOC Layer (ohms/□)
Graphite Rubbed On Rolled Mullite (MV20) ^a	10-25	250-600
Graphite Rubbed On Pressed Mullite (Amer. Lava)	100-150	1K-60K
Vitreous Carbon (Vitregraf) On MV20	2.5-5	2.5-5

^a The thickness of the layer based on weight gain is 7 μ m which would give a sheet resistivity of about 2.5 ohms/□ .

It is clear from the table that the rubbed-on graphite is almost entirely removed by the silicon melt. The amount of graphite depends on the method of preparation and on the smoothness of the ceramic. The vitreous graphite (prepared by Tylan Corp.), on the other hand, is almost wholly intact after contact with the melt, even after one hour of contact with the melt (sample MR78TC). Since the resistivity of the vitreous graphite is only 2 to 5 ohms/□ , it is much lower than the sheet resistance of the p-type silicon layer (50-500 ohms/□), and could seriously affect the sheet resistivity measurement if there is low resistance contact between p-silicon and vitreous graphite. The nature of this contact was therefore investigated and the results are reported in the next section.

Silicon-Carbon Contact Resistance

To measure the current-voltage relationship of the contact between the p-silicon and the vitreous

carbon layer, samples were prepared by selectively etching away the silicon, leaving pads of silicon on the exposed graphite. The geometry was the same as used for the contact resistance measurements discussed below. Current flowed from one pad to another, and the voltage drop between the silicon and the graphite at the edge of the silicon was measured. Typical results are shown in Figure 9.

The resulting I-V characteristics for sample MR78 were quite nonlinear, characterized by a Schottkey diode-like behavior. The slope at zero voltage gave contact resistance values of averaging about 6 ohm-cm^2 . This sample had been in the melt for over an hour and so a rather thick layer of SiC is presumed to have formed.

Sample MR106D had a much shorter time in the melt, about 80 seconds at the top of the SOC layer and about 3 minutes at the bottom. Three contacts were evaluated. A, B, and C had increasing times in the melts and had zero voltage contact resistivities of 0.03, 0.04 and 0.13 ohm-cm^2 , respectively. The former values are quite low, and contacts A and B in particular, were quite linear in their behavior.

These results are particularly encouraging because they indicate that the vitreous carbon can provide an adequate base contact to the p-layer. On the other hand, it means that sheet resistance measurements on these SOC layers can be in error because of shorting by the graphite. In fact, four-point probe measurements of sheet resistivity were made on sample MR106D and were found to vary by a factor of 30 from region to region, with the low readings corresponding to the readings for the graphite. Thus the silicon-carbon electrical contact is not uniform on this sample.

Diode Fabrication

Our procedures for reproducibly fabricating and evaluating solar cells have been improved significantly during this quarter. The effort concentrated mostly on single crystal cells with the goal of improving the solar cell efficiency of cells fabricated in a planar fashion, i.e., both contacts on the top surface as required in our present SOC cells.

(a)

(b)

(c)

SILICON CERAMIC
SILICON ETCHED AWAY TO EXPOSE VITREOUS CARBON LAYER

Figure 9. Silicon-vitreous carbon electrical contact: (a) current-voltage relationship for sample MR78TC which had been in silicon melt 1 hour; (b) sample MR106TC, 2 minutes in melt; (c) four-terminal method measurement. Both (a) and (b) had 10-mA/cm vertical current scale.

A photolithographic process for fabricating 1cm^2 cells having interdigital electrode geometry has not been fully implemented yet. However, the various steps have been tested. A spun-on Kodak 747 microresist is easiest to use, and we have found chemical etches that can be used for the mesa etch operation. We also found that a plasma etch works very nicely and is convenient. A possible process, outlined in Figure 10, uses a final etch to define the mesa. In this way the exposed mesa is not subjected to any high temperature process, namely, sintering of the metallization at 600°C .

Some typical results of uncoated single-crystal cells is presented in Table 3. V_{OC} values as high as 0.55 volt have been obtained with conventional geometry cells and have also been obtained with planar cells using PtSi contacts to the base. Short-circuit currents as high as 29 mA/cm^2 have been obtained, and these numbers are highest with the low-temperature diffusion and with lapped surfaces. The reason for the higher values with lapped surfaces is not clear. It may be due to a lower reflectivity of the surface, or it may be due to a gettering action of the lapped layer. Spectral response measurements may be useful in establishing the reason. The last two cells listed in Table 3 were 1cm^2 in area, were made with a photolithographic process, and had sputtered PtSi contacts to both the p and n regions. The characteristics of PtSi contacts is discussed in the following subsection.

Also during this quarter, aluminum-doped single-crystal cells were prepared from a Czochralski ingot grown here by Bob Hagar. Four diodes made on an Al wafer averaged 9.9 percent conversion efficiency, whereas four cells made from a boron-doped comparison cell averaged 11.1 percent efficiency. Both V_{OC} and J_{SC} were slightly lower in the aluminum-doped wafer. It should be mentioned that both wafers had lapped (1000-grit) front surfaces but had no antireflection coating. The cells had the conventional geometry with a back contact of electroless nickel and a front contact of silver paste. The diffusions were done at 832°C for 20 minutes. The solar cell characteristics were measured with a new setup using a ELH 300W tungsten-iodide slide projection lamp which has a color temperature of 3400K and an internal dichroic reflector which filters out some of the IR. We believe this source should more closely simulate the solar spectrum than the previous system using a flood lamp.

FIRST PHOTORESIST
(PR)

MESA ETCH
DEPOSIT Pt
REMOVE PR
SINTER

RECOAT PR

DEPOSIT METAL
(CONTACT TO n^+
AND PtSi)

THIRD PR

ETCH FINAL MESA
REMOVE PR

Figure 10. Proposed fabrication procedure.

Table 3. Single-Crystal Control Cell Performance (AM1)

Diode No.	Diffusion Temp ($^{\circ}\text{C}$) ^a	Time (min)	Doping	ρ_s (ohms/ $\square$)	V_{OC} (V)	J_{SC} (mA/cm ²)	Fill Factor	Efficiency (%)	Comments
SC36 A	832	20	B	23	0.50	30.8	Poor	Poor	
SC36 B1	832	20	B	23	0.55	25.4	0.66	9.2	
SC36 B2	832	20	B	23	0.55	23.9	0.70	9.2	
SC37 A1	832	20	B	23	0.54	22.2	Poor		Electroless nickel top base contact
SC38 C1	828	20	B	20	0.55	21.8	0.713	8.6	
SC39 A2	830	15	B	25	0.51	29.4	0.51	7.8	Top e-Ni, top base contact
SC40 A2	832	60	B	14	0.53	26.1	0.525	7.3	
SC42 A2	832	20	A1		0.51	27.2	0.73	10.2	Al-doped base
SC42 B3	832	20	B		0.53	29.1	0.72	11.2	
SC42 C2	832	23	B		0.54	25.7	0.59	8.2	Polished surface
SC41 C2	829	20	A1	26	0.52	22.3	0.73	8.5	
SC44-02	966-1017	14	B		0.53	23.8	0.64	8.0	1cm ² cells made with PtSi contacts, etched surfaces
SC44-04	966-1017	14	B		0.54	21.4	0.71	8.3	

^a The diffusion temperatures listed are probably too low by about 70 $^{\circ}\text{C}$ due to a faulty thermocouple.

Contact Resistance Measurements

Contact resistance has been a problem for two reasons: (1) lack of low contact resistance has resulted in poor cell performance, and (2) in a cell design with top contacts to the base region the base contacts must be small in area and therefore must have low contact resistivity. The definition and measurement of contact resistivity is not always straight-forward, as pointed out by Berger.² It is convenient experimentally to measure contact resistance using a planar resistor, which complicates the analysis since the current density is not uniform (see Figure 11). We have used both circular geometry and linear geometries to measure contact resistance (Figure 11c and d). Our technique is somewhat different than the techniques described for planar diffused resistors² because our samples are much larger, and we can use tungsten probes to measure voltage at a point using a high-impedance (1000-megohm) buffer amplifier.

Measurements were first made on electroless nickel (e-Ni) contacts using various geometries. We found that, in some of the photodiodes using e-Ni, the contact's resistance to the p-type base was quite nonlinear and variable. Sputtered nickel was more reproducible if sintered at least at 450°C but gave contact resistivities of 0.3 ohm-cm² or greater, and were nonlinear.

We discussed our contact problems to the p-type silicon with various people at Honeywell's Solid State Electronic Center, and they suggested the use of platinum silicide (PtSi) or palladium silicide (PdSi) as a contact material. These materials are formed by sputtering the metal and sintering at temperatures in the range of 500°C.

We had a platinum sputtering target on hand and found that PtSi contacts were easy to produce in a reproducible manner on silicon with various surface finishes. We found that the annular geometry (Figure 11c) gave values of V_2 much less than V_1 , showing that the current density was quite nonuniform. We therefore proceeded to make resistors with a planar linear geometry (Figure 11d). We found that, even with fairly narrow contacts, the voltages V_1 and V_2 were not equal so that the current density was not uniform. On the other hand, the wafer was not sufficiently thin to use the transmission line model. A simple assumption is that the current density varies exponentially across the contact, which gives the expression for contact resistivity.

²"Contact Resistance and Contact Resistivity," H.H. Berger, J. Electrochem. Soc. 119, 507 (April 1972).

Figure 11. Definition and measurement of contact resistivity: (a) definition in terms of uniform current flow; (b) measurement by annulus on one side and uniform current on other side; (c) measurement with planar annular geometry; (d) measurement with planar linear geometry - only one contact shown.

$$P_c = \frac{V_1 - V_2}{I} \frac{dw}{\ln(V_2/V_1)}$$

This expression reduces to the correct form when the current is uniform and agrees with the TML model when $V_1 \gg V_2$, and therefore represents an approximate expression for contact resistivity. Using this approximation the contact resistivity of PtSi to 3-ohm-cm p-type silicon was found to be about 0.03 ohm-cm². This compares to values of 0.001 to 0.003 ohm-cm² in the literature.²

SOC Photodiode Measurements

During this quarter, SOC photodiodes were evaluated which had been fabricated on the MV20 and American Lava mullite substrates coated with rubbed-on graphite, and on the MV20 substrates coated with vitreous carbon (Vitregraf). For example, two SOC cells were fabricated on the pressed American Lava mullite substrates which were large, covering many grains. Because of the large size and the high base resistance of the base material, there was a sizeable series resistance, so that the value of I_{sc} could not be determined in the usual manner. However, the value of I_{sc} could still be determined by two techniques. The simplest way is to continue to trace the I-V characteristic into the negative voltage region. A four-terminal method was also used by placing tungsten point probes on the n⁺ and p regions adjacent to the junction to measure the time voltage drop across the junction. High-impedance (10⁹-ohm) op-amps were used to follow the voltage because of the high impedance of the tungsten probes.

Several SOC diodes were made from sample MR78TC. This was the first dipped MV20 mullite substrate that had been coated with vitreous graphite from Tylan Corporation. The substrate was exposed to the silicon melt for over an hour. The raw data from these diodes is summarized in Table 4. Diodes R78D-42-1 through -6 used the low-temperature shallow diffusion which gave the highest J_{sc} and n values for the single-crystal cells. The table shows that these SOC diodes also had high J_{sc} values with an average of 20.3 mA/cm², and uncorrected efficiencies as high as 6.46 percent. It is notable and encouraging that diodes R78D-42-4 and -5 had dimensions on the

Table 4. Summary of SOC Diode Data at 100 mW/cm²

Diode	Diffusion		Area (cm ²)	J _{SC} (mA/cm ²)	V _{OC} (V)	Fill Factor	Efficiency (%)	Comment
	Time (Min)	Temp (°C)						
R73A-33-1	10	964	0.0628	12.82	0.450	0.721	4.11	
-2	10	964	0.00825	16.61	0.444	0.668	4.89	
-3	10	964	0.00505	17.13	0.439	0.592	4.41	
-4	10	964	0.0152	12.41	0.449	0.717	3.96	
-5	10	964	0.00508	13.47	0.451	0.701	4.29	
-6	10	964	0.00383	14.70	0.449	0.720	4.74	
-7	10	964	0.0202	14.48	0.465	0.709	4.78	
-8	10	964	0.00383	18.04	0.449	0.726	5.89	
R78C-36-1	10	964	0.0142	29.22*	0.432	0.537	6.78	
-2	10	964	0.0285	22.84	0.407	0.473	4.39	
R78D-42-1	20	832	0.00995	19.90	0.472	0.655	6.15	0.9cm cross grain 1.0cm along grains
-2	20	832	0.00828	20.89	0.472	0.616	6.08	
-3	20	832	0.00710	19.18	0.472	0.693	6.27	
-4	20	832	0.0856	20.44	0.445	0.401	3.65	
-5	20	832	0.08805	19.82	0.444	0.6	5.44	
-6	20	832	0.020	21.75	0.443	0.670	6.46	

NOTE: The melt was boron-doped giving a base resistivity of 2.0 to 2.5 ohm-cm.

* The I_{SC} of this diode measured differently at different times and the value of J_{SC} given here may not be correct.

order of 0.1cm^2 with the former having a length of 0.9cm across the grains, and the latter having a length of 1cm along the grains. The poorer efficiency of these two cells is due to the lower fill factors which are sensitive to contact resistivity and geometry. The inherent efficiency curves of two of the diodes are shown in Figure 12 and 13, and are about 12 percent using the 40 percent reflectivity value.

The performance of these cells is particularly encouraging. The results indicate that solar cell performance is strongly related to melt contamination from the mullite, and that the vitreous graphite is quite effective in passivating the ceramic and preventing contamination.

Several 1cm^2 SOC cells were made during this period using photolithographic process and PtSi contacts. Only one turned out to have high series resistance due to a poor base contact. This is the first time we have not gotten good contact with PtSi, and we don't expect the problem to reoccur. At any rate, the I-V characteristic shows that the J_{SC} should be about 17 mA/cm^2 . The I-V characteristics were also measured before the PtSi contacts were sintered, and J_{SC} was about the same, but V_{OC} was only 0.3 volt. In any case, if a normal fill factor of 0.7 were assumed, the efficiency would have been 4.75 percent, and the inherent efficiency would have been about 8 percent. This is encouraging since this substrate did not have the vitreous carbon coating, although it did have many large grain areas.

Figure 12. Current-voltage measurements, diode R78C-36-2; lower: measured; upper: corrected.

Figure 13. Current-voltage measurements, diode R78C-42-6; lower: measured; upper: corrected.

SUBSTRATE CHARACTERIZATION (B.G. Koepke, R.B. Maciolek, S.J. Marquardt, and M. Smeltzley)

Comparison of Microstructures of Coors S1SI and McDanel MV20 Mullite Ceramic

Coors' refractory ceramic designated S1SI has a composition close to McDanel MV20 refractory extensively used to date as substrates for this program. Both compositions contain 52 to 55 percent alumina. Eleven substrates were received from Coors and are under evaluation as candidate substrate material. In this section we compare the microstructures of both materials.

An optical micrograph of McDanel MV20 mullite is shown in Figure 14. The microstructure has been revealed by relief polishing for 2 1/2 hours on a Vibromet* polisher using No. 3 alumina on Microcloth* and then etching for 15 seconds in Sirtyl** etch. The dark, continuous background phase is glass, and the light regions are mullite crystallites. An optical micrograph of Coors SiSI mullite is shown in Figure 15. Both samples were prepared in the same way. By comparison the S1SI exhibited less glassy phase and possibly less porosity. Density measurements will have to be performed on both to confirm that the Coors mullite is less dense. From a thermal shock standpoint, a decrease in porosity increases the tendency for thermal fracture. As noted elsewhere in this report, the one Coors substrate that was dipped in molten Si did not crack.

Characterization of Acid-Leached MV20 Mullite

In an effort to eliminate some of the impurities indigneous to mullite, a number of pieces of a mullite substrate were immersed in HF. The HF, of course, dissolved the glass phase leaving the mullite crystallites exposed. In Figure 16 (a) we show a scanning electron micrograph of a fractured cross section of a mullite substrate that had been immersed in HF until about half the total cross

* Buehler Inc.

**50gm CrO₃

100 ml H₂O

75ml HF

Figure 14. Optical micrograph (325X) of McDanel MV20 mullite refractory, specimen MR114.

Figure 15. Optical micrograph (325X) of Coors S1SI mullite refractory, specimen MC1.

(a) Sample at 20X

(b) Region at base of
leached zone (2100X)

(c) Region near base of
leached zone (5300X)

Figure 16. Scanning electron micrographs of a fractured surface of an MV20 sample that had been immersed in HF to leach the glass phase to a depth of approximately one-third the specimen thickness.

section had been leached by the acid. A higher-magnification photo of the interface region at the bottom of the leached layer is shown in Figure 16(b), while a still higher magnification photo is shown in Figure 16(c). These micrographs illustrate nicely the acicular morphology of the mullite crystallites that precipitated during firing. The structure appears to contain only the continuous glass phase and the mullite needles. Knowledge of the morphology of the mullite can aid in determinations of the volume percentage of mullite made from measurements on optical micrographs such as those shown in Figures 14 and 15.

The results of EDAX analyses of regions in the center and at the edge of the leached sample are shown in Figures 17 and 18 respectively. They show two things. First the Al/Si ratio increases drastically, as expected, upon removal of the glass. Secondly, the K, Ti and FE are all lower in the leached regions.

The leached region is considerably weaker than the core and may be removed with some difficulty by scratching with a knife. On the other hand the impurities in mullite refractory are concentrated in the glassy phase, and, by leaching it out, one can separate the glass phase from the surface of the substrate by a controlled distance. We will carbon coat and dip a leached substrate in order to evaluate if leaching noticeably lowers the impurities in the silicon coating.

Confirmation Etch Pit-Dislocation Relation

To confirm that the etch pits observed on polished and etched cross sections of the silicon coating were associated with dislocations, an attempt was made to fracture the silicon and etch matching surfaces. If the pits observed on one fracture surface are mirror images of those observed on the matching surface, the pits correspond to dislocation etch pits.

Although some of the pits coincide, the general agreement is poor. Before deciding whether the test is possible, we will attempt this rather difficult procedure on a few more specimens. In one case the SEM will be used to compensate for the shallow depth of field experienced with optical microscopy.

Figure 17. Results of EDAX analysis on unleached region in center of specimen.

Figure 18. Results of EDAX analysis on leached region at outer edge of specimen.

CONTINUOUS COATING FACILITY (J.D. Heaps, C.D. Butler, L.D. Nelson)

Continuing SOC material evaluations and solar cell studies make it increasingly evident that impurities, resulting from substrate dissolution, play a major role in limiting minority carrier life-time in the silicon coatings. This is particularly evident after several substrates have been dip-coated and the melt has become progressively contaminated. A number of ways have been considered for minimizing this contamination problem, one of which includes developing a silicon coating technique which reduces the contact area of the substrate with molten silicon. A new SOC coating facility is being designed and constructed which will coat larger substrates in a continuous manner. It is generally agreed that this facility must exhibit sufficient versatility to accept and coat 10cm x 100cm substrates that are most likely to be less than perfect with respect to their flatness and perhaps even to their thickness. Likewise it would be desirable to construct a facility with enough flexibility to accommodate exploring more than one coating technique (i.e., vertical, horizontal and angle coating) with a minimum of change-over time involved.

The simplest method is to pass a horizontal substrate (carbonized face down) over a meniscus of molten silicon. Such a method would make the facility more straightforward to design and would more easily accommodate nonflat substrates. Thus the new facility will be designed around this concept, employing sufficient flexibility to accommodate other coating techniques with a minimum of modifications. We choose to call this conceptual coating method SCIM (Silicon Coating by Inferior Meniscus). With this method, graphite-coated ceramic substrates are passed over a silicon-filled side arm of a crucible containing molten silicon (see Figure 19). The level of the molten silicon is adjusted so that the surface of the liquid silicon bulges up above the walls of the side arm. The path that the substrate takes over the side arm is such that it comes in contact with the molten silicon but does not touch the walls of the side arm.

Figure 19. Silicon coating by inferior meniscus.

Design of the inert-gas-filled enclosure and the mechanism which will convey the substrates through the preheating and coating furnaces has been completed. Construction of this portion of the facility is presently under way. This inert-gas-filled enclosure consists of a box that will contain the furnaces and water-cooled heat shields. Attached to the opposite sides of the box are side arms which will contain chain conveyors. These will carry the substrates to, through and from the coating process. To minimize contamination, these chains will contact the surface of the substrate only along the outer quarter of an inch and will not contact that portion of the substrate which is in the hot zone. Such a method should be suitable for large-scale production. Initially about a half dozen substrates will be loaded into a rack within one of the side arms before flushing the enclosure with an inert gas. When the enclosure has been flushed and the silicon melt is at the proper temperature the substrates will be placed on the conveyor chain and sent through the coater. The coated substrates can then be taken off the chain conveyor and placed in a rack within the other side arm until after furnace shutdown. Provisions have been made for tilting the whole SCIM apparatus through about ± 30 degrees. This is in case we find some orientation other than level that results in better crystal growth on the substrate. Larger angles will require modification of the support frame. At this point we have no reason to expect that any orientation other than level will be required. The enclosure for the SCIM apparatus is large enough to accommodate sub-

strates 12 inches wide by one meter long. The substrates will enter and leave the furnace area through slots in the water-cooled heat shields. A method for replenishing the silicon melt will be designed into the facility.

Because the contact area of the substrate with molten silicon will be reduced, the substrate is not likely to contaminate the melt as rapidly as when dip coated. Continuous-coating machines also offer the following process and cost advantages:

- The eliminate substrate dipping and soaking time.
- They should require a less sophisticated temperature control system since the substrate uniformly contacts the melt.
- They utilize less-expensive, smaller-size melt containers than a single dip-coating machine would.
- They are more adaptable to longer substrates, should there be a cost advantage in using same.
- They could be designed to accept unfired substrate material, thereby reducing operator and energy costs.
- They should, by virtue of their size and number, be less expensive and more manageable to maintain.

In an effort to test the feasibility of this SCIM concept the experimental setup shown in Figure 20 was constructed for use with the existing dip-coating facility. A graphite cylinder was fabricated to fit within the heating element. The semicircular substrate was bonded to the dip-coating facility's pulling rod. A trough-shaped quartz piece contains the molten silicon and additional silicon can be added to this trough by lowering a silicon rod into the container until the silicon's surface tension provides an adequate meniscus. The substrate is lowered to contact the graphite cylinder and then is slowly rotated over the silicon meniscus.

Solidification should occur when the substrate ceases to be in contact with either the molten silicon or the graphite cylinder. Admittedly the outer circumference of the substrate should have a faster

Figure 20. Experimental coating test setup for a horizontally oriented substrate.

growth rate, but the experiment should indicate the possibilities and/or problems associated with this concept.

The above experiment was attempted with disastrous results. The silicon container was mistakenly filled with a small ingot of mercury selenide. The experiment, needless to say, thoroughly contaminated the entire dip coating facility. The facility has since been completely disassembled and all metal parts thoroughly cleaned. All furnace parts are being replaced, and reassembly is very near completed. The experiment will be repeated, using silicon this time, "we hope."

Pending the results of the above experiment, a second technique which more nearly resembles the principle of dip-coating may be tried. The substrate would be vertically coated as shown in Figure 21. Again a graphite cylinder is fabricated to fit within the heating element. This cylinder will subsequently be cut into four pieces A, B, C and D as shown. The carbonized substrate will be held snugly against the coating arm by a wedge-shaped section of the graphite cylinder. The silicon melt level will be predetermined, and the substrate will be raised with an offset pulling rod. This test should demonstrate whether or not the substrate adequately contains the molten silicon and if the solidification is similar to that of dip coated substrates.

Work continues on the design of the furnace portion of the continuous coating facility, and known parts and materials have been ordered.

ECONOMIC ANALYSIS (S. Schuldt, R. Winter)

An attempt has been made to model the economics of a large-scale facility for coating ceramic panels with silicon. Following the lead of other companies in the program who have already contributed economic analyses, we chose to set up an economic structure which identifies major categories and subgroupings of cost factors. To each of these factors is assigned, either directly or indirectly, a numerical value which contributes in some way to the price which the customer will pay for the product. Up to this point the primary emphasis has been placed on completeness of structure rather than accurate assessment of numerical values. To this end, the economic model is formulated as a computer subroutine with some of the required numbers supplied from the main program as independent variables.

Figure 21. Cross-sectional view of vertical-growth experimental test setup.

A partial cost breakdown, through the first two levels of the hierarchy, is as follows:

- Capital installation, including amortization and debt interest—
 - Building
 - Production equipment
 - Plant equipment
- Materials and electric power—
 - Ceramic substrate
 - Polysilicon
 - Carbon
 - Argon
 - Power
- Direct labor —
 - Production
 - Engineering
- Burden —
 - Indirect labor and salaries
 - Supplies
 - Services
 - Department management and production planning
 - Allocation based on headcount, wages, and salaries
 - Other allocations
- General and administrative
- Profit

The primary output of the model is price per square meter of silicon-coated ceramic. Parameters of the model are in three categories - independent variables, soft constants, and hard constants.

The independent variables, already mentioned as being passed to the model from the main program, are so designated mainly for the purpose of doing sensitivity studies. These quantities are both

critical and difficult to assign fixed numbers to. Having chosen tentative values, it is instructive therefore to calculate the incremental effects due to each of them upon the total cost. Independent variables include unit costs as those of silicon, ceramic substrate, and ceramic coating machines. Other independent variables, such as the linear coating (pulling) rate, ceramic thickness, and (Si) coating thickness have important indirect effects on costs. For example, the pulling rate determines the number of coating machines required to produce a given annual quota, and therefore affects both labor and capital costs.

The soft constants are handled as data internal to the subroutine but may be charged as warranted by updated information. These include process yield factor, plant efficiency, thermal loss factor, argon loss factor, labor and burden rates, certain capital costs, and interest rate.

The hard constants are the physical densities, specific heats, and Si heat of fusion.

A first iteration based on best available parameter estimates yielded a price of about \$11 per square meter, including profit. In this determination, the major cost items were poly Si (\$2.90 per square meter), labor and burden (\$2.50 per square meter), and the ceramic substrate (\$2.50 per square meter). A pulling rate of 1 cm/sec was assumed. The added value, excluding poly Si cost, is \$8.35 per square meter. The burden rates taken for this calculation represent a somewhat different production situation and are not necessarily realistic for the silicon coating operation.

CONCLUSIONS

During this past quarter, the following conclusions have been reached:

- The problem of electrical contact to SOC solar cells, though more difficult than contacting to conventional cells, is not insurmountable, and cells made with both geometries can have comparable performance.
- Platinum silicide appears to offer the lowest contact resistance to p-silicon.
- Aluminum is comparable to boron as a p-type base dopant for solar cells.
- Vitreous carbon coatings have resulted in the highest-performance SOC solar cells to date, presumably due to this material's action in inhibiting dissolution of the melt.
- Coors' S1SI mullite appears to be acceptable as a substrate for coating with silicon.
- The silicon-vitreous carbon electrical contact, though highly nonuniform, can be low-resistance and should be investigated as a back-contact material.
- Mullite that has been leached with HF has a very white appearance and appears to have had some reduction in impurity content.

RECOMMENDATIONS

It is recommended that in addition to the present effort, further effort should be made in the following areas:

- **The SOC solar cells, including the contact resistance and electrode resistance, should be modeled with the goal of demonstrating an optimized cell design.**
- **Increased effort should be made to determine the variables and the ultimate cost of vitreous graphite coatings on ceramic.**
- **The potential of vitreous carbon as a base contact should be investigated. The possibility of doping the carbon coating with boron or aluminum should also be investigated.**
- **Low cost junction and contact formation processes for fabricating SOC cells should be investigated.**

NEW TECHNOLOGY

A surprising result of our measurements of the silicon-vitreous carbon interface is that the electrical resistance between the two can be quite low if the contact time is sufficiently short. Since the vitreous carbon coatings can have quite low sheet resistance (2 to 5 ohms/ $\square$), they could contribute significantly to the reduction of series resistance. Carbon is basically a low-cost material and could thus provide a cost-effective means of contacting the silicon.

The uniformity of the contact is certainly a problem, even when the contact time is kept low. Further effort is needed to isolate the reasons for the variations and to minimize them.

PROJECTED ACTIVITIES FOR NEXT QUARTER

In the dip-coating experiments planned for the next quarter, emphasis will be placed on three items of concern: (1) impurity control, (2) morphology control, and (3) increased coating rate.

Impurity pickup by the silicon coating will be minimized by utilizing higher-purity substrates, the use of "impervious" graphite coatings such as Vitre-Graf, and by the manner in which the substrate is dipped; i.e., minimize the time and amount of ceramic surface in contact with the molten silicon.

Control of the growth morphology of the coating will be studied by correlating changes in grain size, twinning, and dislocation density with changes in growth rate, melt temperature, graphite coating thickness and type, and thermal coefficient of expansion of the substrate material. In particular more substrates made of Coors mullite and substrates coating with DYLON coatings will be dipped.

Attempts will be made to increase the growth rate by creating a steep, linear temperature gradient above the melt through the use of cooling blocks and/or gas jets.

We will continue to determine microstructure and densities of past and present substrates. These observations will then be correlated with both the appearance and structure of the silicon layers. We anticipate that a facility for measuring thermal shock resistance of substrates dipped in molten silicon will be finished, and some measurements will have been completed. A fracture mechanics technique to measure the adhesion of the silicon layer to the substrate has been devised and will be tested during the next quarter.

The potential of IMMA for detecting impurities in SOC layers and for looking at segregation of impurities at grain boundaries and at dislocations will be investigated further. Spectral response measurements and/or SPV measurements will be measured and related to solar cell fabrication and performance. Cells will be made on a routine basis using photolithographic processes, PtSi contacts, and geometry which should yield good fill factors.

Coating concepts will be experimentally investigated using the dip-coat facility in an effort to adopt the best technique for the continuous coating. Also the work will continue on the construction of the new facility, and the final design will be completed.

The economic analysis will be run for a variety of input factors, and a sensitivity analysis will be performed.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 22, 23, and 24.

NOTE: IN ADDITION TO THE ABOVE PROGRAM PLAN, THE HONEYWELL CORPORATE RESEARCH CENTER WILL PROVIDE THE REQUIRED DOCUMENTATION, ATTEND THE REQUIRED MEETINGS AND DELIVER THE REQUIRED SAMPLES AS PER CONTRACT AGREEMENT.

△ PLANNED GOALS
▲ ACCOMPLISHED GOALS

Figure 22. Updated program plan.

Figure 23. Updated program labor summary.

Figure 24. Updated program cost summary.