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SILICON-ON-CERAMIC COATING PROCESS

Silicon Sheet Growth Development for the Large-Area Silicon Sheet and
Cell Development Tasks of the Low-Cost Silicon Solar Array Project

Quarterly Report No. 9, March 29—June 30, 1978

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July 21, 1978
Date Published

Work Performed Under Contract No. NAS-7-100-954356

Honeywell Corporate Material Sciences Center
Bloomington, Minnesota

U.S. Department of Energy

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Solar Energy

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The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, by agreement between NASA and DOE.

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SUMMARY

The objective of this research program is to investigate the technical and economic, feasibility of producing solar-cell-quality sheet silicon. We hope to do this by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

Beginning the middle of February 1978, we expanded our program to include activities funded by the Task VI Cell Development Group of the Low-Cost Silicon Solar Array (LSSA) program at the Jet Propulsion Laboratory. This work is directed toward the solution of unique cell processing/design problems encountered within the silicon-on-ceramic (SOC) material due to its intimate contact with the ceramic substrate. Beginning this quarter, we will issue two separate quarterly reports. One will report on progress of the total effort; the other will identify the activities specifically funded by the Cell Development Group. The Cell Development Quarterly Report will be a replication of cell development information contained within the total Task II and Task VI Quarterly Report.

During the past quarter, we demonstrated significant progress in several areas:

- The continuous (SCIM) coater developed a silicon meniscus in the coating trough allowing silicon to contact a ceramic and a graphite substrate. These were very poor "coatings" but did represent the first operation of the SCIM coater with respect to silicon contacting a substrate.
- Our best slotted-cell performance (electrical contact on back side of slotted ceramic substrate) increased from 4.3 percent (uncoated) to 6.4 percent (uncoated) on a 2-cm² cell.
- We have developed a detailed theoretical analysis of our growth process which determines the key control parameters necessary for maximizing growth speed and grain size while maintaining the necessary coating thickness.

Results and accomplishments during the quarter can be summarized as follows:

- Different ceramic substrate processing techniques (e.g., dry pressing; tape process) were found to have no effect on the substrate suitability for silicon coating.

- Many Coors substrates of S1SI compositions were dipped. Performance was satisfactory.
- Ceramic substrate bodies with thermal expansion coefficients approaching that of silicon were obtained. The few that were dipped appear to coat as well as the McDanel MV20 body.
- Coors and Honeywell are both processing slotted substrates of various configurations. These have been dipped and processed into cells.
- One hundred fifty substrates were dip coated during this quarter.
- Excellent dip coatings were obtained on substrates with slot widths of 0.5 mm spaced on 1-mm centers.
- Problems concerning SiO and SiO₂ formation on dipped layers were uncovered and solved.
- Cells processed on MV20 and S1SI slotted substrates exhibited shunt resistance problems due to cracking of the silicon layer. This was determined to be caused by the mismatch in thermal expansion coefficients between these bodies and the silicon. The new lower-expansion-coefficient mullite obtained from Coors should eliminate this problem.
- The new experimental coater is scheduled for completion by 1 August 1978.
- The SCIM coater runs made during this quarter were unsuccessful in providing uniform silicon coatings. A silicon meniscus in the coating trough was obtained, however, and more complete thermal control of the various zones was obtained.
- SOC cell performance has shown an increase due, in part, to the incorporation of a new cleaning procedure and a modified diffusion process.
- A metallization adhesion problem of the top contact to the silicon occurred during this quarter which curtailed our cell processing. This problem was related to incomplete oxide removal and has subsequently been solved.
- A photomicrograph revealed change in the microstructure of the dipped silicon layer at the edge of the slot on slotted substrates. The effect of this on cell performance has not been determined.

- Three different methods have been used to make the "stripe" SOC cells necessary for fabrication of the high-voltage cell structure. These will be evaluated next quarter.
- The first plastic concentrators for the integral optical coupler structure were completed but proved unsatisfactory because of rough reflecting surfaces.
- Glassy-carbon layers can act effectively as "wetting" agents and diffusion sources for silicon. We have not demonstrated that they have adequate erosion resistance and impermeability to act as an effective conductive interface.

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INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 12 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous coating process also being investigated have excellent scale-up potential which offers an outstanding cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and the rate at which the substrate is withdrawn from the melt.

The solar-cell potential of this SOC sheet silicon is promising. To date, solar cells with areas from 1 to 10 cm^2 have been fabricated from material with an as-grown surface. Recently, an antireflection (AR) coating has been applied to our SOC cells. Conversion efficiencies greater than 9 percent have been achieved without optimizing series resistance characteristics. Such cells typically have open-circuit voltages and short-circuit current densities of 0.51 V and 20 mA/cm^2 , respectively.

The SOC solar cell is unique in that its total area is limited only by device design considerations. Because it is on an insulating substrate, special consideration must be given to electrical contact to the base region. To date, this has been done using an interdigital

electrode pattern. One method which offers considerable promise is to place small slots in the substrate parallel to the crystalline growth direction and contact the base region by metalizing the silicon that is exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing. Initial cell results indicate a 4.3 percent conversion efficiency (no AR coating) on a 5-cm² cell. This cell was not optimized for device performance. During the quarter, we demonstrated 6.4 percent conversion efficiency (uncoated) on a 2-cm² slotted cell.

Development efforts are continuing in such areas as improvement in growth rate, reduction of progressive melt contamination, and optimization of electrical contacts to the base layer of the cell. The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The impurities from the substrate are believed to adversely affect solar-cell conversion efficiency. A special type of graphite coating on the substrate has shown a potential for inhibiting this dissolution of mullite. Should these coatings prove to satisfactorily isolate the substrate from the melt in a cost-effective manner, improved solar-cell performance should be attained. An alternate method for reducing substrate dissolution is to reduce the contact area the substrate makes with the silicon melt. Therefore, a silicon coating facility has been constructed which is designed to coat large (10-cm x 100-cm) substrates in a continuous manner. It is expected that this new facility will not only improve the growth rate, but also minimize the silicon melt contact with the substrate. This should reduce the rate at which the melt becomes contaminated. This new facility will also permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process.

TECHNICAL DISCUSSION

SUBSTRATE DEVELOPMENT AND CHARACTERIZATION (B. Koepke)

At the end of the last quarter, the substrate development efforts at the Corporate Material Sciences Center (CMSC) were mainly concerned with characterization of various mullite-based ceramic substrates produced by the Honeywell Ceramics Center and by Coors Porcelain Co. To date, the substrates from the Honeywell Ceramics Center have been used in the majority of the dip-coat runs. These substrates are produced from McDanel MV20 mullite by rolling, drying, and firing. Coors has been dry-pressing and firing substrates with varying compositions in an effort to optimize the compatibility of the substrate with the silicon coating process. The "base" composition in the experimental series is a Coors mullite designated S1SI. The alumina-silica ratios of McDanel MV20 and Coors S1SI are 1.20 and 1.48, respectively. The results obtained on dip-coated Coors substrates are discussed in this section. Not enough runs have been made to allow valid comparisons between all the Coors compositions but some qualitative statements can be made.

In addition to producing small dip-coating substrates, both the Ceramics Center and Coors have been developing methods to produce large (10-cm x 1-m) substrates for the SCIM continuous coater. The Ceramics Center has produced large substrates by rolling, drying, and firing McDanel MV20 mullite and Coors has produced large S1SI substrates by a continuous tape process. Small samples of S1SI produced by the tape process have been successfully dip coated and there appears to be no difference between this material and that produced by dry pressing.

During the quarter, most of the efforts in substrate development were concerned with the production of slotted substrates at the Ceramics Center and at Coors, and the development, at Coors, of a new series of substrate compositions with better thermal properties than those produced previously. The mechanical properties and thermal shock resistance of these materials have not been measured yet at CMSC but thermal expansion data have been obtained from Coors and are reported in this section.

In what follows, we discuss first the results of the dip-coat runs made on the Coors substrates. Results on the new substrate compositions are then covered and, finally, the slotted substrate development is discussed.

Dip-Coat Runs On Coors Substrates

The initial eight compositions of mullite-based substrates received from Coors were described in the 2nd Annual Report and are listed in Table 1 for review.

Table 1. Coors Experimental Mullite Compositions

Letter Code	Material	Al_2O_3/SiO_2	α (R. T. to 1000°C)
A	Standard S1SI mullite	1.48	0.520
B	High-mullite modification	2.14	0.485
C	High-silica modification	1.17	0.480
D	Boric acid added to lower thermal expansion of glass phase	1.48	0.535
E	High-porosity modification	1.48	0.525
F	High-purity modification	1.52	0.510
G	Sintered electrically-fused mullite and silica powders	3.54	0.530
H	S1SI fired in a reducing atmosphere to produce a porous body containing carbon	1.48	0.515
	McDanel MV20	1.2	0.495
	Silicon	-	0.38

For comparison purposes, note that the C Mod material from Coors most closely matches the McDanel MV20. To date, a total of 48 Coors substrates have been dip coated. Data concerning these substrates are listed in Table 2. The type of carbon coating (H = hand-rubbed, D = Dag, V = vitreous), melt temperature, pull rate, and substrate and coating thickness are listed to indicate if correlations between these quantities exist. The values of coating thickness listed in Table 2 are averages taken over the surface of the substrate with a micrometer. Data from the few Coors substrates that have been processed into solar cells at this time are also included. Most of the substrates dipped were of the S1SI composition. Only 14 of the substrates made from the experimental materials have been dipped. Since the substrates were all approximately 3.2 mm (0.125 in.) thick, a correlation between substrate thickness and coating thickness could not be made. With the limited data available, there was no obvious relation between pull rate and coating thickness. The highest efficiency (no AR coating) of a solar cell made on a Coors substrate is 6.83 percent. Due to the paucity of cells processed on Coors substrates, comparison with cells processed on MV20 substrates is not possible.

Table 2. Summary of Data on Dip-Coated Coors Substrates

Material	Number	Carbon Coating	Melt Temp. (C°)	Pull Rate (in./sec.)	Substrate Thickness (in.)	Coating Thickness (in.)	V _{oc} (volts)	J _{sc} (mA/cm ²)	Eff. (%)	Active Area (cm ²)	Comments
SiSi	594-CH	H	1432	0.02	0.116	0.005					
	70-3CX	D	1435	0.03	0.079	0.008					
	72-3CX	D	1440	0.05	0.110	---					
	72-4CX	D	1430	0.05	0.084	0.010					
	92-2CAX	D	1435	0.05	0.126	0.002					
	93-1CAX	D	1438	0.05	0.123	---					
	93-2CAX	D	1438	0.025	0.125	0.012					
	93-4CAX	D	1438	0.025	---	*					
	93-5CAX	D	1438	0.025	0.124	0.007	0.405	14.6	2.39	2.9	Shattered on second dip. Dipped twice. Part of coating spalled off. Coating spalled off. Seeded, portions not coated.
	94-1CAX	D	1430	0.05	0.126	---					
	94-4CAX	D	1430	0.015	0.126	0.029					
	94-5CAX	D	1430	0.04	0.125	0.003					
	94-6CAX	D	1430	0.05	0.126	0.004					
	104-2CAH	H	1438	0.05	0.126	0.009	0.472	21.0	5.85	0.08	Seeded, uniform coating. Rough, uneven coating. Uneven coating. Seeded.
	104-3CAH	H	1438	0.05	0.124	0.002	0.477	20.5	5.93	0.08	
	104-4CAX	D	1438	0.05	0.126	0.006					
	104-5CAH	H	1438	0.05	0.124	0.002					
	104-9CAH	H	1438	0.05	0.125	0.005	0.488	22.2	6.83	0.08	Uniform coating. Uniform coating over 1/3 of substrate.
	104-12CAV	V	1438	0.05	0.127	---					
	104-13CAH	H	1438	0.05	0.124	0.006					
	104-16CBH	H	1438	0.05	---	*					
	105-5CAH	H	1440	0.05	0.125	0.008					
	106-3CAV	V	1435	0.05	0.124	0.002					
	107-2CAH	H	1444	0.1	0.124	0.004					
	107-4CAH	H	1444	0.05	0.124	---	0.484	18.0	5.45	0.08	Dipped twice, uniform coating. Excellent coating.
	107-6CAH	H	1444	0.05	0.124	*					
	107-8CAH	H	1444	0.05	0.124	0.002					
	107-10CAH	H	1444	0.05	0.125	0.002					
	108-3CAH	H	1442	0.05	0.125	*					
	108-10CAV	V	1434	0.05	0.124	---					
	109-9CAV	V	1440	0.05	0.122	0.003					
	109-14CH	H	1440	0.05	0.040	0.008					
	114-7CAV	V	1437	---	0.124	---					
	114-9CAV	V	1437	0.035	0.124	---					
B Mod	91-14CBX	D	1442	0.05	0.128	---					
	91-15CBX	D	1442	0.05	0.124	0.003					
	92-5CBX	D	1435	0.15	0.124	0.003					
	104-16CBH	H	1438	0.05	---	*					
	105-6CBH	H	1440	0.05	---	*					
C Mod	These bodies have not been tested to date.										
D Mod	91-16CDX	D	1442	0.05	0.126	0.003					
	105-7CDH	H	1440	0.05	0.126	---	0.44E	16.2	3.41	1.05	Coating chips off easily. Uniform coating.
E Mod	91-17CEX	D	1442	0.05	0.122	0.004					
	92-4CEX	D	1435	0.05	0.122	---					
	105-5CEH	H	1440	0.05	---	*					
F Mod	92-1CFX	D	1435	0.05	0.128	0.001					
	105-9CFH	H	1440	0.05	---	---					
G Mod	91-13CGX	D	1442	---	0.127	*					
	105-10CGH	H	1440	0.05	---	*					

*Specimen not available for measurement.

A few comments can be made concerning the few substrates from the experimental series of compositions that were dipped. The only composition that did not survive the thermal shock during dipping was the electrically-fused material (G Mod) as reported in Quarterly Report No. 7. Since this material also had one of the higher thermal expansion coefficients, the lower thermal shock resistance is not surprising. One of the corners of a B Mod substrate with a high mullite content cracked during dip coating. The thermal expansion of this material is not excessively high but the glass content is comparatively low. Boric acid was added to the D Mod material to decrease the thermal expansion coefficient by converting the glass phase to a lower-expansion borosilicate glass. The attempt was unsuccessful and the expansion of the D Mod material was one of the highest measured (2nd Annual Report). Two D Mod substrates were dipped under approximately identical conditions. Both substrates had uniform, but thin coatings and a cell was fabricated on one of them. The electrical characteristics of the cell were poor. The coatings on most of the experimental Coors substrates have been observed to at least partly spall off. Our feeling is that this is due more to the Dag coating than to the properties of the various substrates. Many more of these substrates would have to be coated before this point could be verified. Although not apparent from Table 2, the coatings on the Coors substrates were, in general, thinner than those on the MV20 substrates (Quarterly Report No. 8). This is attributed to a greater temperature gradient at the solid-liquid interface of the thinner (2 mm) MV20 substrates. The effect of substrate thickness on growth conditions will be systematically studied during the next quarter in the new dip-coating apparatus described in a later section of this report. The C Mod series of substrates were recently shipped from Coors and will be characterized with respect to thermal and mechanical properties and will be dipped during the next quarter. As noted above, these substrates should coat in a similar manner to the MV20 substrates.

Coors Experimental Low-Expansion Compositions

As mentioned in Quarterly Report No. 8, Coors has developed a new series of experimental substrate compositions with thermal expansion coefficients that are closer to silicon than any previous substrate compositions. The compositions are based on the S1SI material and the thermal expansion is lowered by adding naturally occurring fused silica to the S1SI before firing. The thermal expansions of these materials are shown in Figure 1 as a function of the excess silica added to the S1SI. The thermal expansion decreases continuously with silica additions and appears to cross that of silicon at about 30 percent excess silica. Coors has also produced a body with 60-percent fused mullite and 40-percent fused silica that, as shown in the figure, has a thermal expansion less than that of silicon.

During the past quarter, we obtained some samples of these materials and a few were dip coated. The coating data on these substrates are summarized in Table 3. All carbon

Figure 1. Thermal Expansion of S1S1 Mullite Containing Excess Silica

Table 3. Summary of Coating Data on Coors High-Silica Substrates

Material	Number	Melt Temp (C°)	Pull Rate (cm/sec)	Substrate Thickness (in.)	Coating Thickness (in.)	Comments
60% Mullite, 40% Mullite	127-9S	1442	0.04	0.075	0.016	Substrate partially coated. Carbon coating difficult to apply on rough surface.
S1S1	129-7CH	1437	0.06	0.055	0.006	Sample coated but growth was dendritic.
S1S1 + 15% Silica	129-5CH	1437	0.06	0.055	0.004	Sample coated but growth was dendritic.
S1S1 + 27.5% Silica	129-6CH	1437	0.04	0.056	≈ 0.020	Good coating but uneven in thickness.

coatings were applied by hand-rubbing graphite on the substrates. In every case, the lower-expansion substrates survived the dipping process. The fused-mullite/fused-silica bodies were overfired and had rough surfaces. As a result, the hand-rubbed graphite coating could not be applied evenly. This was probably the reason the coating did not cover the whole substrate. In future runs, the substrates will be surface-ground before carbon coating to verify this point. The only comment that can be made at this time concerning the SISI/fused-silica substrates is that they all survived the dipping process. The onset of dendritic growth during this series of runs was unfortunate and comparisons of coating quality cannot be made. Decreasing the pull rate eliminated the dendrites and produced a good, but very thick, coating. During the next quarter, more substrates with these promising compositions will be dipped and will be processed into cells.

Slotted Substrate Development

The development of slotted substrates is being carried out simultaneously at CMSC, the Honeywell Ceramics Center, and at Coors. Efforts at the Ceramics Center have been concerned with slotting MV20 substrates in the green and in the bisque-fired states. The green substrates are slotted with a stylus and a template after rolling. The other technique involves machining the slots into bisqued substrates before final firing. The substrates are bisqued at the Ceramics Center, machined at CMSC, and final-fired at the Ceramics Center. A number of MV20 substrates slotted by both techniques were dipped and processed into cells during the quarter. The performance of these cells is reported in a later section of this report.

A new Super Kanthal electric kiln has been installed at CMSC and is now available to fire substrates. The kiln will be used both to final-fire bisqued substrates containing machined slot patterns and to refire substrates to purify them before dipping.

A number of slotted SISI substrates were received from Coors that were produced from tape and from pressed bodies. Examples of these slotted substrates are shown in Figure 2. The longer substrates are the pressed bodies. In both materials, the slots were cut with an abrasive wheel after bisque firing. The nonuniform shrinkage during firing, particularly in the substrates produced from rolled tape, is attributed to the slots.

A standard slotted substrate design has been arrived at CMSC, and workers at Coors are currently setting up to produce the pattern by a die-cutting process. The substrate design will have 1-mm-wide slots on 4-mm centers. The slot pattern will be square to allow both horizontal and vertical slot patterns to be investigated. Slotted substrates

with three compositions (S1SI, S1SI plus 20 percent excess silica, and S1SI plus 30 percent excess silica) and two thicknesses (1.4 mm and 2.4 mm) will be supplied by Coors.

Figure 2. Slotted Substrates Produced at Coors from Dry-Pressed (Top Row) and Rolled-Tape (Bottom Row) Bodies

SHEET SILICON GROWTH (J. D. Heaps, B. Koepke, L. D. Nelson, D. J. Sauve, K. Wouri, and H. Burke)

Dip-Coat Processing

With limited exceptions, the dip-coating runs during the quarter were generally restricted to satisfying the material needs for solar cell fabrication and evaluation. This restricted usage of the dip coater is in the interest of maintaining a high purity level within the system.

A total of about 150 substrates were silicon coated. Most of these coatings were made on a wide variety of slotted substrates. The present coating technique minimizes thermal shock by positioning the substrate just above the surface of the melt for 1 minute before and after dip coating. By doing so, substrate breakage has been virtually eliminated.

During the quarter, excessive SiO gradually appeared on the surface of dip-coated silicon layers. Occasionally, some coatings would also have a trace of SiO₂. The accumulation of SiO takes place as the substrate is being withdrawn from the melt and can be limited to a degree by the manner in which the argon gas is admitted and exhausted from the coating chamber. This accumulation also appears to be sensitive to the flow rate of the gas and to the pressure of the atmosphere within the chamber. A number of runs were made where the above parameters were varied, but none of the changes that were made had any lasting effect on eliminating the accumulation of SiO. As the summer season approached, the appearance of SiO₂ became more prevalent. This suggested that the increasingly higher relative humidity may be the source of the problem. To minimize this problem, the following measures were taken:

- 1) The carbon-coated substrates were baked out prior to being dip coated with silicon. This measure was taken to drive off any moisture which may have collected in the pores of the carbon coating and/or the substrate.
- 2) During dip-coating runs the system evacuation time was prolonged during the warmup period of the coater's heating element. This measure also was adopted to allow sufficient time to evacuate any moisture trapped in the pores of the coater's internal parts.
- 3) The commercial-grade argon gas normally used was replaced by a cylinder of higher-purity liquid argon.

At least the first two of the above measures played a significant role in eliminating the SiO₂ problem and in minimizing the SiO accumulation.

Among the slotted substrates coated were some where the slots were machined into bisque-fired MV20 substrates prior to the final high-temperature firing. On these particular substrates, slots of various widths and spacings were represented. Slot spacings with 2.5-mm centers were successfully coated without breakage. A variety of slotted substrates from Coors Porcelain Co. were also successfully dip coated. These substrates included vertically- and horizontally-oriented slots of varying widths and centers. Most impressive were the excellent silicon coatings obtained on substrates with slot widths of 0.5 mm spaced 1.0 mm on centers. The results of numerous coatings strongly indicate that superior silicon layers are obtained when the slots are oriented perpendicular to the growth axis. In regions on an individual substrate where the slots were oriented parallel to the growth axis, the silicon coating was recessed above each slot. On the other hand, where the slots were oriented perpendicularly, there was no observable manifestation of this recessing. The results further suggested that there is no

fundamental problem related to the silicon coating process which would prohibit the use of slotted substrates as a means of electrically contacting the base layer of a solar cell.

To evaluate the effect of the p-type doping level in silicon coatings, it is important that layers of various doping levels be grown under identical conditions. To achieve this, 15 silicon layers having various doping levels were coated during a single run.

This was done by attaching, as required, additional boron doping pills to substrates yet to be coated. The pills were attached to the substrate using a small droplet of Dag. The substrate was then dipped approximately 2 mm into the melt, allowing the pill to melt and become a homogeneous mixture before the dipping operation was continued. The results of this study are reported in the Material Evaluation section.

Two of Coors 60-percent fused mullite, 40-percent silica substrates were also dip coated during the month. They survived the dipping but did not coat uniformly. There appeared to be more reaction than usual between the substrate and the molten silicon, possibly due to a breakdown of the SiO_2 content in the substrate. This assumption is supported by the heavier-than-usual deposit of SiO at the top of the substrate. These substrates, however, were overfired by Coors, causing blistering on the surface, which made it extremely difficult to carbonize the substrate by the "rub-on" method. This poorer-than-usual substrate carbonization would have also contributed to the nonuniformity of the coatings. More of these particular substrates will be dipped using a Dag carbon coating to determine whether or not more-uniform silicon coatings can be obtained on these substrates.

More recently, Honeywell's Ceramic Center has been busy developing its version of mullite compositions that can be rolled or pressed into substrate form. Two substrates made from Ceramic Center compositions were dip coated. One substrate, which was shaped by the Ceramic Center's rolling technique, coated satisfactorily with a smooth, uniform silicon layer. The second substrate, which was pressed from a different composition, produced a spotty, nonuniform layer. Further evaluation of these compositions will be performed when the experimental dip coater is operational.

During the reporting period, the silicon melt was positioned 5 mm higher within the heating element. This resulted in somewhat thicker layers for a given pull rate. During the next quarter, the position of this melt will be further elevated, with the objective of achieving 100- μm -thick layers at a pulling rate of 0.1 cm/sec.

Experimental Dip Coater

An experimental dip-coating facility is being designed to study the supported growth of silicon-on-ceramic substrates. The major goal of the effort is to define the optimum conditions necessary to grow reasonably thick (i.e., 100- μ m) films at high rates (i.e., 0.15 to 0.3 cm/sec). The design of the experimental dip coater closely resembles that of the existing coater, with a few major exceptions. The new coater will be larger to allow more access to the vicinity of the liquid-solid interface and to allow afterheaters to be used. Our initial attempts to improve the growth rate while maintaining a film of reasonable thickness will involve the use of cold fingers to increase the temperature gradient at the liquid-solid interface.

The design of the facility, with the exception of the cold fingers, is complete and all components are either finished, under order, or are under construction. The main stainless-steel chamber is being fabricated by an outside vendor and will be finished in the last week of July. The pulling apparatus and the frame to hold the chamber are finished. The carbon resistance heaters are in-house. Current design efforts are directed at the cooling shoes to extract heat immediately above the liquid-solid interface. We plan on using water or gas-cooled nickel plates containing gas jets to cool the silicon coating and substrate.

The facility should become operational during the next quarter and growth experiments should be underway by the end of the quarter.

Continuous Coating Process

As discussed in Quarterly Report No. 8, the method initially used by the continuous (SCIM) coater for heating the large (10-cm x 100-cm) substrates resulted in their breakage. This was caused by the large thermal gradient in the warmup path through which the substrate passed. During the reporting period, preheaters and postheaters were designed to remedy this problem and the preheater has been installed. A lateral and longitudinal thermal profile of the modified system was taken and will be discussed later in the report.

Adding the preheater to the SCIM coater required extensive alteration of the system. In the interest of keeping the coater operational so that we could pursue solutions for other coating problems, parts for the preheaters and postheaters were fabricated in kit fashion. This approach reduced the down time while the preheater was being installed. During the time kit parts were being assembled, several operational runs were made. From these runs the following observations were made:

- 1) As experienced with the dip coater, after a prolonged period of time a crust of SiO condenses around the periphery of the silicon crucible. In the SCIM coater this crust also forms a ring around the quartz displacer. If the diameter of the displacer is too large, after a period of time the crust on the crucible combines with the crust on the displacer and the mobility of the displacer is lost; a smaller displacer solved this problem.
- 2) Applications of a Dag film to the coating trough is not a reliable method for causing molten silicon to wet and flow along the trough. The principal problem results from separation of the Dag film from the trough causing discontinuity. Placing a thin graphite plank in the trough was considered, but once molten silicon fills the trough the undissolved portion of the graphite plank will float to the surface of the silicon.
- 3) One method for causing molten silicon to flow along the trough is to fill the trough with solid silicon. This assures the operator that the trough is up to temperature before he displaces the molten silicon.
- 4) Once the trough is full of molten silicon, a meniscus of considerable height (6 to 8 mm) can be achieved. This meniscus is very visible from the side viewing port and its height can be adjusted using the displacer. The initial version of the quartz crucible/trough piece restricted the flow of silicon at the mouth of the trough. This restriction was removed and the silicon flow was improved.

In one of the operational runs, a graphite substrate was passed over the silicon meniscus. Wetting occurred as expected, but this particular graphite was unusually porous and the coating soaked up a considerable amount of silicon. Solidification of this coating took place 2 or 3 cm downstream from the center of the meniscus. This could be easily seen through the side viewing port where a thick film of molten silicon was observed dangling from the bottom surface of the graphite substrate.

In other operational runs, an attempt was made to silicon coat smaller (approximately 8-cm x 10-cm) mullite substrates. The attempts were for the most part unsuccessful from a coating point of view, but they did reveal a need for additional temperature profiling to establish the temperature conditions required for a successful coating procedure. In all of the runs, a silicon meniscus was achieved in the coating trough. As previously pointed out, this was more easily accomplished after the mouth of the quartz trough was modified to remove a minor restriction to the flow of molten silicon.

One run failed when the substrate softened because of an excessively high substrate heater temperature. The substrate consequently sagged, preventing it from being passed over the meniscus. In a subsequent run, the substrate was below the melting point of silicon, causing the meniscus to solidify as the substrate came into contact with it. An effort to remelt the silicon was abandoned after reaching a heating-element temperature considered unreasonably high.

In the following run, the substrate was successfully passed over the silicon meniscus wetting the substrate, but, as with the graphite substrate, solidification did not occur sufficiently near to the trough and the layer built up in thickness to where it came into contact with the heated graphite part beneath it.

Because these smaller substrates were located near the quartz trough during the entire warmup period, a large amount of SiO collected on their carbonized face. This undoubtedly inhibited uniform wetting on the one substrate we were successful in passing over the meniscus.

To prevent substrate breakage, a method was developed to modify the temperature profile of the SCIM coater. See Figure 3. A dual-walled insulated preheater compartment is nonthermally attached to a modified wall of the water-cooled heat baffle which surrounds the coating chamber. A long rectangular graphite tube or tunnel extends from the coating compartment in to the preheater compartment. This two-piece graphite tube can be easily separated to rearrange guides for various substrate widths. One end of this tube is heated by the upper and lower substrate heaters. Midway in the preheater compartment the upper half of this tube passes by a temperature- and position-adjustable resistance heating element. See Figure 4. The function of this additional heater is to trim the temperature profile. This long graphite tube serves the purpose of providing a longer, more gradual temperature gradient. Because it completely surrounds the substrate, the edges of the substrate can no longer radiate their energy to the cold walls of the system. To accommodate this modification, the substrate conveyor chain was re-located 4 in. further from the coating compartment. By doing so, this stainless-steel mechanism will never experience a temperature greater than 600°C.

A temperature profile of this newly installed preheater was taken using shrouded Type R platinum + platinum-rhodium thermocouples (TCs). Three side-by-side TCs were used so that the lateral temperature profile could also be measured. These TCs were attached to the conveyor chain so that they could be made to traverse the entire length of the preheater and coating zones of the system. The temperatures of these zones were measured in 0.5-in. increments. Each time the TCs were moved, sufficient time was allowed for them to reach thermal equilibrium before the temperatures were recorded.

Figure 3. Cross-Sectional View of Modified Substrate Preheater

Figure 4. Cross-Sectional View Looking into the Preheater Compartment as Viewed from the Coating Chamber

The results of the center thermocouple's longitudinal temperature profile is shown in Figure 5. It is immediately apparent that substantial modification is needed before mul-lite substrates can be suitably coated with silicon. As shown, the substrate reaches a maximum temperature about 2.5 in. before it passes over the silicon meniscus, and this maximum temperature would be about 120°C above the melting point of silicon. This could explain why the substrate in a previous run softened and sagged prior to reaching the silicon meniscus.

Figures 6, 7, and 8 show the longitudinal profile results of all three (left-center-right) TCs. Data from these three graphs are plotted as isotherms in Figure 9. This plot also demonstrates the need for improvement in lateral temperature uniformity. The plot shows that the cooler portion of the rectangular graphite tube has reasonably good lateral temperature uniformity but that the high-temperature end is very nonuniform, with a hot spot occurring in the center region. To improve this nonuniformity, a modified substrate heater has been ordered which is designed to surround the graphite tube on three of its four sides (see Figure 10). By doing so, the edges of the graphite tube will also be heated.

To correct, as needed, the longitudinal temperature profile, the following measures will be or have been taken:

- 1) The system's thermal flexibility has been improved by powering the substrate's upper and lower heaters with separate power supplies. (They were previously electrically series-connected and powered by one supply.) The additional supply previously was to be used to power an afterheater that has never been used and is not likely ever to be used. This power supply change has been made and performs satisfactorily.
- 2) At the suggestion of our contract monitor, Dr. Martin H. Leipold, an array of thermocouples is being assembled on a large (10-cm x 66-cm) mul-lite plate. By inserting this thermocouple plate into the coater, longitudinal and lateral temperature profiles can be routinely taken in a quick and efficient manner. It is believed that by use of this technique the electrical resistance in appropriate regions of the various graphite heating elements can be altered to effect the needed temperature profiles.
- 3) The offset crucible-trough configuration, discussed in a previous report, will be installed in the system. This will locate the molten silicon meniscus adjacent to the designated solidification zone.

Figure 5. Longitudinal Temperature Profile of Center Thermocouple in Relation to Coater Parts

Figure 6. Longitudinal Temperature Profile of Left-Hand-Side Thermocouple

Figure 7. Longitudinal Temperature Profile of Center Thermocouple

Figure 8. Longitudinal Temperature Profile of Right-Hand-Side Thermocouple

Figure 9. Temperature Isotherms in Relation to Coater Parts

Figure 10. Cross-Sectional View Showing the Temperature Graduation Tube's Position Relative to the Upper and Modified Lower Substrate Heating Elements

- 4) If required, cooling shoes will also be installed in this zone in place of this "never used" afterheater.

Before any further effort is made to silicon coat substrates, appropriate temperature profiles must be achieved. The attainment of these profiles, plus the addition of our recently acquired temperature controllers, will be the objective of our immediate effort.

MATERIAL EVALUATION (D. Zook and B. Grung)

Auger electron spectroscopy was used to examine several problems associated with the fabrication of SOC cells. One problem was the presence of an inadvertent antireflection (AR) coating on some cells. That is, a few cells had a black appearance after processing. Auger analysis demonstrated that the black coating was an approximately 250-Å-thick layer consisting of oxygen and silicon (the exact stoichiometry was not determined). It is probable that the layer was SiO_2 . In the top 80 Å of the inadvertent coating, several contaminants were found: indium, fluorine, sodium, aluminum, and carbon. The first came from the indium solder; the rest, from the various cleaning fluids. The inadvertent AR coating has not been observed on recent solar cells; consequently, we have not determined the exact source of this potential problem.

A second problem was the fact that some samples had a yellowish appearance in various regions. Auger analysis demonstrated that the yellow color was due to small particles consisting of oxygen and silicon. Again, the exact stoichiometry was not determined, but it is probable that the particles are SiO_2 , rather than SiO . The particles are about 5 µm wide (See Figure 11). The density of particles was greater on some grains of silicon than on others. The higher the density the more the surface appeared yellow.

The small particles were apparently deposited on the silicon surface during the growth process. The steps taken to eliminate these deposits are described in the coating section of this report.

IMPROVEMENT OF FABRICATION TECHNIQUES (TASK VI) (B. Grung, D. Zook, T. Heisler, R. Hegel, S. Znameroski)

The performance of recent SOC cells has been improved by using a new cleaning procedure and by modifying the diffusion process. These two improvements were suggested by Gene Daszko of Honeywell's Solid State Electronics Center and by Wiley Smith of the University of Minnesota.

- a. Shows the small particle on the as-grown surface and illustrates the selectively adherence to the surface. Optical microscope, 200X.

- b. Shows the SEM photo of a similar region at 500X. Note the fine lines emanating from each particle.

Figure 11. Photographs of Small Particles on As-Grown SOC Silicon Surfaces

The new cleaning procedure is used before the high-temperature (approximately 850°C) phosphorus diffusion. The objective of the procedure is to eliminate four possible contaminants from the silicon surfaces. First, SiO_2 is removed by using a 10:1 etch ($\text{H}_2\text{O}:\text{HF}$). Second, SiO is removed by scrubbing the surface with a cotton swab dipped in deionized water. Third, organic compounds are removed by using hot H_2SO_4 . Finally, heavy-metal ions are removed by using hot aqua regia. After this cleaning procedure, the SOC material is heated for 10 min. at 120°C in flowing N_2 . This evaporates any residual cleaning liquids from the SOC material.

The modifications of the diffusion process were as follows: First, quartz wool was packed around the ends of the diffusion tube. This produced a more uniform temperature profile inside the tube. Second, the baffle was removed from the source end of the tube. A baffle often improves the uniformity of results; however, it proved to be unnecessary. It should be noted here that it is usually better to setup the diffusion furnace without using a baffle and then to add it later if necessary. Third, the various flow rates were changed as shown in Table 4.

Table 4. Gas Flow Rate (cc/min.)

Gas	Old	New
N_2	2700	3500
O_2	124	35
$\text{N}_2 + 1\% \text{PH}_3$	1160	525

After these improvements were incorporated, five 3-in.-dia. single-crystal test wafers were processed. The average sheet resistance of each wafer was within the range from 37 to 39 $\Omega/\square$. This result represents exceptional uniformity for our system. In subsequent processing, the average sheet resistance of an SOC cell was within the range from 43 to 52 $\Omega/\square$. Thus, for the same diffusion conditions, the sheet resistance of an SOC cell is about 10 $\Omega/\square$ greater than that of a single-crystal cell. This is due primarily to the polycrystalline nature of the SOC material.

SUMMARY OF CELL PERFORMANCE (Task II and Task VI) (B. Grung, R. Hegel, and T. Heisler)

The solar cell and photodiode performance of nonslotted substrates is summarized in Table 5. Corresponding results for slotted substrates and for substrates coated with glassy (vitreous) carbon are given in Tables 6 and 9, respectively. All cells made by the unmodified diffusion process are identified by a P in the diode number; the new diffusion process described above is identified with a Q. The dipping of the base layer was verified from 6×10^{15} to 3×10^{16} boron atoms/cc.

Table 5. Summary of Cell and Diode Performance

Diode	Base ρ_s ($\Omega/\square$)	N_A (10^{16}cm^{-3})	No. of Diodes (avg.)	Active area (cm^2)	ρ_s ($\Omega/\square$)	V_{oc} (volts)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (%)	Max. Eff.* (%)	Comments
104-18A-P30	42-94	0.6	6	0.068	66	0.51	19.6	0.732	7.3	7.9	Omit 1 - Visual defect
104-18B-P30-0	42-94	0.6	1	1.05	66	0.50	17.5	0.626	5.5	5.5	
104-18B-P30	42-94	0.6	7	0.078	66	0.51	20.3	0.731	7.5	8.0	
104-18C-P30	42-94	0.6	1	1.05	66	0.49	18.4	0.635	5.7	5.7	
105-4A-P30	36-111	1.2	7	0.078	66	0.48	20.1	0.649	6.4	7.6	
105-4A-P30-0	36-111	1.2	1	1.05	66	0.48	17.6	0.522	4.4	4.4	
106-6A-P30	68-159	1.2	1	2.77	72	0.51	20.8	0.607	6.5	6.5	
106-6B-P30	68-159	1.2	1	1.05	72	0.50	19.5	0.619	6.0	6.0	
106-6C-P30	68-159	1.2	7	0.078	72	0.50	20.4	0.699	7.2	7.5	
107-4A-P28	159-254	2.3	7	0.078	58	0.48	17.9	0.626	5.4	5.4	V. Carbon
107-4A-P28-0	159-254	2.3	1	2.77	58	0.51	19.0	0.585	5.6	5.6	
107-7A-P28	29-105	2.3	1	2.77	68	0.48	15.7	0.506	3.8	3.8	
107-7C-P28	29-105	2.3	6	0.082	68	0.50	19.8	0.642	6.3	6.3	
107-9A-P30	51-193	2.3	1	2.77	67	0.51	17.8	0.650	5.9	5.9	
107-9B-P30	51-193	2.3	1	1.05	67	0.47	17.0	0.624	5.0	5.0	
108-15A-P27	8-17	1.2	1	2.77	60	0.47	21.2	0.360	3.6	3.6	V. Carbon
108-15B-P27	8-17	1.2	1	1.05	60	0.40	18.5	0.322	2.4	2.4	V. Carbon (Damaged)
108-15C-P27	8-17	1.2	7	0.078	60	0.47	20.2	0.625	6.2	6.2	
112-1A-P31	302-616	0	1	2.77	58	0.46	22.2	0.283	2.9	2.9	Omit 1 - Inconsistent
112-1B-P31	302-616	0	1	1.05	58	0.46	21.8	0.365	3.6	3.6	
112-3A-P31	96-267	0.6	1	2.77	59	0.48	19.4	0.486	4.6	4.6	
112-3B-P31	96-267	0.6	1	1.05	59	0.49	19.5	0.619	6.0	6.0	
112-3C-P31	96-267	0.6	6	0.082	59	0.48	21.4	0.635	6.6	7.2	
112-5A-Q2	40-150	1.2	1	2.8	48	0.49	17.4	0.66	6.0	6.0	
112-5B-Q2	40-150	1.2	1	1.05	48	0.50	17.8	0.66	5.9	5.9	
112-5C-Q2	40-150	1.2	7	0.05	48	0.50	19.1	0.72	6.7	7.3	
112-7A-P31	44-206	1.8	1	1.38	54	0.50	19.9	0.597	6.0	6.0	
112-7B-P31	44-206	1.8	1	1.38	54	0.50	19.9	0.597	6.0	6.0	
112-10A-Q3	45-91	2.3	1	2.8	44	0.51	17.0	0.66	5.7	5.7	
112-10B-Q3	45-91	2.3	1	1.05	44	0.51	15.6	0.72	5.7	5.7	
112-10C-Q3	45-91	2.3	7	0.05	44	0.51	17.7	0.72	6.5	6.8	
112-12A-P31	43-111	2.9	1	2.77	61	0.51	18.1	0.566	5.2	5.2	
112-12C-P31	43-111	2.9	1	1.05	61	0.46	15.8	0.528	3.9	3.9	
112-14A-Q2	33-87	2.9	1	2.8	48	0.51	16.1	0.66	5.5	5.5	
112-14B-Q2	33-87	2.9	1	1.05	48	0.57	16.7	0.71	6.0	6.0	
112-14C-Q2	33-87	2.9	7	0.05	48	0.50	16.6	0.73	6.1	6.4	
P-29A			1	13.06	33	0.56	27.6	0.531	8.1	8.1	Single-crystal
P29B			1	13.06	34	0.56	26.9	0.575	8.6	8.6	
P-28			1	1.05	---	0.54	24.9	0.595	8.0	8.0	
P-30A, B, C			5	1.05	55	0.55	25.2	0.678	9.4	10.0	
P-31B			1	1.05	51	0.54	25.5	0.660	8.7	8.7	
P-31E			1	1.05	45	0.55	25.1	0.687	9.0	9.0	
Q1			1	1.05	41	0.54	23.6	0.67	8.5	8.4	
Q2			1	1.05	42	0.53	23.8	0.62	7.8	7.8	
Q3			1	1.05	43	0.53	22.3	0.68	8.0	8.0	

*Uncoated.

Table 5 shows that, on the average, there is a decrease in the short-circuit current, J_{sc} , an increase in the fill factor, FF, and a slight increase in the open-circuit voltage V_{oc} , with increased doping. Figure 12 shows the (active-area) conversion efficiencies values as a function of base doping levels. This figure does not clearly indicate an optimum doping level for the SOC material and, as a result, further experiments will be required to determine the effects of doping variations.

The modified diffusion process gives less variation in the cell performance, although it has not resulted so far in a noticeable improvement in efficiency.

SLOTTED CELL DEVELOPMENT (Task II and Task VI) (B. Grung and T. Heisler)

Twenty-five slotted substrates were dip coated during June. Included were substrates from Coors and from the Honeywell Ceramics Center. The resulting SOC material demonstrates the following:

- 1) Silicon can easily bridge across wide slots. Typical slot dimensions were 1 cm long by 1 mm wide.
- 2) The silicon surfaces on the slotted substrates were nearly as smooth as those on non-slotted substrates. Horizontal slots perturbed the surface less than vertical slots.
- 3) The distance between slots can approach the width of the slots. For several substrates, the slots were 1 mm wide on 1.5-mm centers (i.e., the intervening ceramic material was 1 mm wide).

Figure 13 shows a cross section of one of the slotted substrates. The silicon layer was grown at 0.04 cm/sec and was 250 μm thick, which is about 100 μm thicker than usually obtained, but serves to illustrate many of the features of SOC. In the left-hand portion of the micrograph we see the usual SOC structure 1 grain thick, having many twin boundaries running perpendicular to the substrate and surface. Small particles of silicon carbide can be seen at the silicon-mullite interface. Note that the surface of the silicon over the slot is smooth and that the silicon fills the slot only slightly (the slots on this sample were not carbonized). Also note the change in microstructure that occurs at the edge of the slot. The relationship between such structure and the growth conditions, as well as the effects of this change in structure on the electrical properties of solar cells, is presently under investigation. It is significant that the extent of slot filling can be controlled through the application of the carbon coating.

Figure 12. Conversion Efficiencies of SOC Cells versus Base Doping Levels

Figure 13. Photomicrograph of a Cross Section of a Slotted Substrate, Taken Perpendicular to the Growth Direction and Slot Length

The electrical evaluation of slotted cells has been delayed somewhat by the metallization problem described later in this report. So far, 24 slotted cells have been completed and tested; however, the metallization on most of these cells did not adhere properly. The best slotted cell so far had an (active-area) conversion efficiency of 6.4 percent. This cell did not use an AR coating. Figure 14 shows the current - voltage characteristics of this slotted cell, which had a total area of 2.3 cm^2 . Figure 15 shows the corresponding characteristics of a (0.045-cm^2) photodiode fabricated adjacent to the slotted cell. The primary characteristics of the slotted cell and the photodiode are listed in Table 6.

Compared with the photodiode cell, the slotted cell has: 1) an identical open-circuit voltage, 2) a slightly larger short-circuit current, 3) a much lower fill factor, and 4) a lower conversion efficiency. The low fill factor is due to the effects of both shunt and series resistances.

The shunt resistance is the result of small cracks which developed in the silicon during processing. At the present time we do not know exactly when or how these cracks were formed; however, they are a potential problem associated with the slotted substrate approach. The cracks were discovered as follows: One cell was divided into two parts by cutting the metal lines and by plasma-etching through the n^+ emitter region. Detrimental shunting effects were observed for one half but not the other. This indicated that

Figure 14. Current - Voltage Dark Characteristics of Slotted Substrate SOC Cell

Figure 15. Current - Voltage Characteristics of SOC Photodiode on Slotted Substrate

the shunting effects were associated with localized regions. Close inspection of the half cell with shunting effects revealed a small crack.

Table 6. Slotted Cell and Photodiode Performance

Device	Active Area (cm ²)	V _{oc} (volts)	J _{sc} (mA/cm ²)	Fill Factor	Eff. (%)
Slotted Cell	1.9	0.52	20.7	0.59	6.4
Photodiode	0.045	0.52	19.3	0.76	7.7

NOVEL DEVICE DEVELOPMENT (Task VI) (B. Grung and S. Znameroski)

The fabrication of the high-voltage cell has been delayed somewhat by the metallization problem. However, we have investigated three methods for making the required silicon stripes. The first involves chemical etching; the second, sandblasting; and the third, carbon patterns on the ceramic before dipping in silicon. Each method has some advantages and some disadvantages.

For the (chemical) etching method, black wax is used to define the silicon pattern. The exposed silicon is then etched using CP4. The wax is removed using ether as a solvent. The junction is then diffused into the silicon.

For the sandblasting method, the junction is diffused first. Then, tape is used to define the silicon pattern and the exposed silicon is removed using a sandblaster. The tape is removed using acetone, alcohol, and deionized water.

For the third - or "carbon" - method, the silicon stripes are formed as follows: The silicon pattern is defined by using tape on the ceramic substrate. Carbon is applied to the exposed substrate regions and the tape is then removed. The substrate is dipped in silicon. The silicon adheres only to the regions that are covered with carbon. The junction is then diffused.

A comparison of the three methods indicates the following: 1) Larger grain sizes are possible using the etching or sandblasting methods. For the carbon method, the grain size is somewhat reduced as a result of the growth conditions in the narrow stripes. 2) Closer stripes are possible using the sandblasting method. For the etching method, CP4 typically undercuts the wax. This prevents accurate control of the dimensions of the silicon pattern. For the carbon method, the silicon typically will bridge across the carbon regions if these regions are less than 2 mm apart. 3) Better junction characteristics

are possible using the sandblasting method. For this method, the junctions are diffused before the stripes are formed. For the other two methods, the junctions are diffused after the stripes are formed. In the former case, the junction does not extend down to the silicon-ceramic interface. This interface may introduce undesirable recombination effects for the high-voltage cells fabricated using the etching method or the carbon method.

The first plastic concentrators were completed, but they proved to be unsatisfactory because the reflecting surfaces were too rough. This result was caused primarily by our inexperience with the fabrication of plastic parts. As a result, all future concentrators will be made by companies specializing in the fabrication of plastic parts having good optical performance.

METALLIZATION PROBLEMS (D. Zook, B. Grung, R. Hegel, and T. Heisler)

During part of the quarter, few cells were processed successfully because of problems that developed in our metallization processing. The basic process, described in previous reports, is based on sputtering, and uses PtSi for ohmic contact to the p-region. The main metallization for both the p and n electrodes is a sputtered Ni layer which can then be coated with solder. The basic problem is that the Ni would not adhere during soldering.

Various causes of this problem were investigated. The suspected causes were:

- Increased humidity
- A change in the processing (diffusion or cleaning)
- A change in the system (e. g. , presence of other targets in sputtering system)

To test these hypotheses, a number of experiments were run, namely:

- The cooling system in the sputtering system was modified so that warm water is used to heat the target and substrate table prior to opening up the sputtering system so as to avoid condensation due to high humidity.
- A triple cup shield was constructed to prevent contamination from different targets.

- The ground shield used in the sputter etch position was thoroughly cleaned.
- Various fluxes were used to optimize solderability under different conditions.
- A lower melting-point solder (In/Sn) was used to reduce oxidation during soldering.
- Various cleaning procedures were investigated.

In the experiments, a number of the following types of substrates were used:

- n and n+ type single-crystal wafers
- n+ and p-type SOC material
- Slotted and interdigital electrodes on SOC
- Freshly processed cells and reworked SOC cells

The results of these experiments can be summarized as follows:

- Single-crystal substrates can always be soldered with good adhesion, whether or not they are processed with SOC material.
- PtSi contacts on SOC material can always be soldered with good adhesion, regardless of the number of times the solder is stripped and resputtered.

The experiments showed that the lack of adhesion was not due to increased humidity or to cross contamination in the sputtering system. The problem was due to a change in the cleaning process that was used to strip the oxide after diffusion. It was found that etching with 10:1 dilute HF was the main cause of the problem and that an etch with full-strength HF solves the problem.

We tentatively conclude that the oxide layer formed during diffusion of SOC material is not fully removed by the dilute HF etch normally used in semiconductor processing. Since HF does react with the mullite, it is entirely conceivable that the mullite affects the HF etching process. The use of dilute HF was a recent change recommended as being less stressful to the silicon surface. We need to fully understand the role of the mullite and of the platinum as they affect HF etching. The presence of surface oxides would be expected to be more critical in alternative metallization methods, such as evaporation or electroless deposition rather than sputtering.

We plan to verify the above conclusions with measurements of the oxide thickness for different processes using Auger analysis.

CONDUCTIVE INTERFACE (T. Schuller and D. Zook)

We have previously reported observations and measurements of the silicon-carbon interface. The primary goal of this task is to improve the conductance (increase the thickness) of the carbon layer used to wet the ceramic and to obtain ohmic contact between the carbon and the p-type silicon so that the carbon contributes significantly to decreasing the series resistance of the solar cells. Two additional goals are: 1) to investigate the use of doped carbons as diffusion sources for doping of the back surface of silicon to provide a BSF effect, and 2) to investigate the use of the glassy carbon as a protective barrier against unwanted impurity diffusions from the substrate into the silicon layer.

An important part of this effort is to have control of the carbon layer. For this reason, we have begun development of a method of producing doped glassy carbon layers. We had previously demonstrated that "Vitregraph" glassy carbon coatings made by Tylan Corporation showed very little erosion by the molten silicon. This is important if the vitreous carbon is to be used as a protective barrier.

The basic approach we have taken is to use a modification of techniques described in the open literature to produce bulk glassy carbon ware. A resin is diluted with solvent and spun onto the substrate. The layers are then fired in a conventional belt furnace at 900°C to produce a glassy carbon (GC) layer as described in the Quarterly Report No. 8.

In this quarter, two dip coating runs were devoted to silicon coating of GC and boron-doped GC substrates. Previously, only one or two substrates were dipped at the end of a dipping run. The first of the two dip runs resulted in poor silicon coatings. This is believed due to thick unheat-treated glassy carbon layers ($\rho_s = 5$ to $15 \Omega/\square$) and poor dipping conditions.

Sheet resistivity measurements of the first dip-run silicon coatings were made using the four-point probe and are summarized in Table 7. All samples were dipped with the same pull-rate, resulting in a similar silicon coating thickness.

In Table 7, silicon-to-carbon contacting is indicated in the dipped GC-coated substrates by a lower ρ_s measurement of 8 to $40 \Omega/\square$. In contrast, the hand-rubbed Ultra-Carbon control sample is $200 \Omega/\square$. On some of the dipped samples the silicon was etched off with CP4 etch and considerable erosion of the vitreous carbon layer was observed. High-

temperature firing of the carbon layers may reduce this degree of erosion. There is evidence of the boron-doped carbon doping the melt. This is indicated by contrasting the ρ_s of the silicon layer on the doped carbon samples and the ρ_s of the silicon on a hand-rubbed Ultra-Carbon sample dipped after the doped carbon samples.

Table 7. Sheet Resistivity of Silicon Coatings
(First Dip Run)

Substrate	Silicon Layer ρ_s ($\Omega/\square$)
Hand-rubbed Ultra-Carbon control before 900° Fired GC (4 samples)	200 8 to 40
900° Fired boron-doped GC (dipped) near end of run	4.2, 4.4
Hand-rubbed Ultra-Carbon dipped after boron-doped samples	17

In the second dip run, eight GC-coated substrates with thinner carbon coatings (avg. $\rho_s = 52 \Omega/\square$) were dipped. The silicon coated all of the substrates very well. Sheet resistivity measurements for the sequence are summarized in Table 8. All samples were dipped with the same pull-rate, resulting in similar silicon coating thicknesses.

Table 8. Sheet Resistivity of Silicon Coatings
(Second Dip Run)

Substrate	Silicon Layer ρ_s ($\Omega/\square$)
Hand-rubbed Ultra-Carbon control before Unheat-treated GC (3 samples)	120 avg. = 130
Boron-doped GC (5 samples)	avg. = 3.4
Hand-rubbed Ultra-Carbon control after GC samples	2.1

Comparison of the first two lines of Table 8 shows no evidence of electrical contact between the silicon and carbon. This is possibly due to the high ρ_s of the carbon layer before dipping. The bottom two lines indicate boron doping of the melt by the GC for the same reasons as previously mentioned.

Diodes were made from this dip run and results are listed in Table 9.

The cell measurements show that the GC coatings can produce performance at least as good as that produced with hand-rubbed carbon.

Table 9. Summary of SOC with Glassy Carbon

Diode	No. of Diodes	Avg. Active Area (cm ²)	V _{oc} (volts)	J _{sc} (mA/cm ²)	Fill Factor	Avg. Eff. (%)	Max. Eff. (%)	Comments
120-1A-Q11	5	0.048	0.47	22.2	0.668	7.2	8.2	Hand-rubbed carbon control
120-3B-Q11A	6	0.070	0.50	21.6	0.679	7.25	8.4	GC
120-3B-Q11B	6	0.085	0.50	22.0	0.672	7.4	7.7	GC
120-3A-Q11	1	1.05	0.50	19.5	0.619	6.0	6.0	GC

It is expected that the erosion resistance and the impermeability of the GC layers will be increased by high-temperature firing. For this purpose, an induction furnace for high-temperature heat treatment of vitreous carbon coatings has been set up. Several samples have been fired with varying degrees of success. Substrates with multiple vitreous layers peeled when fired at temperatures greater than 1200°C. To correct this problem, we began firing the substrates after each carbon layer. It was found to be necessary to use a lower-viscosity resin for the second layer after the high-temperature firing of the first. At present, the effort is being directed toward correcting a nonuniform heating problem in the high-temperature firing. As soon as this is corrected, high-temperature firing of successive layers will continue.

In summary, GC layers have been demonstrated to act effectively as wetting agents and as diffusion sources for doping silicon layers. Firing at 900°C does not appear to give adequate erosion resistance and impermeability, although such films are adequate to produce good cell performance. High-temperature firing is under investigation.

ANALYSIS OF GROWTH (D. Zook and S. Schuldt)

During the quarter, there was significant activity in the theoretical analysis of conditions required for stable growth. The details are presented in Appendices A and B. There was fruitful interaction between Honeywell and Professor Scriven's group at the University of Minnesota, and our results have been tempered by the discussions with them. At this point, however, they do not necessarily agree with our analysis.

The first results relate to the relationship between growth velocity and thickness. The basic assumption used was that thermal gradients in the liquid are negligible. This

assumption gives the limiting growth velocity

$$v = \frac{K_m}{L} \left(\frac{dT}{dx} \right)_i \quad (1)$$

proportional to the temperature gradient $(dT/dx)_i$ in the solid at the liquid-solid interface. Here, K_m is the thermal conductivity of the solid at the melting point and L is the heat of fusion per unit volume.

A general one-dimensional analysis then gives the relationship

$$v^2 t = \frac{2}{L^2} \int_{T_0}^{T_m} K f(T) dT \quad (2)$$

where T_0 is room temperature and T_m is the melting point; t is the thickness and $f(T) = f_1(T) + f_2(T)$ is cooling function of the surface (w/cm^2), including both the front surface and the back surface.

Equation (2) implies that with a given cooling condition the square root of thickness should be inversely proportional to the growth velocity. This is approximately true experimentally, as shown in Figure A-1 of the Appendix A. To increase the growth velocity for a given thickness, the cooling rate must be increased.

The second analytical result relates to the shape of the liquid-solid interface. Analysis of the heat flow in the vicinity of a corner gives relationship for θ_1 , the angle of the interface:

$$\sin \theta, \cos \theta_1 = \frac{f_1(T_m)}{Lv} \quad (3)$$

Numerically, the right hand side of Equation (3) is much less than unity. The nearly flat interface usually assumed corresponds to small values of θ_1 . There is also another solution with $\theta_1 \leq 90^\circ$, corresponding to a very steep interface, almost parallel to the solid surface.

These two solutions correspond physically to quite different physical situations, and so it is important to clarify which solution corresponds to reality. This question is addressed in Appendix B, where a linearized radiation law is used at the exterior solid surface. According to the linear models in Appendix B, the freezing interface must be nearly flat (θ_1 small). It is shown there that a solution $\theta_1 \leq 90^\circ$ leads to physical absurdities.

Assuming that the interface is nearly flat, an expression for the radius of curvatures, ρ , can also be derived:

$$\rho = \frac{Lv t_1}{f_1 (T_m)} = \frac{Lv t_2}{f_2 (T_m)} \quad (4)$$

where t_1 and t_2 are the thicknesses measured from the maximum point of the liquid-solid interface, and the total film thickness is $t = t_1 + t_2$.

A final theoretical result has been an expression for the contact angle, α_1 , between the liquid and the grown surface. In normal EFG ribbon growth, this angle is observed to be about 11° . The expression we obtained is

$$\alpha = \frac{\sigma_2}{\sigma_1} \left(1 - \frac{\sigma_3}{\sigma_1} \right) \theta_1$$

where the σ 's are the surface tensions. Since θ_1 is a small angle, the value of α_1 is σ_2/σ_1 , the surface tension vapor interface, divided by that of the liquid-solid interface. Its value is only slightly affected by thermal gradients in the solid.

On the basis of this analysis, we conclude that:

- 1) The $v^2 t = \text{constant}$ relationship is quite general and applies for a given set of cooling conditions in any coating system.
- 2) The growth rate for a given thickness can only be increased by increasing the cooling rate in the solid.
- 3) The liquid-solid interface is a slightly curved, slightly tilted surface, with the tilt and curvature determined by the cooling rate at the interface divided by the heat of fusion times the velocity.
- 4) The liquid contact angle for stable growth is not significantly affected by the growth rate.
- 5) The tilt angle of the interface is determined by the relative amount of cooling that occurs from the ceramic side compared with the amount of cooling from the exposed side of the silicon. This angle may be important in determining the type of nucleation and hence the grain size.

CONCLUSIONS

From work performed during the quarter, we conclude that:

- The method of processing the ceramic substrate is not critical in terms of its ability to maintain its integrity before, during, and after dipping.
- A wide range of mullite compositions will withstand the dipping process.
- Mullite substrates having 0.5-mm slots on 1-mm centers were successfully dipped, indicating high slot/material ratios in the ceramic are feasible.
- Slotted mullite substrates must have a thermal expansion coefficient closely matching that of silicon to prevent post-process cracking of the ceramic/silicon layer. This cracking results in poor cell performance.
- Full strength hydrofluoric (HF) acid must be used to etch the surface of dipped layers or the top sputtered contact will not adhere.
- Increasing the "P" dopant in the SOC layer increases open-circuit voltage (V_{oc}), increases fill factor (FF), and slightly decreases short-circuit (J_{sc}). The optimum doping level has not been determined yet.
- Removing the baffle from our diffusion furnace, packing the ends with quartz wool, and changing the gas flow rate has improved our diffusion uniformity.
- Elevating the silicon melt with respect to the heating element in the dip coater causes thicker coatings to form at the same pull rate.
- Molten silicon can be made to fill the coating trough of the SCIM coater and a 6- to 8-mm meniscus can be obtained.
- Better temperature control of the various hot zones of the SCIM coater must be obtained before successful coating can occur.
- Whereas glassy carbon coatings can be used as silicon diffusion source and wetting agents, we have not proven their erosion resistance or impermeability when used with the dipping process.

- A detailed theoretical analysis of conditions required for stable growth indicates that:
 - 1) The $v^2t = \text{constant}$ relationship is quite general and applies for a given set of cooling conditions in any coating system.
 - 2) The growth rate for a given thickness can only be increased by increasing the cooling rate in the solid.
 - 3) The liquid-solid interface is slightly curved, slightly tilted surface, with the tilt and curvature determined by the cooling rate at the interface divided by the heat of fusion times the velocity.
 - 4) The liquid contact angle for stable growth is not significantly affected by the growth rate.
 - 5) The tilt angle of the interface is determined by the relative amount of cooling that occurs from the ceramic side compared with the amount of cooling from the exposed side of the silicon. This angle may be important in determining the type of nucleation and hence the grain size.

RECOMMENDATIONS

To date, our cell processing activity has been carried out on unslotted substrates, with both contacts being brought out the top surface. Henceforth, we would recommend that our standard cell configuration use slotted substrates, with our active area consideration only relating to top contact area requirements.

Further, once a definitive high-temperature firing of our conductive interface (glassy carbon) has been achieved (to demonstrate whether an erosion-resistant dopant source can be obtained using GC coatings), we recommend a cessation of this activity and an increase in our slotted-cell fabrication activity until the fabrication techniques for slotted cells are better defined.

NEW TECHNOLOGY

There were no reportable "New Technology" items uncovered during this reporting period.

PROJECTION OF FUTURE ACTIVITIES

Future activities are projected as follows:

- We will complete the dedicated coater which will then be used to maximize our coating rate for 100- μ m layers.
- Various compositions of mullite substrates will be dip coated. The goal will be to define the composition best suited to slotted-cell fabrication.
- More slotted substrates of various mullite compositions will be fabricated to be used for cell processing.
- Work will continue to define the optimum N_D value for our silicon-base layer.
- The dip coater will undergo minor modifications to increase pull-rate without sacrificing layer thickness.
- An array of thermocouples will be assembled on a large mullite plate to provide accurate longitudinal and lateral temperature profiles in the SCIM coater.
- An offset crucible-trough configuration will be installed within the SCIM coater to locate the silicon meniscus adjacent to the solidification zone.
- We will accelerate our efforts to provide a "standard" slotted-cell processing technique.
- The effect on cell performance of silicon layer microstructures near slot edges will be investigated.
- A greater number of slotted substrate solar cells will be processed.
- High-voltage stripe cell configurations will be fabricated and evaluated.
- Plastic optical couplers will be fabricated for use with high-voltage cells.
- High-temperature firings of doped GC layers will be carried out to prove the viability of this approach to providing a conductive interface.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 16, 17, and 18, respectively.

NOTE: IN ADDITION TO THE ABOVE PROGRAM PLAN, THE HONEYWELL CORPORATE TECHNOLOGY CENTER WILL PROVIDE THE REQUIRED DOCUMENTATION, ATTEND THE REQUIRED MEETINGS AND DELIVER THE REQUIRED SAMPLES AS PER CONTRACT AGREEMENT.

△ PLANNED
▲ ACCOMPLISHED GOALS

Figure 16. Updated Program Plan

Figure 17. Updated Program Labor Summary

Figure 18. Updated Program Cost Summary

APPENDIX A
ANALYSIS OF NONLINEAR GROWTH CONDITIONS
(D. Zook)

This appendix analyzes the growth conditions retaining the nonlinear aspects of the problem. This approach has the advantage of generality, but has some limitations in the conclusions that can be reached.

1. RELATIONSHIP BETWEEN MAXIMUM GROWTH VELOCITY
AND TEMPERATURE GRADIENT AT THE LIQUID-SOLID
INTERFACE

Thermal analysis of the growth of sheet silicon has been discussed by a number of authors.¹⁻⁶ Since silicon has a large heat of fusion, there is a significant discontinuity in the temperature gradient at the liquid-solid interface. Assuming a planar interface, we can write the heat flow per unit area in the x direction, perpendicular to the interface as

$$-K \left(\frac{dT}{dx} \right)_{x_i + \delta x} = -K_L \left(\frac{dT}{dx} \right)_{x_i - \delta x} + vL \quad (A1)$$

where K and K_L are the thermal conductivity of the solid and liquid, respectively, x_i is the value of x at the interface, v is the velocity, and L is the heat of fusion (in joules/cm³).

The heat conducted away from the freezing interface is limited by the rate of heat dissipation from the rest of the sheet ($x > x_i$). As the growth velocity increases, the second term increases, so that the first term must decrease. In the limit, the temperature gradient in the liquid will approach zero, and the limiting growth velocity is given by

$$v = - \frac{K}{L} \left(\frac{dT}{dx} \right)_{x_i + \delta x} \quad (A2)$$

Examples of cases in which the gradient in the liquid is much less than that in the solid are given by Bell¹ in his computer modeling of EFG ribbon growth, at growth rates of 0.05 cm/sec and greater, which is the region of interest to silicon-on-ceramic (SOC) growth.

2. SIMPLE HEAT FLOW ANALYSIS

An analytical approach can be used if it is assumed that the heat loss from the surface of the sheet is only a function of absolute temperature, T . This is certainly the case for radiative heat loss. We will follow Ciszak² and neglect the convection term in the heat-transfer equation. The heat flow is given by:

$$J_x = wtK \left(\frac{dT}{dx} \right) \quad (A3)$$

where w is the width and t the thickness of the silicon sheet (see Figure A1). If radiation

Figure A1. SOC layer thickness, t , as a function of growth speed, v , for a number of dip-coating runs under different conditions. Triangles and circles are used to indicate two series of coating runs in which attempts were made to hold the conditions constant.

losses dominate, the heat loss from a surface of the sheet is given by

$$dJ_x = \epsilon \sigma T^4 w dx \quad (A4)$$

where σ is the Stefan - Boltzman constant and ϵ is the emissivity. We can generalize to include other types of heat loss by letting

$$\left(\frac{dJ}{dx}\right) = w f(T) = w [f_1(T) + f_2(T)] \quad (A5)$$

where f_1 and f_2 are the cooling functions (W/cm^2) for surfaces 1 and 2. Combining Equations (A3) and (A5) gives:

$$\frac{d}{dx} \left(K \frac{dT}{dx} \right) = \frac{1}{t} f(T) \quad (A6)$$

This equation can be solved analytically for the case when $f(T)$ is a power law. However, for purposes of the present discussion, we will assume that the solution is given by $T = T(x)$ and consider the effect of scaling.

Consider the effect of a change in sheet thickness. Let $t^* = t/a^2$ be the new thickness. Equation (A6) then becomes

$$\begin{aligned} \frac{d}{dx} \left(K \frac{dT}{dx} \right) &= \left(\frac{f(T)}{t^*} \right) \\ &= \left(\frac{a^2 f(T)}{t} \right) \end{aligned} \quad (A7)$$

with a solution $T = T^*(x)$. This can be written as

$$\frac{d}{d(ax)} \left(K \frac{dT}{d(ax)} \right) = \frac{f(T)}{t} \quad (A8)$$

which is exactly the same as Equation (A6) but expressed in terms of the variable ax . Since the equation is the same, the solution will be the same, provided the boundary conditions on both variables are the same. If we take $ax = 0$ and $x = 0$ to be at the interface

($T = T_m$) and $ax = \infty$, $x = \infty$ to be at room temperature (T_0), then the boundary conditions are the same in spite of the scale change, and $T^*(x) = T(ax)$ is the new solution. The temperature gradient at the interface is given by

$$\left(\frac{dT^*}{dx}\right)_i = a \frac{dT(ax)}{d(ax)} \Big|_{x=0} = a \frac{dT(x)}{dx} \Big|_{x=0} \quad (A9)$$

so that the product

$$\sqrt{t}^* \left(\frac{dT^*}{dx}\right)_i = \sqrt{t} \left(\frac{dT}{dx}\right)_i = \text{constant} \quad (A10)$$

is independent of the value of thickness. The scaling argument applies in the case where the convective term is included in the analysis.

Combining Equation (A10) with (A2) states that

$$v\sqrt{t} = -\sqrt{t} \frac{K_m}{L} \left(\frac{dT}{dx}\right)_i = \text{constant} \quad (A11)$$

should be a constant for given conditions of heat removal from the surface. In our system, the rate of heat removal depends on the position of the liquid-solid interface, which will vary with growth speed and temperature of the melt. However, this variation will be small, so that the $v\sqrt{t}$ relationship should be approximately obeyed for a given crucible position and melt temperature. This is approximately the case as shown by the experimental data in Figure A1.

If we assume that the temperature is a monotonic function of x , then x can be expressed as a unique function of T . Thus, the temperature gradient, dT/dx , can be expressed as a function of T and we can set

$$K \frac{dT}{dx} = -g(T) \quad (A12)$$

with the heat flow (watts) given by

$$J_x = wt K \frac{dT}{dx} = -wt g(T) \quad (A13)$$

From conservation of energy, it follows that

$$-\Delta J_x = wt \frac{dg}{dT} \frac{dT}{dx} \Delta x = \Delta J_y = w \Delta x f(T) \quad (A14)$$

so that

$$g \frac{dg}{dT} = \frac{K}{t} f(T) \quad (A15)$$

This equation can be integrated to give

$$g^2(T) = \frac{2}{t} \int_{T_0}^T K f(T) dT \quad (A16)$$

where we have taken $g(T_0) = f(T_0) = 0$, and T_0 is the ambient temperature.

Combining Equation (A16) with (A11) we find that

$$\begin{aligned} v^2 t &= \frac{L}{L^2} g^2(T_m) \\ &= \frac{2}{L^2} \int_{T_0}^{T_m} K f(T) dT \end{aligned} \quad (A17)$$

which is a closed form for the $vt^{1/2}$ product in terms of the cooling function, $f(T)$. For the case of radiant cooling of an SOC layer, we might assume $f_2 = 0$, $f_1 = \epsilon \sigma T^4$. This gives

$$v^2 T = \frac{\epsilon \sigma K_m T_m^5 (T_m^4 - T_0^4)}{2L^2} \quad (A18)$$

or $vt^{1/2} = 1.25 \mu\text{m/sec} (\mu\text{m})^{1/2}$ for silicon, using values from Table A1.

Table A1. Properties of Silicon at the Melting Point

Symbol	Parameter	Value
L	Heat of fusion/volume of solid	4120 J/cm ³
K	Thermal conductivity of solid	0.287 W/cm°C
	Density of solid	2.30 g/cm ³
	Density of liquid	2.53 g/cm ³
σ_i	Surface of tension of liquid	720 dyne/cm
ϵ	Emissivity	0.46
θ_c	Growth contact angle	11°

3. LIQUID-SOLID INTERFACE ANGLE

The nature of the liquid-solid interface profile has been the subject of intense discussion, and a number of people have suggested to us experiments to determine the tilt angle of the interface. The above analysis can be extended to provide a simple relationship regarding the angle of the liquid-solid interface. Consider an isothermal interface as shown in Figure A2 inclined at an angle θ with respect to the y axis. An element of thickness, Δy , will generate a heat flow

$$\Delta J = Lv\Delta y = Lv\Delta s \cos\theta \quad (A19)$$

where Δs is an elemental distance along the interface. This heat must be removed by the thermal gradient, ΔT , which must have a magnitude

$$K |\nabla T| = \frac{\Delta J}{w\Delta s} = Lv \cos\theta \quad (A20)$$

The horizontal component of flux at the left surface is then

$$K \left(\frac{dT}{dy} \right)_1 = Lv \cos \theta_1 \sin \theta_1 \quad (A21)$$

which must equal the heat loss function, $f_1(T_m)$. Thus, the angle of the interface at the trijunction is given by

$$\sin \theta_1 \cos \theta_1 = \frac{f_1(T_m)}{Lv} \quad (A22)$$

As an example, if we consider the case of radiant cooling, $f_1(T_m) = \epsilon\sigma T_m^4 = 21.6 \text{ W/cm}^2$, using the value from Table A1. Thus, $f/L = 0.005 \text{ cm/sec}$, and at a growth rate $v = 0.1 \text{ cm/sec}$, the value of $\sin \theta_1 \cos \theta_1 = 0.05$, and, in general, $f(T_m)/Lv \ll 1$.

In general, there are two solutions to Equation (A22): one for θ_1 near 0 and one for θ_1 near 90°. Actually, only the small value is physically allowable, as shown in Appendix B. In view of this, the angles at the corners of the interface are simply:

$$\theta_1 = \frac{f_1(T_m)}{Lv} \quad \text{and} \quad \theta_2 = \frac{f_2(T_m)}{Lv} \quad (A23)$$

In between these two values, the interface is curved, with the curvature also determined by the heat flow, as discussed below.

Figure A2. Growth Geometry. (a) The liquid-solid interface has a radius of curvature ρ and an angle θ_1 and θ_2 with the y-axis. (b) The s-coordinate is tangent to the interface and the r-coordinate is normal to the interface.

Power Law Cooling Function

At this point it seems worthwhile to discuss in more detail and power law case, $f_1 = cT^n$, $f_2 = 0$. Cizek² has given an analytic solution for $n = 4$ (radiative cooling) which can be generalized to show that for any n with $T_0 = 0$ and $K = K_m T_m / T$, the solution is of the form

$$T^{-n/2}(x) = \frac{1}{ax+b} \quad (A24)$$

without the restriction that $T_0 = 0$. Equation (A16) gives

$$g^2(t) = \frac{2}{nt} K_m T_m [f_1(T_0)] \quad (A25)$$

so that

$$\theta_1 = \frac{(dT/dy)_1}{(dT/dx)_1} = \frac{f_1}{g} = \frac{nt}{2T} \left(\frac{dT}{dx} \right)_1 \quad \text{and} \quad vt^2 = \frac{2}{L^2} \frac{K_m T_m}{n} [f(T_m) - f(T_0)] \quad (A26)$$

In particular, for radiative cooling ($n = 4$), the interface angle is given by

$$\theta_1 = 2 \frac{t}{T_m} \left(\frac{dT}{dx} \right)_i = \frac{2Lvt}{K_m T_m} \quad \text{and} \quad v^2 t = \frac{\epsilon \sigma K_m T_m (T_m^4 - T_o^4)}{2L^2} \quad (\text{A27})$$

The latter formula agrees with Ciszek's expression² for the maximum growth velocity.

4. CURVATURE OF THE LIQUID-SOLID INTERFACE

The first two subsections of this appendix used a strictly one-dimensional approach, and the third subsection discussed the slope of the liquid-solid interface at the surface.

The two-dimensional problem is much more complicated than the one-dimensional equation. The basic equation is $\nabla \cdot J = 0$. If we choose a rotated cartesian coordinate system (r, s) as shown in Figure A2b, so that r is along the normal to an isotherm, and s is along it, then

$$\nabla \cdot J = \frac{\partial}{\partial r} \left(K \frac{\partial T}{\partial r} \right) + K_m \frac{\partial^2 T}{\partial s^2} = 0 \quad (\text{A28})$$

since $K(t) = K_m$ along the s -axis. The basic boundary conditions are that $T = T_m$ along the boundary and Equation (A20) which states that

$$\left(\frac{\partial T}{\partial r} \right)_i = \frac{Lv \cos \theta}{K_m} \quad (\text{A29})$$

Equation (A28) is an elliptic partial differential equation and therefore, as discussed by Morse and Feshbach⁷, both the value of T and the gradient of T cannot be specified on a given boundary if the equation is to have a solution. In our problem we must specify both of these, and we therefore have the problem of determining the shape of the boundary which yields unique and reasonable solutions of the Laplace equation.

One way to approach the problem is to expand the temperature in a Taylor's series about a point on the interface:

$$T(r, s) = T_m + \left. \frac{\partial T}{\partial r} \right|_o r + \frac{1}{2} \left. \frac{\partial^2 T}{\partial r^2} \right|_o r^2 + \frac{1}{2} \left. \frac{\partial^2 T}{\partial s^2} \right|_o s^2 \quad (\text{A30})$$

where $\partial T/\partial s$ and $\partial^2 T/\partial r \partial s$ must vanish because the s -axis is tangent to the isotherm. Choosing r and s to be on the isotherm, $T(r, s) = T_m$, we get a relationship between r and s . If we consider a circle that is tangent to the isotherm, it is easy to show that its radius ρ is

$$\rho = \frac{s^2}{2r} = - \frac{\frac{\partial T}{\partial r}}{\frac{\partial^2 T}{\partial s^2}} \quad (\text{A31})$$

Combining Equations (A28), (A29), and (A31) gives

$$\rho = \frac{Lv \cos \theta}{\frac{\partial}{\partial r} \left(K \frac{\partial T}{\partial r} \right)_i} \quad (\text{A32})$$

In particular, the curvature at the maximum ($\theta = 0$)¹ is given by

$$\rho = \frac{Lv}{\frac{\partial}{\partial x} \left(K \frac{\partial T}{\partial x} \right)_i} \quad (\text{A33})$$

Since we know θ is small from Appendix B, it follows that denominator is given approximately by Equation (A6), so that

$$\rho = \frac{Lv t_1}{f_1(T_m)} \quad (\text{A34})$$

Here, t_1 denotes the thickness from the maximum to the left surface. The angle of the edge is then

$$\theta_1 = \frac{t_1}{\rho} = \frac{f_1(T_m)}{Lv}$$

which is exactly the same as Equation (A23).

Thus, the curvature arrived at by considering the two-dimensional heat flow is totally consistent with the edge angle deduced by considering heat flow in the vicinity of the edge. The total thickness, $t_1 + t_2$, is $(f_1 + f_2)/Lv$, and the analysis is consistent whether heat flows to or from the ceramic. In the latter case, f_1 , θ_1 and t_1 are negative quantities. In the case of ribbon growth there is complete symmetry and $f_2 = f_1$, etc.

5. EFFECT OF SURFACE ENERGIES

The intersection of a liquid-vapor interface with a solid-liquid interface to form a solid-liquid-vapor trijunction occurs in all growth from the melt. There are surface energies, or surface tensions, associated with these interfaces. These energies determine whether sheet growth is stable, and whether the sheet gets thicker or thinner or remains constant as growth proceeds.

The equilibrium conditions at the trijunction have been described theoretically by Voronkov⁸ and by Bardsley, et al⁹. They calculate the equilibrium angles between the three phases (i. e., the angles α_1 and α_2 in Figure A3). Their result is that the sense of the surface energies, $\hat{t}_i$, times a unit tangent vector along the i th surface is zero (see Figure A3b):

$$\sum_{i=1}^3 \sigma_i \hat{t}_i = 0$$

This relationship can readily be derived by considering virtual displacements of the trijunction point in any direction. Apparently it is an old, well-known result¹⁰ known as "Newmann's Triangle." It has been generalized by Herring¹¹ to include the case when the surface energy depends on crystalline orientation.

This equilibrium relation cannot apply to the crystal growth case, for the following reason. The triangle relationship clearly fixes the angle between the solid vapor surface 3 and the liquid-solid interface 2 in Figure A3. However, we have seen that this angle is determined by heat flow conditions. Bardsley, et al.⁹, postulate that the interface curves around in order to satisfy the triangle condition "within a few microns" of the junction which is inconsistent with the third subsection of this appendix. In any case, this does not appear reasonable, since surface energy is a macroscopic concept, and the argument regarding virtual displacements should equally well apply over a large scale. On the other hand, if there is a gradual bending of the surfaces due to pressure or thermal condition, the virtual work argument applies to the tangents at the trijunction (see Figure A4).

Thus, crystal growth is a steady-state situation dominated by heat flow conditions necessary to remove the latent heat, rather than an equilibrium situation determined solely by surface energies. The conditions for a stable surface can be derived by considering the freezing of a film of thickness Δl on the surface A_2 . Consider the liquid-vapor surface to be displaced at an angle α_3 with respect to its steady-state position defined by $\alpha_3 = 0$. The change in surface energy is given by (see Figure A5):

$$\Delta F_s = \sigma_3 \Delta A_3 - \sigma_1 \Delta A_3 \cos(\alpha_1 + \alpha_3) - \sigma_2 \Delta A_3 \cos(\alpha_2 - \alpha_3) \quad (A35)$$

Figure A3. Trijunction Geometry. (a) Interfaces between three phases. (b) At equilibrium, the surface energies, σ_i , times the unit tangent vector, $\hat{t}_i$, form a closed triangle.

Figure A4. The Effect of Surface Curvature. (a) Curvature at the trijunction. (b) Gradual bending. In both (a) and (b) there is a well-defined tangent, and a virtual displacement of the trijunction (shown along 3) produces the same changes in areas, δA_i .

The change in volume energy is

$$\begin{aligned}\Delta F_v &= L\Delta V \\ &= L\Delta l(A_2 + 1/2 \Delta A_2)\end{aligned}\tag{A36}$$

The second term, which is the volume associated with the triangular shaded region in Figure A5, is second order in Δl and thus can be dropped. The sum of Equations (A26) and (A27) then gives an effective latent heat which depends on the angles:

$$L_e = \frac{\Delta F}{\Delta V} = L + \frac{1}{t} \frac{\sigma_3 - \sigma_1 \cos(\alpha_1 + \alpha_3) - \sigma_2 \cos(\alpha_2 - \alpha_3)}{\csc \alpha_2 \sin(\alpha_2 - \alpha_3)}\tag{A37}$$

where t is the thickness of the layer. With a typical sheet thickness of $t = 10^{-2}$ cm, the first term is larger than the value of σ_1 given in Table A1 by about a factor of 10^6 .

Although equilibrium thermodynamics do not apply to the present case, the basic principles of nonequilibrium thermodynamics appear to be applicable. Stationary nonequilibrium states have the important property¹² that they are characterized by a minimum of the entropy production rate compatible with the external constraints imposed on the system. Such states are stable with respect to perturbations of thermodynamic forces.

Figure A5. Variation of the Growth Surface. A film of thickness Δl is frozen onto the surface 2, with the new solid surface ΔA_3 at an angle α_3 with respect to the original.

In our case, the entropy production rate associated with the rate of heat flow is from the melt to the environment. The rate of entropy production is

$$\dot{S} = L_e v \text{ wt} \left(\frac{1}{T_m} - \frac{1}{T_o} \right) \quad (\text{A38})$$

Clearly, the only parameter not fixed by the heat flow is the angle α_3 , which we assume not to be determined by flow conditions in the melt. Thus, minimization of $\dot{S}$ implies minimization of L_e with respect to θ_3 . Differentiation of Equation (A37) gives:

$$0 = \frac{d}{d\alpha_3} \left(\frac{\Delta F}{\Delta V} \right) = \frac{1}{t} \frac{\sigma_3 \cos(\alpha_2 - \alpha_3) - \sigma_2 - \sigma_1 \cos(\alpha_1 + \alpha_2)}{\csc \theta_2 \sin^2(\alpha_2 - \alpha_3)} \quad (\text{A39})$$

For steady-state conditions, $\alpha_3 = 0$, and α_1 is the contact angle, θ_c . Equation (A39) gives:

$$\sin(\theta_c + \theta_1) = \frac{\sigma_2}{\sigma_1} + \frac{\sigma_3}{\sigma_1} \sin \theta_1 \quad (\text{A40})$$

where θ_1 is the tilt angle of the interface, and $\theta_1 = \alpha_2 - \pi/2$. The second derivative evaluated at the same angles is

$$\frac{d^2}{d\alpha_3^2} \left(\frac{\Delta F}{\Delta V} \right) = \frac{\sigma_3}{t} \quad (\text{A41})$$

which is always positive, so that the energy is indeed a minimum. We note that the minimum is sharper for thinner films.

A check of Equation (A40) can be made for germanium from the data cited by Bardsley.⁹ He cites experimental values of $\sigma_1 = 632 \text{ erg/cm}^2$ and $\sigma_2 = 181 \text{ erg/cm}^2$. With $\sigma_i = 0$, which is a good approximation for Czochralski growth, Equation (A40) gives $\theta_1 = 16.6^\circ$, compared with observed values of 15 to 20°. Comparable data for silicon are not available.

Using the small-angle approximation, we can write equation (A40) as

$$\theta_c = \frac{\sigma_2}{\sigma_1} - \left(1 - \frac{\sigma_3}{\sigma_1} \right) \theta_1 \quad (\text{A42})$$

Thus, the effect of a positive interface tilt, θ_1 , is either to decrease or increase θ_c depending on the relative magnitudes of σ_3 and σ_1 . From the fact that $\theta_c = 11^\circ$ for silicon when $\theta_1 = 0$, we obtain $\theta_c = 140 \text{ erg/cm}^2$. The triangle condition then puts limits on σ_3 :

$$\sigma_1 - \sigma_2 < \sigma_3 < \sigma_1 + \sigma_2 \quad (\text{A43})$$

which means that the coefficient of θ_1 in Equation (A32) is within the range of $\pm \sigma_2/\sigma_1 = \pm 0.2$. Therefore, the effect of a tilt of the interface on the meniscus is not large.

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APPENDIX B
DIMENSIONAL MODEL ANALYSIS
(S. Schuldt)

Two quasi-one-dimensional models and a two-dimensional model for the silicon-on-ceramic (SOC) growth problem are examined. A nearly planar freezing front ($\theta_{\max} \ll \pi/4$) is consistent with reasonable physical parameters in all three models. The approximate value obtained from the three models is $\theta_{\max} \doteq (h/\rho v \lambda) (T_m - T_o)$. Neither of the one-dimensional models yields a ribbon thickness, t . However, the thickness according to the two-dimensional model satisfies $v\sqrt{t} \doteq (\sqrt{2}kh/\rho \lambda) (T_m - T_o)$.

ASSUMPTIONS

Heat transfer is neglected from silicon to the ceramic ($\frac{\partial T}{\partial y} = 0$ at ceramic surface). For this approximation, the SOC problem is equivalent to the unsupported ribbon growth problem through the half-thickness $0 \leq y \leq t/2$. Temperature gradients are neglected in the melt, and piston-like flow is assumed. Other special assumptions are listed in the three models. Parameter definitions are:

- λ = Heat of fusion (cal/gm^{-1})
- h = Effective heat transfer coefficient ($\text{cal/cm}^{-2}/\text{deg}^{-1}/\text{sec}^{-1}$)
- k = Heat conductivity ($\text{cal/cm}^{-1}/\text{deg}^{-1}/\text{sec}^{-1}$)
- ρ = Density (gm/cm^{-3})
- c = Specific heat ($\text{cal/gm}^{-1}/\text{deg}^{-1}$)
- v = Pulling velocity (cm/sec^{-1})

MODEL 1

The y -component of temperature gradient is constant on any vertical line in the shaded region of Figure B1. Hence, only part of the latent heat released at the freezing front flows crosswise through the solid to the water surface:

$$k |\nabla T| \sin \theta = \frac{k(T_m - T_s)}{\eta} = h(T_s - T_o) \quad (\text{B1})$$

Figure B1. Parameters of Model 1

In addition, local heat balance at the freezing front requires that

$$\rho \lambda V \cdot \underline{\underline{n}} = k |\nabla T|$$

or

$$|\nabla T| = (\rho \lambda V / k) \cos \theta \quad (B2)$$

Elimination of $|\nabla T|$ between Equations (B1) and B2) gives

$$\rho \lambda V \sin \theta \cos \theta = \frac{k(T_m - T_s)}{\eta} = h(T_s - T_o) \quad (B3)$$

When T_s is eliminated from Equation (B3), one obtains:

$$\sin \theta \cos \theta = (k / \rho \lambda V) (T_m - T_o) / (\eta + k/h) \quad (B4)$$

where θ and η are understood to be functions of x over $0 \leq x \leq b$, the limits of the shaded region in Figure B1. [It is not necessary to know the value of b , since x is a suppressed parameter in Equation (B4).]

One would hope that Equation (B4) holds over the entire range $0 \leq x \leq b$, so that $\theta_{\max}$ and $\eta_{\max} = t/2$ may both be found by setting $\eta = 0$ and $\theta = 0$, respectively.

(a) Setting $\eta = 0$ gives:

$$\sin \theta_{\max} \cos \theta_{\max} = (h / \rho \lambda V) (T_m - T_o) \quad (B5)$$

It might appear that Equation (B5) has two complementary solutions in the first quadrant (i. e., θ and $\pi/2 - \theta$). Note from Figure B1, however, that θ must be a decreasing function of η ; in other words, $d\theta/d\eta < 0$. Differentiating Equation (B4),

$$\cos 2\theta \, d\theta/d\eta = -(k/\rho\lambda V) (T_m - T_o) / (\eta + k/h)^2 \quad (B6)$$

we find that $d\theta/d\eta < 0$ only if $2\theta < \pi/2$. It follows that $\theta_{\max} < \pi/4$, and the melt profile is much more planar than the diagram shows. In fact, taking:

$$\rho = 2.33 \text{ gm/cm}^3$$

$$\lambda = 337 \text{ cal/gm}$$

$$T_m = 1700^\circ\text{K}$$

$$h(T_m - T_o) \doteq (T_m - T_o) \cdot d/dT(\sigma T_4)/T = T_m$$

we find $(h/\rho\lambda V) (T_m - T_o) \doteq 3.4 \times 10^{-5} (T_m - T_o)/V$, and this is $\ll 1$ for reasonable values of $(T_m - T_o)$ and V .

- (b) The ribbon thickness, $t = 2\eta_{\max}$, corresponds to $\theta = 0$ in Equation (B4). Unfortunately, this gives $t = \infty$, which is an indication of a breakdown in the model.

MODEL 2

To address the problem in (b) above, let the main assumption in Model 1 be changed as follows. Let all of the latent heat released at the freezing front flow diagonally through the solid to the outer surface. The direction is along the normal, $\tilde{n}$, to the freezing front (see Figure B2).

Figure B2. Slant Conduction Path

Equation (B1) must now be replaced with

$$k |\nabla T| = K(T_m - T_s) \eta \csc \theta = h(T_s - T_o) \sin \theta \quad (B1')$$

where $\eta \csc \theta$ is the distance AB (a function of x). The factor, $\sin \theta$, is needed in the right-hand group because an area, ΔA , on the freezing front at point A corresponds to an area $\Delta A / \sin \theta$ at B. Local heat balance, Equation (B2), is unchanged. Eliminating T_s and $|\nabla T|$ between Equations (B1') and (B2) gives

$$\cot \theta = (k/\rho\lambda V) (T_m - T_o) (\eta + k \sin^2 \theta / h) \quad (B4')$$

As before, an attempt is made to determine $\theta_{\max}$ and $\eta_{\max}$:

(a) Setting $\eta = 0$ gives the same result as Model 1:

$$\sin \theta_{\max} \cos \theta_{\max} = (h/\rho\lambda V) (T_m - T_o) \quad (B6')$$

(b) Setting $\theta = 0$ gives $\eta_{\max} = 0$, a result which is obviously no better than Model 1.

MODEL 3

We ignore, for the moment, condition (B2) along the freezing front and attempt a solution, $T(x, y)$ satisfying Laplace's equation and other known conditions (see Figure B3):

$$\Delta T = 0 \text{ in the solid} \quad (D7)$$

$$T(x, y) = T(x, -y) \quad (B8)$$

$$T(0, t/2) = T(0, -t/2) = T_m \quad (B9)$$

$$T(\infty, y) = T_o \quad (B10)$$

$$-k \partial / \partial y T(x, t/2) = h[T(x, t/2) - T_o] \quad (B11)$$

$$\int_0^\infty h[T(x, t/2) - T_o] dx = \rho V \lambda t/2 \quad (B12)$$

Figure B3. Parameters for Model 3

Such a solution is

$$T(x, y) = T_o + (T_m - T_o) \cos ay e^{-ax} / \cos at/2, \quad (B13)$$

with $\underline{a}$ and $\underline{t}$ satisfying

$$\tan at/2 = h/ak \text{ from Equation (B11)} \quad (B14)$$

and

$$at/2 = h(T_m - T_o) / \rho v \lambda \text{ from Equation (B12)} \quad (B15)$$

Although the transcendental Equation (B14) has an infinite number of solutions a for any given t , the relation (B15) restricts the choice to

$$a = (h/k) \cot [h(T_m - T_o) / \rho v \lambda] \quad (B16)$$

Substituting Equation (B16) into (B15) gives

$$\begin{aligned} t &= (2/a) h (T_m - T_o) / \rho v \lambda \\ &= [2k (T_m - T_o) / \rho v \lambda] \tan [h (T_m - T_o) / \rho v \lambda] \end{aligned} \quad (B17)$$

Since $h(T_m - T_o) / \rho v \lambda \ll 1$, Equation (B17) may be approximated by

$$\boxed{v\sqrt{t} \doteq \sqrt{2kh} (T_m - T_o) / \rho \lambda} \quad (B18)$$

The freezing isotherm may be found by setting $T(x, y) = T_m$. In particular, the corner angle, $\theta_{\max}$, of this isotherm is given by

$$\begin{aligned}
\tan \theta_{\max} &= \left. \frac{dx}{dy} \right|_{\text{corner}} = \left. \left(\frac{\partial T}{\partial y} \right) / \left(\frac{\partial T}{\partial x} \right) \right|_{\text{corner}} \\
&= (\sin at/2) / (\cos at/2) \\
&\doteq h(T_m - T_o) / \rho v \lambda \text{ from Equation (B15)}
\end{aligned}$$

Thus,

$$\theta_{\max} = h(T_m - T_o) / \rho v \lambda$$

as in the first two models.

CHECKING (B13) AGAINST (B2)

Equation (B2), which must be satisfied along the freezing front, was ignored in deriving Equation (B13). From (B13), the gradient is

$$|\nabla T| = a(T_m - T_o) e^{-ax} / \cos at/2 \quad (\text{B19})$$

Noting that

$$a = (\rho v \lambda / k) / (T_m - T_o) \text{ [Equation (B16)]}$$

and

$$(T_m - T_o) e^{-ax} / \cos at/2 = (T_m - T_o) / \cos ay \text{ [Equation (B13)]}$$

We have

$$|\nabla T| \doteq (\rho v \lambda / k) / \cos ay \quad (\text{B20})$$

Comparing (B20) with (B2), we see that (B13) does not strictly satisfy (B2) because $\cos \theta \neq 1 / \cos ay$. However, θ and ay are both very small, so the numerical discrepancy is also very small.

INCLUDING CONVECTION

If convective heat transfer is included, Laplace's equation (B7) must be replaced by

$$d/dx (\rho c VT) - \Delta (kT) = 0. \quad (\text{B7}')$$

The other conditions, (B8) through (B12), are unchanged. A solution to (B7') is then

$$T(x, y) = T_o + (T_m - T_o) \cos ay e^{-bx} / \cos at/2 \quad (B21)$$

with a, b, and t satisfying

$$b = -(\rho cv/2k) + [(\rho cv/2k)^2 + a^2]^{1/2} \quad (B22)$$

$$\tan at/2 = h/ak \quad (B23)$$

$$bt/2 = h(T_m - T_o) / \rho V\lambda \quad (B24)$$

The main effect of convection is to weaken the exponential decay. The magnitude of this effect is small, as can be seen by estimating the ratio of $(\rho cV/2k)$ to a . Since

$$a \doteq (\rho v\lambda/k) / (T_m - T_o)$$

this ratio is

$$(\rho cv/2k)/a \doteq c(T_m - T_o)/2\lambda \doteq (T_m - T_o)/3370$$

where $\lambda = 337$ cal/gm and $c = 0.2$ cal/gm/deg have been assumed. Hence, b is only slightly smaller than a ;

$$b \doteq a - (\rho cv/2k) \quad (B25)$$

CONCLUSIONS

None of the three models is entirely satisfactory, since each violates one or more known physical conditions. Model 3 comes closest, although a simple closed-form solution of Laplace's equation satisfying all the conditions is not likely. In our opinion, the evidence presented by the models is overwhelmingly in favor of a nearly planar freezing front.