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Planar Magnetic Component Development

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Planar Magnetic Component Development

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Abstract

By replacing hand-wound bobbins with printed circuit board technology, planar technology can produce magnetic components that perform more consistently and that have a lower profile. By combining these components with other circuitry on a printed circuit board, circuit construction is simplified.

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Planar Magnetic Component Development

Introduction

Traditional manufacturing methods for transformers and other magnetic components have worked well for over a century, but have several disadvantages. Building the component has required a sequence of manual operations, which results in an expensive component. Chemical waste is generated in some of the steps. Most importantly, small differences in how the operator builds the transformer contribute to variation among a component lot and there is an even wider variation when different operators are used.

To construct a transformer using the traditional method, an operator wraps a bobbin with a thinly-insulated copper wire with the required number of turns. These wires are secured with tape, and the process is repeated until all layers are added. The finished bobbin is placed inside a ferrite shell to complete the magnetic circuit. The operator then strips insulation from the wires and solders them on pins. The assembly is encased in some type of housing to hold the windings securely and to keep the ferrite element together.

Planar technology offers the following improvements:

- In essence, the hand-wound bobbin is replaced by a printed circuit board. Because the placement of the windings is controlled by a precise photolithographic process, transformers are standardized and are not affected by operator differences.
- Because wire stripping has been eliminated, chemical waste is reduced. This helps minimize our use of hydrofluoric acid or other dangerous chemicals.
- The soldering step in which wires are connected to header pins is eliminated. In fact, all soldering related to the magnetic component can be eliminated if the transformer windings fit on one circuit board, combined with conductors that connect all the electronic components.

Figure 1 shows an exploded view of a planar transformer. For low-voltage transformers, all the winding layers may be contained within the laminations in one printed circuit board. High-voltage transformers will require additional insulation between winding layers, and therefore will be implemented with several stacked circuit boards.

Figure 1. An Exploded View of a Planar Transformer

The planar coils are formed as a spiral conductor on each layer of a multi-layer circuit board. Conductors can be connected from layer to layer in series if a higher number of turns is desired, or can be connected in parallel to reduce winding resistance. Since the coils are formed by an etching process as part of the circuit board, the labor in making the coils is minimal and results in a cost savings over conventional wire windings. Holes cut in the multi-layer board permit the magnetic cores to be installed. The core halves form a partial shell around the windings in the board. The resulting magnetic component profile is similar in height to other components on the board. Examples of these components are integrated circuit packages, resistors, or capacitors.

Planar magnetic components are not yet common because industry has just begun to develop them. The primary advantages of planar transformers over conventional transformers are cost, control of

parasitic parameters, and height. The disadvantages are board area and expense of coil design changes. Stacking standardized winding modules could lead to very flexible manufacturing of magnetic components. This would allow products to be customized to a customer's needs.

This study did not involve sufficient quantities to obtain a good measure of the uniformity of parasitic capacitance and leakage inductance. The dc resistance of a planar winding is expected to have a greater tolerance than an equivalent round conductor. The resistance tolerance of round conductors ranges from approximately $\pm 2\%$ for number 30 wire gage to $\pm 8\%$ for number 44 wire gage. Etched conductors are approximately $\pm 15\%$ tolerance. The variation for etched conductors includes line widths and deviation in the stock copper thickness and resistivity.

Low profile cores are not as efficient for conductor space as a core that approaches the shape of a cube. In addition, the coils etched on a thin circuit board have a significant amount of the core window filled with insulation rather than conductor.

Multi-layer circuit boards are more expensive than single-layer boards, but have the advantage of easy series / parallel connections for multiple coil layers. The coils are connected by vias. After the boards are connected, all that remains is to mount the cores. By deleting the cost of qualification acceptance and by eliminating the need to handle individual transformers, Sandia could reduce its applications cost considerably.

Future development could increase the ratio of copper to insulator in the core window. Techniques for enclosing the entire conductor in insulation are needed for high-voltage applications. Circuit applications that reduce the number of turns (that is, high frequency, low voltage) will help move planar designs from the drawing board to the marketplace.

Planar Coil Design Considerations

Winding resistance is a major factor in transformer and inductor design. This is especially true for planar coils, since low profile cores tend to reduce winding

volume. (See Figure 2). The area filled by conductors on a printed circuit board (Figure 3) is much less than an identical core that uses a conventional wire-wound bobbin (Figure 4). Finally, the resistance variability of an etched conductor is higher than a drawn round wire with a similar cross-sectional area.

Figure 2. Winding Volume Effect in Low Profile Cores. The half-height core on the right also has half the winding volume.

As indicated above, if one half of a core is used to give a low profile (height), a flat plate is required to complete the magnetic path. Thus, the winding volume is cut in half, but the core volume is less than half since the total height becomes that of the half-core plus the flat plate. As the core profile is further reduced, the winding volume decreases faster than the core volume. Thus, low profile cores tend to require a larger core volume for a given application.

Figure 3. Only 20% of This Planar Coil Cross Section Is Filled with Copper. The cross-hatched areas are copper.

Figure 4. Conventional Wire-wound Coils May Have 70% Area Filled with Copper. The cross-hatched areas are copper.

Planar Layout Issues

Two important issues in designing planar magnetic components are the winding resistance (or current-carrying capacity) and parasitic parameters. When designing current-viewing transformers (CVTs), minimizing winding resistance is the primary concern because as voltage across the winding increases, the ability of the transformer to represent the current present through the primary is diminished. But for power components, minimizing power loss is more important. Planar coils have inherently better control of parasitic winding parameters. Three parasitics of interest are the capacitance between windings, capacitance within windings, and leakage inductance (short circuit inductance). All three of these directly depend on winding geometry. Control of these parasitic parameters is especially important for higher frequency transformers. Planar coils have nearly identical geometry from unit to unit; thus, the planar transformer's in-circuit performance will be more consistent than the conventional wire wound coil's performance.

Planar Winding Resistance

We select the cross-sectional area of conductors for a power application based on its anticipated current, which approximates the desired concern of minimizing power losses. Conservative designs allow as much as $0.6 \times 10^{-6} \text{ m}^2$ conductor area per amp. For applications like current-viewing transformers, the issue is still the loss in the conductors, but the focus is on winding resistance. The limitations on the cross-sectional area of a trace are the copper thickness and the maximum trace width that will fit in a given core size. In the normal manufacturing of printed circuit boards, thicknesses up to $100 \mu\text{m}$ (3 oz copper per square foot) are available.

The resistance calculation of an etched spiral can be approximated by using successive circles with each conductor's mean radius and the cross sectional area. This resistance calculation technique is shown in Appendix A. In fact, the actual layout of printed circuit boards more closely resembles concentric circles than a spiral, so this approximation is acceptable.

The first multi-layer design we attempted had poor performance because transformer conductors with an insufficient cross-sectional area were used. A plating thickness of $16 \mu\text{m}$ copper and tracing widths of $100 \mu\text{m}$ were attempted. The resulting conductor losses affected the performance of both the flyback transformers and the current-viewing transformers. For efficient energy storage in an inductor, the pulse duration t should be less than a tenth of the inductance divided by the total winding and circuit resistance:

$$t < 0.1 \cdot \frac{L}{R_{total}}$$

If the pulse duration is too long, more energy is transferred into the resistor and considerable energy is dissipated. Example calculations illustrating this relationship are shown in Appendix D.

The best industry capability for etched circuits on a printed circuit board is presently about $75 \mu\text{m}$ conductor width with $75 \mu\text{m}$ spacing between conductors. The transformers in this project required more conductor cross-sectional area than could be obtained with the minimum width. Five turns on each side of the printed circuit board was the maximum used. The current transformer required 50 turns on the output winding, which was achieved by connecting ten 5-turn coils in series. Several printed circuit boards were stacked and the coils connected in series where several turns were needed, and in parallel where current-carrying capacity was needed. These coils were interleaved to improve the coupling coefficient. Figure 1 shows how the coils could be stacked.

Power loss in the planar coils and in the core should be calculated and used to estimate the temperature

rise of the transformer. The McLyman *Transformer and Inductor Design Handbook* (Reference 1) is a good source for this information. If the result yields an unacceptable temperature, a design using a larger core may be necessary. Optimum designs usually have the core losses nearly equal to the copper losses. If the core losses are high, the operating flux density should be reduced. If the copper losses are high, the cross-sectional area of the conductor should be increased and its length should be reduced where possible. High frequency skin effects on the conductor should be considered as well. If the dc resistance is acceptable and the ac resistance is not, paralleling sets of thin conductors may help.

G. E. Bloom's *Final Project Report*² gives details of a *core geometry factor* design technique. This technique is used to obtain the planar core and winding relationships for the transformers designed by e/j Bloom. Rather than using a conductor current capacity, this technique begins with a specification of conductor power loss, and then determines the conductor cross-sectional area.

Leakage Inductance

Leakage inductance, or self-inductance, occurs when some of the magnetic flux generated in one winding does not link to another. This reduces the linkage between coupled inductors. The two generalizations listed below apply when a high coefficient of coupling is required in a transformer design.

1. Keep the coil windings as close together as possible. Interleaving the coils is an effective way to do this, especially since planar coils lend themselves well to interleaving. Alternating layers of primary and secondary windings is the best approach, if possible. This is demonstrated later in the *Evaluation of Designs* section with one of the transformer designs, where two different interleaving patterns were tried. Lower leakage inductance is obtained as the coupling coefficient approaches 1, where 1 is perfect coupling. High leakage inductance translates into higher power losses for a switch-mode power converter.
2. Place the windings around as much of the core length as possible. Toroidal cores wound over

their entire 360 degrees are the most effective in this regard. Solenoidal wound coils covering a portion of the core length are not as good.

Printed Circuit Board Layout

Planar coils etched on printed circuit boards are especially cost effective where multi-layer circuit boards are used. The coils are part of the board conductor pattern. Board interconnects are made, holes are machined in the board, and the magnetic cores are mounted in the holes. Considerable fabrication time is saved compared to winding a coil with wire, soldering the coil wires to a mount, and then soldering the mount into a circuit board.

Five areas need attention when the path of windings is chosen during board layout:

- Cut-out regions for the transformer core
- Trace to edge spacing
- Trace width and trace-to-trace spacing
- Via diameters
- Stock material copper thickness.

First, an area is cut out of the board. This cut-out allows the transformer core to be inserted through the board. The area drawn must consider available routing bit sizes and normal component tolerances.

Second, the proximity of copper traces to the cut out region is a manufacturing constraint. Most board manufacturers will accept 500 μm spacing (0.020 in.) in the design. After machining, they require a minimum of 250 μm .

Third, copper trace widths and spaces between traces is another manufacturing constraint. Although industry capability is 75 μm lines and spaces (0.003 in.) as mentioned in the "Planar Winding Resistance" section, boards designed with these dimensions are difficult to manufacture with high yield. Normal dimensions for standard manufacturing practices are about twice this, or about 150 μm .

Fourth, the diameter of vias used to interconnect winding layers usually becomes a constraint because of the fine diameters needed (400 μm to 600 μm), and because of the accuracy in drilling the hole in the center of the land, with annular ring requirements of more than 175 μm .

Fifth, the thickness of copper used can cause a problem for timely delivery of materials. Stock with 65 μm copper thickness (2 oz) is usually readily available. Using stock material of the desired thickness (rather than plating copper to meet the requirement) is preferred because it maintains trace dimensions and provides the lowest resistivity.

Transformer Testing

Discrete planar magnetic components can be tested using the same procedures as other components. Where planar transformers are part of the etched circuit, additional testing may be required to verify correct operation of the transformer. Additional tests may include assembling the magnetic components on the board with no other devices, and then measuring the usual inductive properties. It may be possible to measure an insulation resistance between windings before components are installed on the printed circuit board and to perform the test at a somewhat higher voltage than normally applied in the circuit. The normal continuity testing and capacitance measurements used to evaluate printed circuit boards may provide sufficient evidence that a planar transformer will operate properly when the core is added. Then, functional tests that focus on the magnetic component may be added to the tests chosen to evaluate the assembled circuit board. For example, in a circuit that incorporates a current-viewing transformer, some stimulus could be applied and the transformer's and the rest of the circuit's response could be measured.

Planar Design Contract

To encourage planar technology at Sandia, we chose to initiate a consulting agreement with a technical partner. Before placing the contract, Sandia designed a demonstration circuit with transformer windings included in the circuit board. This design was only marginally successful, but did provide a basis for later work with the technical consultant.

Placing the Contract

An initial request for quotation (RFQ) is provided in Appendix B. Initially, the RFQ required the contractor to construct a power converter as part of the statement of work (SOW) to demonstrate planar magnetics. This RFQ was sent to several magnetic

component manufacturers. The only response was from e/j Bloom and Associates, Inc., and their quote exceeded the available funding. Thus, we prepared a new statement of work. This SOW was written to design only discrete planar transformers instead of circuits with planar transformers. (See Appendix C). This time Sandia received quotes from: e/j Bloom and Associates, Inc., Cypress Magnetics Inc., Electromagnetic Components Inc. and Remtec, and the quotes were within our funding capability. Following a review to evaluate the technical merits of each proposal, the contract was placed with e/j Bloom and Associates.

Contractor Meetings

An initial meeting was held with Mr. Bloom on September 3, 1993 to review the requirements. Design considerations for the transformers were reviewed and some alternatives were discussed. The initial design for power and current-viewing transformers (CVT) was critiqued. This led us to modify the specifications for the CVT. A larger core would be used to lower the winding resistance. The application circuit was also reviewed and suggestions were made to improve the circuit and its associated transformers.

A second meeting was held with Mr. Bloom on December 3, 1993. By then, the transformer designs had been completed, hardware had been ordered and some hardware had been received. Design specifications for all the transformers were reviewed. Our discussion centered on the assembly of parts, including one set of parts that would be stacked but not electrically connected. We agreed to experiment with different stacking arrangements of the power transformer to demonstrate the effects of stacking sequence on leakage inductance. The Sandia breadboard circuit design was operated and some design changes were suggested. This circuit was later used to evaluate the Bloom transformers.

Design of a Planar Magnetic Evaluation Circuit

Sandia designed three circuit boards to evaluate the performance of planar magnetic components in a circuit. The first was a multi-layer circuit board with

the transformer windings included in the board. The second was a simple double-sided board using planar components that were assembled separately and attached as discrete components. Based on the results of this second design, a third design was implemented by Sandia as part of a separate project that included transformer windings within the circuit board, but it is not discussed here.

Circuit Requirements

The evaluation circuit board contained the following sections (a schematic is shown in Appendix F):

- An 8 W power converter accepting 8-V to 12-V input voltage and producing 5-V, 0.4-A and ± 15 -V, 0.2-A outputs.
- A 2 W power converter accepting 8-V to 12-V input voltage and producing a -35-V output.
- Two 0.8-J capacitive discharge units (CDUs).
- Two current-viewing transformers, one for each CDU, monitoring a 50-A peak pulse.

The intent of the evaluation board was to include typical magnetic component functions that are encountered in Sandia designs. Both power converters use the flyback topology, an integrated design in which the magnetic component has energy-storage functions like an inductor, but that also includes voltage conversion like a transformer. (Though technically not just a transformer, we refer to a “flyback transformer” from this point forward.) The first power converter could supply normal digital and analog circuits. The -35-V converter charges the CDUs. Note that a negative voltage was used for the CDU, something not possible without a switch-mode power converter. The negative voltage facilitates the use of n-channel field-effect transistors, which have a lower on resistance than equivalent p-channel devices that would be used to switch a positive CDU voltage. Current-viewing transformers are routinely used to monitor the performance of CDUs and perform that same function here.

Current-Viewing Transformer (CVT) Design

CVTs allow us to measure the current flowing through a circuit without significantly changing that circuit’s impedance. The ability of a CVT circuit to reproduce the input current waveform diminishes with increasing duration of the current pulse. The equation below is for a rectangular pulse and relates the duration of a voltage across a CVT with other parameters:

$$N \cdot B \cdot A_c = L \cdot I = V \cdot t \quad (\text{Eqn. 1})$$

Because of component limitations, some loss in fidelity must be tolerated for a practical design. For our demonstration circuit, we wanted to monitor the output of a CDU, which appears like an exponential decay function. The important part of the waveform for this application is the initial peak current, so the time factor t in the equation above can be short. Thus, 100 μ s was used. Figure 5 shows the schematic of a current source, transformer, and resistor load.

Figure 5. Schematic Showing a Current Source, a CVT, and a Load

CVT designs are normally specified with a “volts per amp” rating. That is, if 1 amp in the primary winding (N_p) gives 5 volts across R , this is 5 volts per amp. The basic relationship then is:

$$\frac{V_{out}}{I_{in}} = R \cdot \frac{N_p}{N_s} \quad (\text{Eqn. 2})$$

To determine the number of secondary winding turns N_s , Equation 1 can be rearranged:

$$N_s = \frac{\int V(t) \cdot dt}{A_c \cdot \Delta B} \quad (\text{Eqn. 3})$$

where:

- ΔB $\equiv$ Desired change in the magnetic flux density, Tesla
- A_c $\equiv$ Cross-sectional core area, m^2
- N_p $\equiv$ Number of primary turns
- N_s $\equiv$ Number of secondary turns

If a low impedance device is used to sense the voltage across R, that impedance in parallel with R should be used to determine the V/I rating of the transformer. If the winding resistance is significant compared to R, then V(t) used to calculate the number of secondary turns, N_s , in Equation 3 above should include the voltage drop of the winding resistance plus the load resistor R for the total voltage generated in the secondary coil.

If it is necessary to have $N_p = 1$ turn, then with V, I, and N_p fixed, unknowns in the equation are reduced to R/N_s and a selection of one determines the other. For good fidelity, the secondary winding impedance should be much greater than the load resistance R, $X_L(N_s) \gg R$, and ΔB should be checked to verify the core is not being driven to saturation or excess heating.

For example, consider a single-turn primary to measure a 50 A peak output of the CDU. The pulse has a fast rise and exponential decay with about a 1-ms time constant and 2 pulse per second duty cycle. An output of 0.05 V for 50 A input is desired, but only the peak value is important, so good fidelity beyond 100 μs is not required. Substituting these values into Equation 2 above, $R/N_s = 0.001$. If we choose $R=0.05\Omega$, then N_s equals 50 turns.

Note that if R were selected to be 0.1 Ω , then the N_p would be 100 which is quite a few turns for a planar design. If we try a Philips RM5 square core constructed using 3F3 ferrite, the secondary winding resistance comes out to be 5 Ω , assuming 10 layers of 5 turns per layer. This appears too high, and in any case, would be difficult to implement on the printed circuit board. Instead, we will try a RM6S core. The secondary winding resistance comes out to be 1.6 Ω and the inductance equals 4.9 mH. The voltage across the winding secondary is the total resistance, which includes the winding resistance R_{wdg} , times the current in the secondary:

$$V(t) = (R + R_{wdg}) \cdot I_0 \cdot e^{-R/L} \quad (\text{Eqn. 4})$$

The magnetic flux density change ΔB is calculated by rearranging Equation 3 and substituting Equation 4 for the voltage:

$$\Delta B = \frac{R + R_{wdg}}{N_s \times A_c} \int_0^{10^{-4}} I_0 \cdot e^{-R/L} \cdot dt \quad (\text{Eqn. 5})$$

Now ΔB is equal to 0.1035 Tesla. This is acceptable for a unidirectional pulse, as shown in the 3F3 ferrite B-H loop in Figure 8. Since the pulse is longer than 100 μs duration, ΔB is greater than calculated, so core loss per pulse is relatively high. However, a low duty cycle keeps the core from running too hot. The reactance of the transformer secondary, X_{Ls} , is calculated to be 154 Ω for a frequency of 5000 Hz. This is well above the 1.65 Ω winding and load resistance, so the transformer should satisfactorily measure the peak current.

Flyback Topology Power Converter

The purpose of a power converter is to convert the input voltage and current efficiently into the required output voltage and current. Switch-mode power converters (SMPCs) are inherently more efficient than linear converters above some minimum power because the output current in an SMPC does not have to be the same as the input current.

For example, to provide a 5-V, 1-A output from a 30-V input, a linear converter must dissipate 25 W for an efficiency of 17%, while the efficiency of an SMPC would be above 70%. Looked at another way, while SMPCs drive semiconductors as switches, either on or off, linear converters operate semiconductors in the linear mode. This requires larger semiconductor components to dissipate the heat and larger capacity energy sources. Other limitations of a linear converter are a lack of voltage inversion (no negative output) and no electrical isolation. However, the linear converter is less complex and does not produce the high-frequency switching noise of an SMPC.

A flyback SMPC stores energy in a magnetic field during the first part of a cycle, and then transfers that energy to the load during the second part. The energy

transfer for this particular design is discontinuous³ because no residual energy remains in the transformer at the end of a cycle. The duty ratio, δ , is the fraction of time spent in the first stage with respect to the total length of a cycle. The name flyback comes from the circuit's early use in cathode ray tubes, where it was used to drive the beam trace back before starting the next horizontal scan. The spot of light appeared to "fly back" to the edge of the screen.

In a flyback converter, the transformer plays three roles: storing and transferring energy, ratioing multiple output voltages, and (if desired) providing electrical isolation. Capacitors are required to supply current to the transformer during the first part of the cycle and to act as a buffer for current on the outputs. Energy is controlled with power field effect transistors (FETs) and diodes. Figure 6 shows a model of a flyback power converter.

Figure 6. Flyback Converter Model

Overview of Design Features

Power must be provided to the SMPC control integrated circuit, in this case a Unitrode UCC2805D. For many applications, a separate supply circuit is used for steady-state operation and a temporary (or "bootstrap") energy source is needed to initially power the circuit. In this case, the control integrated circuit will operate over the 8-V to 12-V input voltage, so it is driven directly with the supply voltage. No protective circuitry was added to limit the supply voltage to below the level that would cause damage to the chip or to the power FET gate. The current-limiting feature of the UCC2805D was used; this allowed the converter outputs to be shorted indefinitely. Neither converter takes advantage of

input-to-output isolation that is possible with this topology.

Power is directed with both a controlled switch (transistor) and naturally commutated switches (diodes). A single FET is used to switch power into the transformer. Heat sinks are not required because the thermal resistance through the FET to the printed wiring boards is low enough to dissipate the small amount of heat generated by the FET. Diodes were selected for their current-carrying and peak-inverse voltage capacity, and for their forward voltage. Some compromises are necessary. For example, Schottky diodes have low forward voltages, but also have low peak-inverse-voltages.

Flyback Transformer Equations

References are available, like Reference 4, to assist in designing a power transformer. The following analysis begins with first principles to derive the important design equations. When the power FET is turned on, current through the transformer primary increases linearly (assuming that the on time is much less than the magnetizing inductance divided by the resistance, and that the magnetic flux density does not exceed saturation). The function of current over time depends on the applied voltage V , the magnetizing inductance L_m , and time, t :

$$i_m(t) = \frac{V}{L_m} \cdot t \quad (\text{Eqn. 6})$$

Energy stored in the transformer is delivered to the load when the power FET turns off. Thus, the transformer's output current linearly decreases. The switching cycle time (T_s) is the sum of the time that the FET is on plus the time it is off:

$$T_s = T_{on} + T_{off} \quad (\text{Eqn. 7})$$

An important point is that the time to fully discharge the magnetic energy stored in the inductance must be less than or equal to the time that the FET is off. If the FET turns on before the magnetic field is exhausted, the circuit moves into continuous mode. Since the transformer was not designed for this region, it saturates.

$$T_{disch} \leq T_{off} \quad (\text{Eqn. 8})$$

Figure 7 shows the associated current and voltage waveforms of flyback power converter operation. When the time that the power FET is on (T_{on}) is substituted for time in Equation 6, the peak input current results:

$$\hat{I}_m = \frac{V_{in}}{L_m} \cdot T_{on} \quad (\text{Eqn. 9})$$

Figure 7. Flyback Converter Waveforms

This value is important as an indicator of the component stress levels. It may also limit the output power when the current limiting circuit is considered. Another important factor is the voltage across the FET. This value, $\hat{V}_t$, occurs when the FET is off and energy is being transferred to the output. In the ideal case, $\hat{V}_t$ equals the input voltage plus the output voltage multiplied by the turn ratio, as shown in Equation 10.

$$\hat{V}_t = V_{in} + V_o \cdot \frac{N_p}{N_s} \quad (\text{Eqn. 10})$$

Unconfined magnetic fields can degrade power converter performance and affect the operation of other nearby circuits. To confine the magnetic field as much as possible, "pot" magnetic cores are often

used. The ferrite in a pot core completely surrounds the bobbin on which the conductors are wound except for narrow openings where the wires exit. With planar magnetics, windings are imbedded in printed circuit boards. Wider openings in the core are required for the conductors to emerge. For these designs, square cores were used with almost 180° open on the core. The transformer design is a function of several constraints:

- Power to be delivered to the load
- Minimum input voltage
- Maximum duty ratio
- Switching frequency
- Magnetic material and core properties.

Choosing the Magnetic Core

Gapped cores are usually used for flyback transformer designs because the energy capacity of a gapped core is much higher per unit volume than is an ungapped core. Design guides are available to assist the selection of cores.⁵ The energy stored is the volume of a region times the energy density within the region. The magnetic field density remains constant through the magnetic material and across a gap. The magnetic energy stored in a gapped-core inductor is then the sum of the energy in the core and in the gap:⁶

$$W_m = l_c \cdot A_c \cdot \frac{B^2}{2\mu_c} + l_g \cdot A_c \cdot \frac{B^2}{2\mu_o} \quad (\text{Eqn. 11})$$

where:

- W_m ≡ Magnetic energy, Joules
- l_c ≡ Core magnetic path length, m
- l_g ≡ Gap length, m
- B ≡ Magnetic flux density, Tesla
- A_c ≡ Cross-sectional core area, m²
- μ_o ≡ Permeability of free space, $4\pi \times 10^{-7}$
- μ_c ≡ Permeability of core.

For the pot cores used, the cross-sectional area of the core and the gap are both equal to A_c , so the respective volumes of the core and gap are the magnetic path length of each, times the cross-sectional area. Because the permeability of the core is more than a thousand times that of free space, the energy stored in the core is much smaller than that stored in the gap, and the core energy can be ignored. As a result, the maximum power capability of a

particular core depends on the gap volume, the maximum magnetic field density in the material, and the operating frequency:

$$P_{\max} = l_g \cdot A_c \cdot \frac{B_{\max}^2}{2\mu_o} \cdot f_s \quad (\text{Eqn. 12})$$

where:

$P_{\max}$ $\equiv$ Maximum power, Watts

$B_{\max}$ $\equiv$ Maximum magnetic flux density, Tesla
(usually half B_{sat})

f_s $\equiv$ Permeability of core.

The appropriate core can be selected by comparing the power requirements with core power capacity. An additional consideration when selecting a core is the winding area that is required. As shown later when the number of primary turns is calculated, the number of turns is inversely proportional to the core cross-sectional area. Thus, a smaller core may meet power requirements but may be impractical when the number of turns is considered.

Determining the Magnetizing Inductance

To deliver a specified power, an inductance is calculated that will store the necessary energy when the minimum rated input voltage is applied. Two operating modes are possible for a flyback converter: continuous and discontinuous conduction. Continuous conduction means that not all the energy stored in the inductor is used each cycle, so a larger transformer volume is needed for the higher total energy. Because the current never decreases to zero (it is continuous), the ripple in the input and output current is lower. However, with non-zero current being switched twice as often, the amount of switching noise is doubled.

For this design, discontinuous conduction mode was chosen to minimize transformer volume and switching noise.

Power supplied to the converter is the input voltage times the average current. The transformer's input current waveform ramps from zero to a peak current $\hat{I}_m$, expressed in Equation 6, with a duty ratio δ . The average current is then:

$$I_m = \frac{1}{2} \hat{I}_m \cdot \delta \quad (\text{Eqn. 13})$$

Substituting the above into the relationship for input power and rearranging the equation, we have:

$$\hat{I}_m = \frac{2P}{V_{in} \cdot \delta} \quad (\text{Eqn. 14})$$

and then substituting $\hat{I}_m$ for $i_m(t)$ at time δT_s in Equation 6, we have:

$$L_m = \frac{V_{in}^2 \cdot \delta^2 \cdot T_s}{2P} \quad (\text{Eqn. 15})$$

If the maximum power capacity of the selected core is not used in the above equation, the inductance will be larger. As a consequence, a higher number of turns will be required. However, ripple will be higher with a significantly over-designed transformer; peak currents will also be higher. Usually, the volume available for winding is restrictive enough that the fewer turns will be gratefully used, especially for planar components, which are much more difficult to design with many turns. If the maximum core power, Equation 12, is substituted, we have the inductance required for the maximum power of a given core:

$$L_m = \frac{V_{in}^2 \cdot \delta^2 \cdot 2\mu_o}{l_g \cdot A_c \cdot B_{\max}^2 \cdot f_s^2} \quad (\text{Eqn. 16})$$

$$T_s = \frac{1}{f_s}$$

Since a gapped core is used, the inductance is essentially independent of the magnetic material properties:

$$L_m = \frac{\mu_o \cdot A_c \cdot N^2}{l_g} \quad (\text{Eqn. 17})$$

The core material properties (and conductor resistance) limit the usable peak current. As the maximum magnetic field density is exceeded, the relationship between the field density (B) and the intensity (H) becomes non-linear. The field density increases more slowly with intensity until the core is

"saturated" and the magnetic field density cannot increase further. When this condition occurs, the inductance becomes very small and the current very large. Because the power FET is switching this current, its ratings are rapidly exceeded and the device is destroyed unless a current limiting feature is used. A maximum operating magnetic field density B_{max} is chosen below the non-linear region of the B-H curve. (See Figure 8).

Figure 8. The B-H Curve for Philips 3F3 Ferrite⁷

Assuming constant input power, a minimum input voltage produces the maximum peak current and requires the largest duty ratio. Using these minima and maxima and equating the two inductance Equations 16 and 17 and rearranging terms, the maximum number of primary turns, N_p , that ensures operation at the minimum input voltage is:

$$N_p = \frac{V_{in,min} \cdot \delta_{max}}{B_{max} \cdot A_c \cdot f_s} \quad (\text{Eqn. 18})$$

If this number of turns is exceeded, the inductance will be higher than desired, and the magnetic flux density will be insufficient at the minimum operating voltage. Conversely, if fewer turns than this are used, the peak current and peak magnetic flux density may be higher than desired.

Choosing a Secondary Turn Ratio

The ratio of the input voltage to output voltage for a flyback converter can be found by viewing the flyback as a buck and a boost converter in cascade. The voltage ratio is then the product of the two converter voltage ratios. With the transformer added to the circuit, the voltage ratio becomes:

$$\frac{V_o}{V_i} = \frac{N_s}{N_p} \frac{\delta}{(1-\delta)} \quad (\text{Eqn. 19})$$

A voltage must be added to the output to compensate for the drop across the rectifier. Adding this factor and rearranging terms, the equation for the secondary turn ratio is:

$$(\text{Max.}) \quad \frac{N_s}{N_p} = \frac{(V_s + V_{diode})(1-\delta_{max})}{V_{in,min} \delta_{max}} \quad (\text{Eqn. 20})$$

This is the maximum turn ratio that can be used and still keep the converter operating in the discontinuous mode. The minimum number of turns is defined by the maximum voltage stress that the FET will tolerate. The ideal situation was described in Equation 10. In reality, an extra factor needs to be included because some ringing occurs when the FET first turns off. A factor of 1.3 times the voltage reflected from the secondary is commonly used. Rearranging Equation 10 and including this factor, gives:

$$(\text{Min.}) \quad \frac{N_s}{N_p} = \frac{1.3 (V_o + V_{diode})}{\hat{V}_i - V_{in}} \quad (\text{Eqn. 21})$$

Load changes to one output of a multi-output converter may affect different outputs to varying degrees because the magnetic field is not perfectly coupled through each transformer winding. This lack of coupling, called leakage inductance, causes transformer voltages to vary from values predicted by turn ratios.

Applying the Equations

Under the contract with e/j Bloom and Associates, prototype magnetic components were developed. These components use an RM6S core that has been modified to increase the opening through which conductors will emerge. The effective core cross-

sectional area after modification is similar to an RM5S core. For illustration, the equations derived in the *Flyback Transformer Equations* section of this report are applied to a standard RM6S core.

For a given power requirement, several cores may have sufficient capacity. Because the losses in the ferrite are proportional to core volume, generally the smallest core with the necessary capacity is chosen. However, the volume available for conductors may force the use of a larger core. For this design, the output power is 8 W, and an efficiency of 70% is assumed to cover transformer and rectifier losses. Therefore, a 11.5-W core is needed.

The calculated number of primary turns is based on a minimum input voltage, $V_{in,min}$ of 8 V, and on a maximum duty cycle, δ_{max} of 0.45. A 200 kHz switching frequency was chosen. Square cores are used to be compatible with the planar, printed circuit board construction. Based on the RM series from Philips and their 3F3 ferrite, the RM6SPA100 core was selected and will be operated with a B_{max} of 0.15 Tesla. Substituting these values into Equation 18, a primary of 3 turns is required. Based on a maximum FET voltage rating of 40 V and a forward voltage drop of 0.6 V on the diode, the +5 V secondary to primary turn ratio must fall in the range of 0.26 to 0.86. A ratio of 0.33 (or a 3:1 primary to secondary ratio) was chosen. The other secondary turn ratios are derived from the +5 V ratio. For the +15 V and -15 V outputs, three turns each are used. The calculations producing these results are shown in Appendix E.

The complete winding listed for the flyback transformer is shown in Table 1. Because increasing the number of turns leads to either a larger number of circuit board layers or to narrower traces, multi-tap opportunities can be taken to combine windings. For example, the +15-V output was created by adding two turns on top of the +5-V output.

Table 1. Winding for the 3-Output Flyback Transformer

Board Layer	Voltage	Turns
1,4&5,8	Primary	3
2, 7	+5	1
3, 6	±15	3

For the CDU power converter, the input power required with a 2-W output power and a 70% converter efficiency is about 3 W. Using a B_{max} of 0.15 Tesla, the closest part is a RM6SPA250 core, capable of 8.4 W. Using this as the power in further calculations, the primary is determined to be 3 turns. The secondary must fall between 5 and 16 turns based on component stress and on the continuous /discontinuous boundary. A secondary of 10 turns is chosen. The results are summarized in Table 2.

Table 2. Winding for the -35 V-CDU Flyback Transformer

Board Layer	Voltage	Turns
1,3&6,8	Primary	3
2&7, 4&5	-35	10

A model of the flyback transformer, Figure 9, shows the magnetizing inductance L_m , an ideal transformer to relate turns, and leakage inductances L_p on the primary side and L_s on the secondary side. Because the leakage inductance is not coupled, the leakage inductance appears as a separate inductor in series with the load, and voltage is dropped across it. Winding resistance also contributes to the voltage drop, but is usually insignificant. If the load is decreased on the +5-V output in the multiple-output flyback transformer, the reduced demand reduces the voltage drop across the secondary leakage inductance. This drop is compensated by the feedback circuit, but the voltage decreases slightly on the other two outputs because the transformer turn ratio reflects this lower voltage on their windings.

For example, with full loads on all outputs of the of the demonstration power supply, the results are +5 V, +17 V, and -17 V. When only the +5-V output load is reduced to 10% of full load, the supply generates

+5 V, +14 V and -14 V. As a second example, if full loads are placed on all outputs except for 10% of full load on the +15-V output, +5 V, +22 V and -17 V are generated.

This cross-regulation problem may be tolerable if the load is constant and if voltage variances can be compensated with design tuning. Because the affected voltages are for analog circuitry in this design, a wider variation is acceptable.

Figure 9. Model of a Multiple-output Flyback Transformer

Planar Transformer Design

Once the basic design of the magnetic component is complete, it can be implemented using planar technology. Choosing a planar format actually affects the transformer design, since the number of turns must be minimized for successful printed circuit board layout. The calculations shown in Appendix E for the transformer design examples used in the design section above include estimates on winding resistance and power loss; they also detail the transformer construction.

For the demonstration transformers, double-sided boards with 65- μm thick copper plating were used. Although thicker, 100- μm copper plating is available, the expected 50% lower resistance is not obtained because the etching process and thick copper on a thin board could reduce the reliability of the coil. CVTs T1 and T2 by e/j Bloom and Associates have a secondary winding composed of a stack of five double-sided boards with 5 turns on each side, for a total of 50 turns. The 1-turn primary winding was

stamped from 250- μm (0.010-in.) copper sheet with a thin layer of insulation applied to both sides that prevents shorting to other coils. Since no printed circuit board was used, the coils have improved copper space efficiency.

For the flyback transformers T3 and T4, the windings were again constructed using a modular approach. The primary and secondary windings for the transformers were interleaved to the maximum extent possible to minimize leakage inductance. The 10-turn primary of T3 was built from four double-sided boards in parallel, 5 turns on each side. Three of the same boards were connected in series for the 30-turn secondary. The basic module for T4 was a 2-turn double-sided board, one turn on each side. The 6-turn primary serially connected 3 board sets; each set was paired in parallel to reduce winding resistance. The secondary used these same boards to create a 2-turn output for the +5-V winding, and 6 turns each for the $\pm 15\text{-V}$ windings.

Capacitor Selection

Capacitors are required to supply and absorb current on both the input and output of the flyback converter. Electrolytic tantalum capacitors are frequently used in this function because they have an order of magnitude lower equivalent series resistance (ESR) than aluminum electrolytic capacitors. Multi-layer ceramic capacitors were used for this design because they have an order of magnitude reduction over tantalum capacitors in ESR, and in addition have reduced equivalent series inductance (ESL) due to the package configuration⁸. Values considerably larger than the minimum theoretical values are usually used for electrolytic capacitors to compensate for the ESR and ESL, but this increase is unnecessary with multi-layer ceramic capacitors. The capacitance required depends on the average current, on the switching current waveform, and on the switching frequency.

Input Filter Capacitor

The size of capacitor is determined by the amount of charge that needs to be supplied and the voltage change tolerated as that charge is delivered. Figure 10 shows the input current waveform. The two shaded areas (Q1 and Q2) show that the integrals of the current above and below the average current are

equal because the average capacitor current must be zero.

Figure 10. Flyback Input Current Waveform

These areas represent the charge delivered and stored, respectively, by the capacitor. The change in charge, ΔQ , is equal to the capacitance value C times the change in voltage over time:

$$\Delta Q = \frac{\Delta V}{\Delta t} \cdot C \quad (\text{Eqn. 22})$$

The charge defined by the first shaded region in Figure 10 is the difference between the peak current and the average current times the duration that the current exceeds the average. The ratio of this duration to the duration represented by the length of the base is the current difference divided by the peak current. The equation for the change in charge is then:

$$\Delta Q = \frac{1}{2} \cdot (\hat{I}_m - I_m) \delta T_s \frac{(\hat{I}_m - I_m)}{\hat{I}_m} \quad (\text{Eqn. 23})$$

where:

- ΔQ $\equiv$ Change in charge, coulombs
- $\hat{I}_m$ $\equiv$ Peak magnetizing current, amps
- I_m $\equiv$ Average magnetizing current, amps
- δ $\equiv$ Duty cycle
- T_s $\equiv$ Switching cycle time, seconds.

Substituting the peak current in Equation 23 with the relationship in Equation 13 and rearranging terms, gives:

$$\Delta Q = \frac{1}{4} I_m (2 - \delta)^2 T_s \quad (\text{Eqn. 24})$$

Although this appears to show that a maximum charge occurs at zero duty cycle δ , obviously the average magnetizing current I_m would then also

become zero. To find the maximum value of ΔQ , the relationship between the average current and the duty ratio must be used. The largest average magnetizing current occurs at the maximum power and minimum input voltage, when the duty cycle becomes its maximum:

$$I_m = \frac{\delta}{\delta_{\max}} \frac{P_{\max}}{V_{in,\min}} \quad (\text{Eqn. 25})$$

The resulting cubic function of ΔQ with δ increases from $\delta = 0$ to a peak at $\delta = 0.67$, beyond the maximum value of $\delta_{\max}$ possible with the SMPC control IC used. Using the IC's $\delta_{\max}$ for δ and combining Equations 22, 24, and 25, the minimum theoretical value for capacitance is:

$$C_{in} = \frac{P_{\max} (2 - \delta_{\max})^2}{4 V_{in,\min} \Delta V_{in} f_s} \quad (\text{Eqn. 26})$$

Assuming:

- $P_{\max}$ = 8.0 W / 0.7 efficiency
- $\delta_{\max}$ = 0.45
- $V_{in,\min}$ = 8 V
- ΔV = 0.5-V fluctuation
- f_s = 200-kHz switching frequency,

the minimum theoretical capacitance is 8.6 μF . Although the next largest size would normally be used, the input voltage fluctuation is not very critical so the closest size available is used, which is 8.2 μF .

Output Filter Capacitor

The output filter capacitor is selected using similar equations, but usually much smaller ripple voltages are tolerated. Because the waveforms are just mirror images of those shown in Figure 10, the change in capacitor charge is just Equation 24 with I_o substituted for I_m , and $(1 - \delta_{\max})$ substituted for δ . The resulting equation for the minimum theoretical output filter capacitance is:

$$C_{out} = \frac{I_o (1 + \delta_{\max})^2}{4 \Delta V_o f_s} \quad (\text{Eqn. 27})$$

Table 3 summarizes the capacitor chosen for the input and each output, assuming $\Delta V_o = 75 \text{ mV}$.

Table 3. Power Converter Input and Output Capacitors.

<u>Voltage</u>	<u>Current</u>	<u>Theoretical Capacitance</u>	<u>Actual Capacitance</u>
Input	1.4 A	8.6 μ F	8.2 μ F
+5	0.4 A	14.4 μ F	16.4 μ F
± 15	0.2 A	7.2 μ F	8.2 μ F

The second design converts the 8-V to 12-V input to -35 V for use charging a CDU. For this design, only the input capacitor selection is a concern because the converter's output is used to charge the rather large CDU capacitors. Only a 1- μ F ceramic capacitor is used on the output to reduce the effects of high-frequency transients.

Power FET Heat Dissipation

Power FETs are operated in the ohmic region, where the on resistance R_{ds} is equal to the voltage drop across the FET divided by the drain current:

$$R_{ds} = V_{ds} / I_d \quad (\text{Eqn. 28})$$

The on-state losses can be calculated from the simple I^2R relationship, using the average current value. But the transistor is only in this mode for a fraction of the time, so that fraction, δ , must be multiplied:

$$P_r = (I_{m,rms})^2 R_{ds} \delta . \quad (\text{Eqn. 29})$$

The parameters required to determine the resistive power loss are as follows:

$$\begin{aligned} P_{\max} &= 8.0 \text{ W} / 0.7 \text{ efficiency} \\ \delta_{\max} &= 0.45 \\ V_{in,\min} &= 8 \text{ V} \\ R_{ds} &= 0.1 \Omega \text{ (IRFU020 FET)} \end{aligned}$$

and the power lost to device resistance is calculated to be about 0.1 W.

The other operating mode in a flyback converter function is while the transistor switches from off to on, or from on to off. Because this design is based on discontinuous energy transfer, the transistor starts with zero current when switched on and the off-to-on transition can be ignored. However, the on-to-off transition occurs when the current is at a peak and is usually many times larger than the on-state losses.

Because the magnetizing inductance acts as a current source forcing current through the FET during the transition, the current remains high until the voltage across the FET returns to the off state, after time t_{fall} . The resulting integral of power over this switching time, when multiplied by the switching frequency, represents the transient switching loss:

$$P_t = \frac{1}{2} \hat{I}_m \left(V_{in} + \frac{N_p}{N_s} V_{out} \right) t_{fall} f_s \quad (\text{Eqn. 30})$$

The worst-case condition will be at the minimum input voltage when the current is at its maximum. Using V_{in} equal to 8 V and δ equal to 0.45, the average magnetizing current (I_m) is calculated to be 1.4 A and then $\hat{I}_m$ is equal to 6.3 A. For the IRFU020 FET used, the value for t_{fall} is 37 ns (typical), and results in a switching transient power loss of 0.5 W. The total power loss from resistive and transient losses is $P_r + P_t$, which adds to 0.6 W. The thermal resistance from the device junction to its case, $R_{\theta JC}$, is 3.0 $^{\circ}\text{C}/\text{W}$ and the connection from the case to the circuit board is about 20 $^{\circ}\text{C}/\text{W}$; this leads to a temperature rise of about 15 $^{\circ}\text{C}$.

Evaluation of Designs

The planar magnetic components were evaluated both on the component level with discrete component testing, and as part of the circuit under operating conditions using the demonstration circuit.

Transformer Measurements

The inductance, the leakage inductance, and the winding resistance were measured for all assembled components. The data are shown in Tables 4 through 6. In the tables, the inductance is measured open circuit (OC), and the leakage inductance is measured short circuit (SC). Leakage inductance is measured across the secondary with the primary winding shorted. All data are from G. E. Bloom's *Final Project Report*².

For the CVT (Table 4), the secondary resistance was specified to be less than 4 Ω . This parameter is important because too large a resistance value will increase the secondary voltage, which degrades the capability of the CVT to reproduce the input current

pulse. No specifications were made for the other parameters, but their measurement provides some information on the consistency of the components.

Table 4. CVT T1/T2 Test Results.
Measurements were at ambient temperature. OC inductance was measured at 20 kHz. SC inductance was measured with L₄₋₅ shorted.

Serial #	R ₁₋₂ , Ω	R ₃₋₆ , Ω	L ₃₋₆ oc, mH	L ₃₋₆ sc, μ H
1	.003	1.64	3.64	28.69
2	.003	1.60	3.02	33.60
3	.003	1.68	3.32	35.30
4	.003	1.68	3.38	36.40
5	.003	1.74	3.92	24.72
6	.003	1.61	3.78	21.90
7	.003	1.64	3.81	23.30
8	.003	1.77	3.80	25.50

The sequence in which transformer windings are interleaved affects the component's leakage inductance. Two different interleaving patterns were tried on Transformer T3. Note that the leakage inductance L₁₋₂ SC in Table 5 is lower for transformer numbers 1 and 2 than for transformers 3 and 4. Seven each 10-turn boards were used to construct the 1:3 turn ratio transformer, with the primary windings using four boards in parallel, and the secondary using three in series. Transformer numbers 1 and 2 used the board interleaving sequence 1p, 1s, 1p, 1s, 1p, 1s, 1p (p = primary, s = secondary). The resulting short circuit inductance averaged 0.08 μ H. When the board interleaving was 1p, 1p, 1s, 1s, 1s, 1p, 1p, the leakage inductance averaged 0.32 μ H. Thus, the interleaving between the primary and secondary was in the best configuration for the former, and in the worst for the latter.

Specifications provided for Transformer T3 were the primary resistance R₁₋₂ less than 0.2 Ω , secondary resistance R₃₋₆ less than 2.4 Ω , primary inductance L₁₋₂ OC equal to 9.0 μ H $\pm$ 20%, and the leakage inductance L₁₋₂ SC less than five percent of the primary inductance.

Table 5. Flyback Transformer T3 Test Results.
Measurements were at ambient temperature. Excitation test frequency 20 kHz. OC inductance was measured with L₃₋₄ open and 0.5 A dc on L₁₋₂, SC inductance was measured with L₃₋₄ shorted.

Serial #	R ₁₋₂ , Ω	R ₃₋₆ , Ω	L ₁₋₂ oc, μ H	L ₁₋₂ sc, μ H
1	.0837	.995	9.4	.090
2	.0832	.936	9.1	.072
3	.0807	1.025	9.4	.344
4	.0822	.891	9.2	.312

Specifications provided for Transformer T4 were the primary resistance R₁₋₂ and secondary resistance R₇₋₈ less than 0.02 Ω , and secondary resistances R₃₋₄ and R₅₋₆ less than 0.08 Ω . The primary inductance L₁₋₂ OC was 3.0 μ H $\pm$ 20%, and the leakage inductance L₁₋₂ SC less than five percent of the primary inductance.

Table 6. Flyback Transformer T4 Test Results.
Measurements were at ambient temperature. Excitation test frequency was 20 kHz. OC inductance was measured with all secondaries open and 1.0 A dc on L₁₋₂, SC inductance was measured with all secondaries shorted.

(resistance in Ω , inductance in μ H)

S #	R ₁₋₂	R ₃₋₄	R ₅₋₆	R ₇₋₈	L ₁₋₂ oc	L ₁₋₂ sc
1	.0075	.0138	.0143	.0052	3.53	.11
2	.0072	.0135	.0141	.0044	3.58	.12
3	.0073	.0140	.0140	.0044	3.55	.11
4	.0073	.0133	.0145	.0047	3.56	.12

CVT Performance

Functional tests of the CVT were accomplished by charging the CDU's capacitor to a certain voltage, and then discharging the CDU through a 1.0 Ω resistor. The load resistor used for the CVT was 0.1 Ω , which is twice the value specified for design calculations. This change has little effect on the performance of the CVT, however, since the average secondary winding resistance is about 1.7 Ω . The voltage across the CVT load resistor is amplified by a factor of 100 using an operational amplifier.

Figure 11. CVT Test Data Showing the Linearity of the Output. Peak values were measured.

The output current was determined from the peak voltage measured across the $1\ \Omega$ CDU load resistor. Based on the difference between this value and the capacitor's charge voltage, the internal resistance of the firing circuit was calculated to be about $0.2\ \Omega$. The calculated volt-seconds product for the CVT was about $450\ \mu\text{V}\cdot\text{s}$, assuming a trapezoidal output waveform.

Power Converter Performance

The first attempt at planar design using a multi-layer circuit board performed poorly because of inattention to winding resistance. Line widths were too fine because a small RM5 core was used. The copper was also too thin since only $16\ \mu\text{m}$ thick ($0.5\ \text{oz./ft}^2$) copper was used. As a result of the high resistance, the power conversion efficiency was only 63%, and the CVT did not work. The efficiency for the new discrete-component planar design was 72% to 80%, with the load varying from 120% down to 50% of full load.

The converter was tested using an electronic load on the three output voltages: +5 V and ± 15 V. Performance was monitored with input voltages of 8.8 V, 10 V, and 11.5 V. The maximum output power measured was about 9.5 W at an input of 13 W, exceeding the design requirement of 8-W output power. The +5-V output, which was the voltage used for control feedback, remained at about 4.95 V. The ± 15 -V outputs were close to 17 V when the outputs were loaded evenly, and ranged from 22 V down to 14 V when the loads were uneven.

The second converter circuit on the demonstration board charges the CDU to about -35 V and was

intended to have an output power of 2 W. Tests were run using input voltages of 8.8 V, 10 V, and 11.5 V. An electronic load was used to provide a continuous current sink. This is different from normal CDU charging operation, where once the capacitor is charged, the power converter idles. Efficiencies ranging from 72% to 78% were measured over load conditions of 50% to 160% of full load. Charge time for a total of $2500\ \mu\text{F}$ was about 300 ms, implying an average output power of more than 4 W. The CDU voltage climbed rapidly for the first half millisecond, then leveled off until the CDU was fully charged at 300 ms. During the first phase, the converter was current limited. The capacitors are charged through $100\ \Omega$ resistance to limit the charging rate, and the power converter is limited to about 6-A peak current with a current-sensing resistor.

Cost Comparison

One reason for using planar magnetic components is to reduce costs. The two options for incorporating planar components into a design are:

1. Use separate circuit boards for the magnetics that then use some type of interconnection with the main circuit board.
2. Combine the windings into the normal circuitry in the board.

Because the magnetic component almost certainly will use more than four conductor layers, Option 2 is practical only for a design that already requires a multi-layer board. The incremental cost is then the increase from what is required to route the circuitry on the board to adding the windings. For a typical board that uses eight conductor layers, prototype quantities may cost \$150 per board. This cost drops to \$100 for four layers and to \$50 for a double-sided board.

A 12 in. by 18 in. panel could yield about 50 winding sets for an RM8-size component, or about \$3 per component, plus about \$3 for the ferrite core. Assembly consists of sliding the windings in a core half and gluing on a lid. Wire clips or encapsulation may be necessary if the final product does not use potting. Total cost, including the labor to test the

component and acceptance tester time, may be as much as \$50/unit.

The additional design effort to create masks for manufacturing printed circuit boards takes about 10 to 20 hours drafting time. This may be equivalent to time needed to create operator instructions when manually winding bobbins.

Cost experience with discrete transformers for Sandia applications varies from \$100 to \$1000 per unit. A CVT similar to the one in this report would cost approximately \$150. This includes hardware, fabrication, and acceptance testing.

Conclusions

Although planar magnetic components are relatively new, the technology offers several advantages. Component properties show less variation because the construction technique keeps the winding in the same relative position each time, and batch processes can be used if the components are all formed on one printed circuit board panel. Assembly is simplified, and labor is reduced. If the component windings are integrated within the same printed circuit board as other circuitry for the design, assembly steps and chemical waste are reduced as well. These advantages could easily translate into cost savings.

The steps used to design planar magnetic versions of a current-viewing transformer and a power converter flyback transformer have been detailed in this report, and include special considerations associated with planar techniques. Finally, we have demonstrated the use of planar components in a circuit.

References

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Appendix A: Resistance Calculation for an Etched Spiral

SPIRCOND.RLN Calculate the resistance of a spiral conductor

$t := .001 \cdot \text{in}$ conductor thickness in inches

$w := .020 \cdot \text{in}$ conductor width in inches

$s := .010 \cdot \text{in}$ conductor separation in inches

$n := 5$ number of turns

$r_0 := .05 \cdot \text{in}$ r_0 is the mean radius in inches at the start of first turn

$\rho := 2.10 \cdot 10^{-6} \cdot \Omega \cdot \text{cm}$ Pure copper is $1.678\text{E-}6$ Ohm-cm, but plating is higher.

Trace resistance (ρ , Width, Length, Thickness) $:= \rho \cdot \frac{\text{Length}}{\text{Width} \cdot \text{Thickness}}$

$i := 0..72 \cdot n$ $\theta_i := \frac{\pi}{36} \cdot i$ increment in 5 degree steps

$r_{i+1} := r_0 + \frac{w+s}{72} \cdot i$ $2 \cdot \left(r_{72 \cdot n} + \frac{w}{2} + s \right) = 0.439 \cdot \text{in}$ coil outside diameter, inches

$ri_i := r_i - \frac{w}{2}$ $ro_i := r_i + \frac{w}{2}$

$ls_i := \left[\left(r_i \right)^2 + \left(r_{(i+1)} \right)^2 - 2 \cdot r_{i+1} \cdot r_i \cdot \cos \left(\theta_i \right) \right]^{0.5}$ length of conductor segment in inches

$L := \sum_{i=0}^{72 \cdot n - 1} ls_i$ $L = 3.916 \cdot \text{in}$ length of conductor in inches

$R := \text{Trace resistance} (\rho, w, L, t)$ $R = 0.162 \cdot \text{ohm}$

The trace length on a transformer can be approximated by summing up the length of a series of concentric circles. In fact, the trace path on the printed circuit board may be closer to this approximation than a spiral. First, we define the inner radius that a trace would take in a transformer. (The distance from the cut-out edge of the board to the trace is a manufacturing constraint.) Then, the width of the band around the core center that is available for winding:

$$\text{Tr_to_Hole} := 0.020 \cdot \text{in}$$

$$\text{Radius}_{\text{RM5S}} := (0.097 \cdot \text{in} + \text{Tr_to_Hole})$$

$$\text{Width}_{\text{RM5S}} := (0.105 \cdot \text{in} - \text{Tr_to_Hole} \cdot 2)$$

$$\text{Radius}_{\text{RM6S}} := (0.127 \cdot \text{in} + \text{Tr_to_Hole})$$

$$\text{Width}_{\text{RM6S}} := (0.148 \cdot \text{in} - \text{Tr_to_Hole} \cdot 2)$$

$$\text{Radius}_{\text{RM8}} := (0.169 \cdot \text{in} + \text{Tr_to_Hole})$$

$$\text{Width}_{\text{RM8}} := (0.166 \cdot \text{in} - \text{Tr_to_Hole} \cdot 2)$$

The width of the trace that fits on this band depends on the number of traces and the spaces between the traces.

Spaces := 0.007 · in Choose 7 mills, an easily manufacturable value (at 2 oz copper)

$$\text{Trace_width}(\text{Width}_{\text{core}}, \text{Turns}) := \frac{\text{Width}_{\text{core}} - (\text{Turns} - 1) \cdot \text{Spaces}}{\text{Turns}}$$

The length of the trace is the summation of the lengths of each of the concentric circles. In reality, some transition is needed to connect from trace track to track between each of the circles, but this is ignored for this approximation.

$$\text{Trace_length}(\text{Turns}, \text{Radius}_{\text{core}}, \text{Width}_{\text{core}}) := \text{Turns} \left(\text{Radius}_{\text{core}} + \frac{\text{Width}_{\text{core}}}{2} \right) \cdot 2 \cdot \pi$$

For a 50-turn CVT, assume that 10 layers of 5 turns per layer are used, and that the copper thickness is 2 oz, or 0.00256 inches. Calculate the resistance for each of the three core sizes above:

$$\text{Trace_thickness} := 0.00256 \cdot \text{in}$$

$$\text{Tr_Len}_{\text{RM5S}} := \text{Trace_length}(5, \text{Radius}_{\text{RM5S}}, \text{Width}_{\text{RM5S}})$$

$$\text{Tr_Len}_{\text{RM5S}} = 4.697 \cdot \text{in}$$

$$\text{Tr_Wid}_{\text{RM5S}} := \text{Trace_width}(\text{Width}_{\text{RM5S}}, 5)$$

$$\text{Tr_Wid}_{\text{RM5S}} = 0.007 \cdot \text{in}$$

$$\text{Tr_Resist}_{\text{RM5S}} := \text{Trace_resistance}(\rho, \text{Tr_Wid}_{\text{RM5S}}, 10 \cdot \text{Tr_Len}_{\text{RM5S}}, \text{Trace_thickness})$$

$$\text{Tr_Resist}_{\text{RM5S}} = 2.05 \cdot \text{ohm}$$

$$\text{Tr_Len}_{\text{RM6S}} := \text{Trace_length}(5, \text{Radius}_{\text{RM6S}}, \text{Width}_{\text{RM6S}})$$

$$\text{Tr_Len}_{\text{RM6S}} = 6.315 \cdot \text{in}$$

$$\text{Tr_Wid}_{\text{RM6S}} := \text{Trace_width}(\text{Width}_{\text{RM6S}}, 5)$$

$$\text{Tr_Wid}_{\text{RM6S}} = 0.016 \cdot \text{in}$$

$$\text{Tr_Resist}_{\text{RM6S}} := \text{Trace_resistance}(\rho, \text{Tr_Wid}_{\text{RM6S}}, 10 \cdot \text{Tr_Len}_{\text{RM6S}}, \text{Trace_thickness})$$

$$\text{Tr_Resist}_{\text{RM6S}} = 1.275 \cdot \text{ohm}$$

$$\text{Tr_Len}_{\text{RM8}} := \text{Trace_length}(5, \text{Radius}_{\text{RM8}}, \text{Width}_{\text{RM8}})$$

$$\text{Tr_Len}_{\text{RM8}} = 7.917 \cdot \text{in}$$

$$\text{Tr_Wid}_{\text{RM8}} := \text{Trace_width}(\text{Width}_{\text{RM8}}, 5)$$

$$\text{Tr_Wid}_{\text{RM8}} = 0.02 \cdot \text{in}$$

$$\text{Tr_Resist}_{\text{RM8}} := \text{Trace_resistance}(\rho, \text{Tr_Wid}_{\text{RM8}}, 10 \cdot \text{Tr_Len}_{\text{RM8}}, \text{Trace_thickness})$$

$$\text{Tr_Resist}_{\text{RM8}} = 1.304 \cdot \text{ohm}$$

Appendix B: Initial Request for Quotation

Statement of Work

Scope

Design and develop low-profile magnetic components for use in the circuit shown in the attached drawings (Drawing #R40816, *Schematic, Demonstration Power Converter and CDU*). The components will utilize planar and/or integrated techniques.

Deliverables

1. The Contractor will design, fabricate, test and deliver five (5) Power Converter/CDU assemblies in planar or integrated form. These will be assembled along with the associated circuitry (per Drawing #R40816) on a printed circuit board or other medium.
2. The Contractor will prepare a final report including all information and data necessary for the design, development, processing, and testing of the Power Converter/CDU. All fabrication and processing steps will be clearly documented.
3. The Contractor shall participate in three design review meetings of approximately four (4) hours duration each. The meetings will be held at the Contractor's facility.

Delivery

1. Five (5) sets of Power Converter/CDUs will be delivered 20 weeks after the contract is awarded.
2. A Final Report will be delivered concurrently with the five (5) Power Converter/CDUs .
3. The first design review meetings will be held within thirty (30) days of contract award; subsequent meetings will be scheduled by mutual agreement.

Appendix C: Revised Request for Quotation

The following request for quotation was revised after the contract was placed with e/j Bloom and Associates to reflect mutually agreed upon changes in component specification.

Statement of Work:

Scope

The purpose of this contract is to design and develop three different low-profile magnetic components as defined in the attached two-page specification, entitled *Transformer Specifications*, and dated June 7, 1993. For reference, the components are for use in the circuit shown in the attached drawing package, Drawing #R40816, *Schematic, Demonstration Power Converter and CDU*. The components will utilize planar and/or integrated techniques.

Deliverables

1. The Contractor will design, fabricate, test and deliver five (5) sets of planar magnetic components. Each set consists of one each of transformers T1, T2, T3, and T4.
2. The Contractor will provide drawings that show transformer dimensions, pin definitions, and a printed circuit board mounting footprint.
3. The Contractor will provide a final report including all information and data necessary for the design, development, processing and testing of the transformers. All fabrication and processing steps will be clearly documented.
4. The Contractor shall participate in three design review meetings of approximately four (4) hours duration each. The meetings will be held at the Contractor's facility.

Delivery

1. Drawings of each of the three types of transformers that show printed circuit board mounting footprints will be delivered 20 weeks after contract award.
2. Five (5) sets of transformers will be delivered 20 weeks after contract award. A transformer set consists of one each of transformers T1, T2, T3, and T4.
3. The Final Report will be delivered concurrently with the five (5) sets of transformers.
4. Design Review Meetings: First meeting to be held within thirty (30) days of contract award, subsequent meetings to be scheduled by mutual agreement.

Transformer Specifications

Transformers T1 and T2. (See Figures B1 and B2.)

Transformers T1 and T2 are identical current-viewing transformers (CVTs). Their specifications are:

1. Turn ratio: 1:50. (Note that this differs from the reference circuit drawing.)
2. Output Load: Open circuit. The CVT load of 0.05 ohm will be added to the circuit board.
3. Primary Current: 50 amps peak.
4. Secondary Voltage: 0.05 volts peak. (1 amp peak through the external 0.05 ohm resistor.)
5. Wave Shape: An abrupt transition to 50 amps, followed by an exponential decay with a time constant of 1 millisecond.

6. Duty Cycle: One pulse every 2 seconds.
7. Tolerance: Represent current pulse within 15%.
8. Environmental Requirements: 0 to 70° C operating temperature.
9. Hi-pot to 100 V.

Transformer T3.

This is a single-output, flyback power converter transformer that will be used to charge a 2000 μ F capacitor to 47 V within 1 second. Output power required is 2.2 watts.

1. Turn Ratio: 1:7
2. Primary Wave Shape: Driven by a 200 kilohertz, square wave, constant-frequency, pulse width modulated voltage. Minimum voltage applied to the transformer primary is 8.8 volts, and maximum is 12 volts. Maximum duty cycle is 50%.
3. Primary Inductance: 4 μ H +/- 15%.
4. Primary Leakage Inductance: Less than 0.2% of the open circuit primary inductance.
5. Primary Winding dc Resistance: Less than 20 m Ω .
6. Primary Current: 1.0 A peak, 0.4 A RMS
7. Secondary Winding dc Resistance: Less than 200 m Ω .
8. Environmental Requirements: 0 to 70° C operating temperature.
9. Hi-pot to 200 V.

Transformer T4.

This is a triple-output, flyback power converter transformer that will be used to supply +5 V, 0.4 A logic power and +/-15 V, 0.2 A analog circuit power, totaling 8 W output power. (Note that this differs from the reference example circuit.).

1. Turn ratio: 5:4:11:11
2. Primary wave shape: Driven by a 200 kHz, square wave, constant-frequency, pulse width modulated voltage. Minimum voltage applied to the transformer primary is 8.8 V, and maximum is 12 V. Maximum duty cycle is 50%.
3. Primary inductance: 2.5 μ H +/- 15%.
4. Primary leakage inductance: Less than 0.2% of the open circuit primary inductance.
5. Primary winding dc resistance: Less than 20 m Ω .
6. Primary current: 3 A peak, 1.3 A RMS
7. Secondary #1 winding dc resistance: Less than 20 m Ω .
8. Secondary #2 and #3 winding dc resistance: Less than 80 m Ω .
9. Environmental Requirements: 0 to 70° C operating temperature.
10. Hi-pot to 200 V.

Figure C1. Current-viewing Transformer T1, Top and Side Views. The transformer had one primary turn and 50 secondary turns. The stacking of the printed circuit boards can be seen in both views.

Figure C2. Transformer T1 Components Displayed in the Order Stacked. The top and bottom windings are the single-turn primary, formed from stamped copper and connected in parallel. The secondary windings use five, 10-turn circuit boards, 5 turns per side.

Appendix D: Energy Lost in an Inductor

ENRGSTOR.RLN Charge an inductor thru a resistor, from a constant voltage source, show the ratio of energy stored in the inductor to the total energy put into the series R-L network. 9/19/94

$$r := 1$$

$$L := 1 \cdot 10^{-3}$$

$$\frac{L}{r} = 0.001 \quad \text{time constant of network}$$

$$i := 0..40$$

$$t_i := \left(\frac{L}{r} \right)^{\frac{i+10}{20}} \quad I_i := \frac{V}{r} \cdot \left(1 - \exp \left(-\frac{r}{L} \cdot t_i \right) \right)$$

$$EL_i := \frac{1}{2} \cdot L \cdot (I_i)^2 \quad \text{energy stored in inductor}$$

$$ET_i := EL_i + \int_0^{t_i} (I_i)^2 \cdot r \, dt \quad \text{total energy, stored in L and dissipated in resistor}$$

ratio of energy stored in an ideal inductor to the total energy put into the circuit vs time constant. At $t_i = 0+$, most of the energy is stored in the inductor, after several time constants, most of the energy is dissipated in the resistor. Thus for efficient flyback converters, it is desirable to have the "on" time less than 0.1 time constant.

Appendix E: Transformer Calculations

Planar magnetic calculation for outputs of +5, +/-15V

$$\eta := 0.70 \frac{\text{watt}}{\text{watt}} \quad \text{Power converter efficiency}$$

$$\mu_o := 4 \cdot \pi \cdot 10^{-7} \cdot \text{kg} \cdot \text{m} \cdot \text{coul}^{-2} \quad \text{Permeability of free space}$$

$$B_{\max} := 0.15 \text{ tesla} \quad \text{Maximum magnetic flux density for a 3F3 ferrite, considering temperature effects, losses, and operation in the first quadrant.}$$

$$f_s := 200 \cdot 10^3 \cdot \text{Hz} \quad \text{Operating frequency} \quad \delta_{\max} := 0.45 \quad \text{Maximum duty cycle}$$

Note: dmax was reduced from 0.45 to match the primary turns chosen.

$$V_{\text{MAXin}} := 12 \cdot \text{volt} \quad V_{\text{MINin}} := 8.0 \cdot \text{volt} \quad \text{Max and min. voltages from 8ea NiCd batteries, 1 V per cell minimum - 0.5V diode drop}$$

$$V_{\text{cc}} := 5 \cdot \text{volt} \quad I_{\text{cc}} := 0.4 \cdot \text{amp}$$

$$V_{\text{dd}} := 15 \cdot \text{volt} \quad I_{\text{dd}} := 0.2 \cdot \text{amp} \quad \text{Output power}$$

$$V_{\text{ss}} := -15 \cdot \text{volt} \quad I_{\text{ss}} := -0.2 \cdot \text{amp}$$

$$P_{\text{in}} := \frac{V_{\text{cc}} \cdot I_{\text{cc}} + V_{\text{dd}} \cdot I_{\text{dd}} + V_{\text{ss}} \cdot I_{\text{ss}}}{\eta} \quad P_{\text{in}} = 11.429 \cdot \text{watt} \quad \text{Input power required}$$

$$P_{\max}(l_g, A_c, B_{\max} f_s) := l_g \cdot A_c \cdot B_{\max}^2 \cdot \frac{f_s}{2 \cdot \mu_o}$$

RM5PA100-3F3	$P_{\max}(0.0082.54 \cdot 10^{-2} \cdot \text{m}, 0.21 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 7.64 \cdot \text{watt}$
RM6SPA63-3F3	$P_{\max}(0.0252.54 \cdot 10^{-2} \cdot \text{m}, 0.37 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 42.068 \cdot \text{watt}$
RM6SPA100-3F3	$P_{\max}(0.0162.54 \cdot 10^{-2} \cdot \text{m}, 0.37 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 26.923 \cdot \text{watt}$
RM6SPA160-3F3	$P_{\max}(0.0082.54 \cdot 10^{-2} \cdot \text{m}, 0.37 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 13.462 \cdot \text{watt}$
RM6SPA250-3F3	$P_{\max}(0.0052.54 \cdot 10^{-2} \cdot \text{m}, 0.37 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 8.414 \cdot \text{watt}$
RM8SPA160-3F3	$P_{\max}(0.0222.54 \cdot 10^{-2} \cdot \text{m}, 0.63 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 63.033 \cdot \text{watt}$
RM8SPA250-3F3	$P_{\max}(0.0122.54 \cdot 10^{-2} \cdot \text{m}, 0.63 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 34.382 \cdot \text{watt}$
RM8SPA315-3F3	$P_{\max}(0.0102.54 \cdot 10^{-2} \cdot \text{m}, 0.63 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 28.651 \cdot \text{watt}$
RM8SPA400-3F3	$P_{\max}(0.0072.54 \cdot 10^{-2} \cdot \text{m}, 0.63 \cdot 10^{-4} \cdot \text{m}^2, B_{\max} f_s) = 20.056 \cdot \text{watt}$

Choose RM6SPA100-3F3 core. The parameters are:

$$l_{g \text{ choice}} := 0.008 \text{ in} \quad A_{c \text{ choice}} := 0.37 \cdot 10^{-4} \cdot \text{m}^2 \quad P_{\text{max choice}} := P_{\text{max}}(l_{g \text{ choice}}, A_{c \text{ choice}}, B_{\text{max}}, f_s)$$

$$A_{l \text{ choice}} := 160 \cdot 10^{-3} \cdot \text{henry}$$

Now, calculate the primary turns. The maximum power for each core configuration was calculated above. The turns will be calculated from the required inductance.

$$L_m(V_{\text{MINin}}, \delta_{\text{max}}, P_{\text{in}}, f_s) := \frac{V_{\text{MINin}}^2 \cdot \delta_{\text{max}}^2}{2 \cdot f_s \cdot P_{\text{in}}}$$

$$L_m(V_{\text{MINin}}, \delta_{\text{max}}, P_{\text{max choice}}, f_s) = 2.407 \cdot 10^{-6} \cdot \text{henry}$$

Calculate the number of turns required to get this inductance. In essence, search for the appropriate core because a single primary turn is desired.

$$\text{Turns}_{\text{table}}(L, L_{\text{core}}) = 1000 \sqrt{\frac{L}{L_{\text{core}}}}$$

$$\text{Turns}_{\text{table}}(L_m(V_{\text{MINin}}, \delta_{\text{max}}, P_{\text{max choice}}, f_s), A_{l \text{ choice}}) = 3.878$$

$$\text{Turns}_{\text{table}}(L_m(V_{\text{MINin}}, \delta_{\text{max}}, P_{\text{in}}, f_s), A_{l \text{ choice}}) = 4.209$$

$$\text{Turns}_{\text{eqn}}(L, A_c, l_g) = \sqrt{\frac{l_g \cdot L}{\mu_0 \cdot A_c}}$$

$$\text{Turns}_{\text{eqn}}(L_m(V_{\text{MINin}}, \delta_{\text{max}}, P_{\text{max choice}}, f_s), A_{c \text{ choice}}, l_{g \text{ choice}}) = 3.243$$

Or, by equating the inductance at the maximum power for a given core to the inductance equation,

$$\text{Turns}_{\text{pri}}(V_{\text{in}}, \delta_{\text{max}}, A_c, B_{\text{max}}, f_s) := \frac{V_{\text{in}} \cdot \delta_{\text{max}}}{A_c \cdot B_{\text{max}} \cdot f_s}$$

$$N_{\text{pri}} = \text{Turns}_{\text{pri}}(V_{\text{MINin}}, \delta_{\text{max}}, A_{c \text{ choice}}, B_{\text{max}}, f_s) \quad N_{\text{pri}} = 3.243$$

The turns calculated from the manufacturer's data is usually 10 to 20 percent high, and from just the core data and gap length, about the same amount low. Because the intended implementation is planar, we will minimize the number of turns used, and choose a primary turns of:

$$N_{\text{pri}} = 3$$

The impact of this choice can be calculated from first, the resulting inductance, and then the input voltage and duty cycle to find the resulting peak current and peak magnetic flux density.

$$L_m(N, A_c, l_g) := \frac{\mu_o \cdot A_c \cdot N^2}{l_g} \quad \text{The standard equation for a gapped core.}$$

$$L_{pri} := L_m(N_{pri}, A_{c \text{ choice}}, l_{g \text{ choice}}) \quad L_{pri} = 2.059 \cdot 10^{-6} \cdot \text{henry}$$

Next, the peak current can be calculated, assuming the minimum input voltage and maximum duty cycle.

$$I_{peak}(L, V, \delta, f_s) := \frac{V \cdot \delta}{L \cdot f_s} \quad \text{Current increases linearly with time (until core saturation)}$$

$$I_{peak_pri} := I_{peak}(L_{pri}, V_{MINin}, \delta_{max}, f_s) \quad I_{peak_pri} = 8.741 \cdot \text{amp}$$

Using the peak current and inductor properties, the peak magnetic flux is calculated:

$$B_{peak}(L, I_{pk}, N, A_c) := \frac{L \cdot I_{pk}}{N \cdot A_c}$$

$$B_{peak_pri} := B_{peak}(L_{pri}, I_{peak_pri}, N_{pri}, A_{c \text{ choice}}) \quad B_{peak_pri} = 0.162 \cdot \text{tesla}$$

Because the magnetizing current appears as a triangular wave form, the average current is found from a simple geometric relationship of base * height / 2. The maximum input power can then be calculated:

$$P(V, I_{pk}, \delta) := \frac{\delta}{2} \cdot V \cdot I_{pk}$$

$$P_{in_actual} := P(V_{MINin}, I_{peak_pri}, \delta_{max}) \quad P_{in_actual} = 15.733 \cdot \text{watt}$$

This power is larger than needed for the design, and the peak magnetic flux density would contribute to higher than desirable losses. Useful designs have current limiting features. Setting the peak current based on the required input power will limit the peak B and protect the design.

$$I_{peak_pri} := 6.3 \cdot \text{amp}$$

$$B_{peak_pri} := B_{peak}(L_{pri}, I_{peak_pri}, N_{pri}, A_{c \text{ choice}}) \quad B_{peak_pri} = 0.117 \cdot \text{tesla}$$

$$P_{in_actual} := P(V_{MINin}, I_{peak_pri}, \delta_{max}) \quad P_{in_actual} = 11.34 \cdot \text{watt}$$

Calculate minimum turns ratio based on component voltage ratings. Use 1.3 times reflected voltage for ringing:

$$V_{FWDdiode} := 0.6 \cdot \text{volt} \quad V_{DSfet} := 40 \cdot \text{volt}$$

$$N_{MINsec}(V_{output}, V_{FWDdiode}, V_{DSfet}, V_{MAXin}) := \frac{(V_{output} + V_{FWDdiode}) \cdot 1.3}{V_{DSfet} - V_{MAXin}}$$

$$N_{sec_min} := N_{MINsec}(V_{cc}, V_{FWDdiode}, V_{DSfet}, V_{MAXin}) \quad N_{sec_min} = 0.26 \quad \text{Times } N \text{ primary}$$

Calculate maximum turns ratio based on Continuous - Discontinuous operation boundary

$$N_{MAXsec}(V_{output}, V_{FWDdiode}, V_{MINin}, \delta_{max}) := \frac{V_{output} + V_{FWDdiode}}{V_{MINin}} \cdot \frac{1 - \delta_{max}}{\delta_{max}}$$

$$N_{sec_max} := N_{MAXsec}(V_{cc}, V_{FWDdiode}, V_{MINin}, \delta_{max}) \quad N_{sec_max} = 0.856 \quad \text{Times } N \text{ primary}$$

$$N_{sec_min} \cdot N_{pri} = 0.78 \quad < N_{sec5} < N_{sec_max} \cdot N_{pri} = 2.567$$

Based on this answer, operation with a 3:1 turns ratio is acceptable and is selected. Choose the following number of turns:

$$N_{pri} = 3 \quad N_{sec5} := 1 \quad N_{sec15} := 3$$

Average input current is (at lowest input voltage, full load):

$$I_{in} := \frac{P_{in}}{V_{MINin}} \quad I_{in} = 1.429 \cdot \text{amp} \quad I_{inPeak} := I_{in} \cdot \frac{2}{\delta_{max}} \quad I_{inPeak} = 6.349 \cdot \text{amp}$$

$$\text{Cond_area}(I) := 1.500 \cdot 10^{-6} \cdot \text{in}^2 \cdot \text{amp}^{-1} \quad \text{Using } 500 \text{ circ. mils per amp}$$

$$\begin{aligned} \text{Spaces_2} &:= 0.010 \text{ in} & \text{Spaces_3} &:= 0.012 \text{ in} & \text{Spaces_4} &:= 0.018 \text{ in} & \text{Tr_to_Hole} &:= 0.020 \text{ in} \\ \text{Width_RM5S} &:= (0.105 \text{ in} - \text{Tr_to_Hole} \cdot 2) & \text{Radius_RM5S} &:= (0.097 \text{ in} + \text{Tr_to_Hole}) \\ \text{Width_RM6S} &:= (0.148 \text{ in} - \text{Tr_to_Hole} \cdot 2) & \text{Radius_RM6S} &:= (0.127 \text{ in} + \text{Tr_to_Hole}) \\ \text{Width_RM8} &:= (0.166 \text{ in} - \text{Tr_to_Hole} \cdot 2) & \text{Radius_RM8} &:= (0.169 \text{ in} + \text{Tr_to_Hole}) \end{aligned}$$

Based on these numbers, calculate the width and thickness of the traces for various turns/layer on an RM6S Core:

$$\text{Trace_width}(\text{Trace_layer}, \text{Sp}) := \frac{(\text{Width_RM6S}) - (\text{Trace_layer} - 1) \cdot \text{Sp}}{\text{Trace_layer}} \quad \text{Trace_height}(\text{Area}, \text{Width}) := \frac{\text{Area}}{\text{Width}}$$

$$\text{Oz}_{Cu}(\text{Thickness}) := \frac{\text{Thickness}}{0.00128 \text{ in} \cdot \text{oz}^{-1}} \quad \text{Trace_width}(5, \text{Spaces_2}) = 0.01360 \cdot \text{in} \quad \text{Trace_width}(3, \text{Spaces_4}) = 0.02400 \cdot \text{in}$$

$$X := \text{Trace_height}\left(\text{Cond_area}\left(I_{in}\right), \text{Trace_width}(1, \text{Spaces_2})\right) \quad X = 0.00661 \cdot \text{in} \quad \text{Oz}_{Cu}(X) = 5.167 \cdot \text{oz}$$

$$X := \text{Trace_height}\left(\text{Cond_area}\left(\frac{I_{in}}{2}\right), \text{Trace_width}(1, \text{Spaces_2})\right) \quad X = 0.00331 \cdot \text{in} \quad \text{Oz}_{Cu}(X) = 2.583 \cdot \text{oz}$$

$$X := \text{Trace_height}\left(\text{Cond_area}\left(\frac{I_{in}}{3}\right), \text{Trace_width}(2, \text{Spaces_2})\right) \quad X = 0.00486 \cdot \text{in} \quad \text{Oz}_{Cu}(X) = 3.796 \cdot \text{oz}$$

$$X := \text{Trace_height}\left(\text{Cond_area}(I_{cc} + I_{dd}), \text{Trace_width}(1, \text{Spaces_2})\right) \quad X = 0.00278 \cdot \text{in} \quad \text{Oz}_{Cu}(X) = 2.17 \cdot \text{oz}$$

$$X := \text{Trace_height}\left(\text{Cond_area}(I_{dd}), \text{Trace_width}(2, \text{Spaces_2})\right) \quad X = 0.00204 \cdot \text{in} \quad \text{Oz}_{Cu}(X) = 1.594 \cdot \text{oz}$$

$$X := \text{Trace_height}\left(\text{Cond_area}(-I_{ss}), \text{Trace_width}(3, \text{Spaces_2})\right) \quad X = 0.00341 \cdot \text{in} \quad \text{Oz}_{Cu}(X) = 2.663 \cdot \text{oz}$$

From these calculations, a 5 oz copper layer would be needed for the primary, or 3 oz if the windings are parallel. Unfortunately, we wish to limit the number of layers, and 5 oz copper is not practical. Instead, we will choose 2 oz stock copper and suffer some reduced performance. Placing two of the three primary turns on the outer layers will result in an actual copper thickness of 3 oz because of the plating needed to connect plate-through holes. Paralleling the third turn, which is in the middle of the board, gives it an equivalent thickness of 4 oz copper. For the outputs, 2 oz copper should be adequate. The printed circuit board construction is as follows:

Stack of board layers for a 3:1:3:3 turns ratio for Pri:5V:+15V:-15V =

Layer A - 1 turn, 3oz Cu (part 1 of 3-turn primary)

Layer B - 1 turn, 2oz Cu (5V secondary)

Layer C - 1 turn, 2oz Cu (part 2 of 3-turn primary, parallel with Layer E)

Layer D - 2 turns, 2oz Cu (+15V secondary part 2 of 3 turns, first part shared with 5V secondary)

Layer E - 1 turn, 2oz Cu (part 2 of 3-turn primary, parallel with Layer C)

Layer F - 3 turns, 2oz Cu (-15V secondary)

Layer G - 1 turn, 2oz Cu (part 3 of 3-turn primary, parallel with Layer H)

Layer H - 1 turn, 3oz Cu (part 3 of 3-turn primary, parallel with Layer G)

Calculate the resistance and power loss in each winding based on the above choices for transformer configuration. Based on the previous numbers, calculate the width, thickness, and resistance for each of the windings.

$$\text{Trace thickness (Plating wt)} := \text{Plating wt} \cdot 0.00128 \text{ in} \cdot \text{oz}^{-1}$$

$$\text{Trace resistance } (\rho, \text{Width}, \text{Length}, \text{Thickness}) := \rho \frac{\text{Length}}{\text{Width} \cdot \text{Thickness}}$$

$$\text{Trace length (Layers, Turns layer, } R_{\text{core}}, W_{\text{core}}) := \text{Layers} \cdot \text{Turns layer} \cdot \left(R_{\text{core}} + \frac{W_{\text{core}}}{2} \right) \cdot 2 \cdot \pi$$

$$\rho_{\text{Cu}} := 2.10 \cdot 10^{-6} \cdot \Omega \cdot \text{cm} \quad \text{Pure copper is } 1.678 \text{E-6 Ohm-cm, but plating is higher.}$$

$$P_{\text{lost}}(I, R) := I^2 \cdot R$$

Now, based upon the number of turns defined as the range Turns below, calculate trace dimensions:
 Primary of transformer, 3 turns using 1 turn / layer for layer 1 and 1 turn/2 layers for layers 2 and 3.
 The equivalent layers is 2 (1 + 0.5 + 0.5).

Turns_{layer} := 1 Layers := 2 Note: 3 physical layers, but the equivalent resistance of 2

$$\begin{aligned} W &:= \text{Trace width}(\text{Turns}_{\text{layer}}, \text{Spaces}_2) & W &= 0.10800 \text{ in} \\ L &:= \text{Trace length}(\text{Layers}, \text{Turns}_{\text{layer}}, \text{Radius RM6S}, \text{Width RM6S}) & L &= 2.526 \text{ in} \\ T &:= \text{Trace thickness} (2\text{-oz}) & T &= 0.00256 \text{ in} \\ R &:= \text{Trace resistance} (\rho_{\text{Cu}}, W, L, T) & R &= 0.00755 \Omega \\ & & P_{\text{lost}}(I_{\text{in}}, R) &= 0.015 \text{ watt} \\ & & P_{\text{total}} &:= P_{\text{lost}}(I_{\text{in}}, R) \end{aligned}$$

5V Secondary of transformer

$$\begin{aligned} \text{Turns}_{\text{layer}} &:= 1 & \text{Layers} &:= 1 \\ W &:= \text{Trace width}(\text{Turns}_{\text{layer}}, \text{Spaces}_2) & W &= 0.10800 \text{ in} \\ L &:= \text{Trace length}(\text{Layers}, \text{Turns}_{\text{layer}}, \text{Radius RM6S}, \text{Width RM6S}) & L &= 1.263 \text{ in} \\ T &:= \text{Trace thickness} (2\text{-oz}) & T &= 0.00256 \text{ in} \\ R &:= \text{Trace resistance} (\rho_{\text{Cu}}, W, L, T) & R &= 0.00378 \Omega \\ & & P_{\text{lost}}(I_{\text{cc}} + I_{\text{dd}}, R) &= 0.00136 \text{ watt} \\ & & P_{\text{total}} &:= P_{\text{total}} + P_{\text{lost}}(I_{\text{cc}} + I_{\text{dd}}, R) \end{aligned}$$

15V Secondary of transformer

$$\begin{aligned} \text{Turns}_{\text{layer}} &:= 2 & \text{Layers} &:= 1 \\ W &:= \text{Trace width}(\text{Turns}_{\text{layer}}, \text{Spaces}_2) & W &= 0.04900 \text{ in} \\ L &:= \text{Trace length}(\text{Layers}, \text{Turns}_{\text{layer}}, \text{Radius RM6S}, \text{Width RM6S}) & L &= 2.526 \text{ in} \\ T &:= \text{Trace thickness} (2\text{-oz}) & T &= 0.00256 \text{ in} \\ R &:= \text{Trace resistance} (\rho_{\text{Cu}}, W, L, T) & R &= 0.01665 \Omega \\ & & P_{\text{lost}}(I_{\text{dd}}, R) &= 6.6591 \cdot 10^{-4} \text{ watt} \\ & & P_{\text{total}} &:= P_{\text{total}} + P_{\text{lost}}(I_{\text{dd}}, R) \end{aligned}$$

-15V Secondary of transformer

$$\begin{aligned} \text{Turns}_{\text{layer}} &:= 3 & \text{Layers} &:= 1 \\ W &:= \text{Trace width}(\text{Turns}_{\text{layer}}, \text{Spaces}_2) & W &= 0.02933 \text{ in} \\ L &:= \text{Trace length}(\text{Layers}, \text{Turns}_{\text{layer}}, \text{Radius RM6S}, \text{Width RM6S}) & L &= 3.789 \text{ in} \\ T &:= \text{Trace thickness} (2\text{-oz}) & T &= 0.00256 \text{ in} \\ R &:= \text{Trace resistance} (\rho_{\text{Cu}}, W, L, T) & R &= 0.04171 \Omega \\ & & P_{\text{lost}}(-I_{\text{ss}}, R) &= 0.00167 \text{ watt} \\ & & P_{\text{total}} &:= P_{\text{total}} + P_{\text{lost}}(-I_{\text{ss}}, R) \\ & & P_{\text{total}} &= 0.019 \text{ watt} \end{aligned}$$

Appendix F: Planar Magnetic Demonstration Board Schematic

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