Solder Technology in the Manufacturing of Electronic Products

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Abstract

The electronics industry has relied heavily upon the use of soldering for both package construction and circuit assembly. The solder attachment of devices onto printed circuit boards and ceramic microcircuits has supported the high volume manufacturing processes responsible for low cost, high quality consumer products and military hardware. Defects incurred during the manufacturing process are minimized by the proper selection of solder alloys, substrate materials and process parameters. Prototyping efforts are then used to evaluate the manufacturability of the chosen material systems. Once manufacturing feasibility has been established, service reliability of the final product is evaluated through accelerated testing procedures.

I. Introduction

Soldering technology continues to play a critical role in all levels of electronics manufacturing. At the chip level, controlled collapse chip components, or "C4" technology[1], tape automated bonding (TAB)[2], and the advent of multichip modules (MCM) have revolutionized the miniaturization and functionality of computer systems. At the sub-system level, soldering has had its most recognized impact, that is, the assembly of printed circuit boards and hybrid microcircuits. Lastly, solder joining is used in the assembly of the final product. Cables between several circuit boards or connections to the back plane depend upon soldering at the terminals to assure high reliability signal transmission. Because connectors must withstand human interaction, their strength requirements are unique. For example, the solder joints must accommodate the removal, insertion, and movement of cable assemblies without failure. Moreover, terminals are exposed to moisture, dust, and corrosive environments which can significantly degrade their integrity.

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Soldering may appear to be a technological subset of electronics manufacturing. However, soldering has been in existence for nearly six thousand years, first used by artisans to make jewelry, and then later by the Romans for the "plumbing" of their aqueducts. Although used for plumbing purposes in the twentieth century, soldering technology has evolved through applications in the electronics industry. Electronic packaging has been engineered to withstand the thermal and physical properties of both molten and solid solder alloys. The development of both manufacturing technologies and newer, non-traditional solder materials has been guided by further package miniaturization, larger volume (cost-effective) assembly requirements, and an enormous increase in device functionality which demands a minimum number of defects in the solder joints for product reliability.

The objective of this paper is to discuss those aspects of soldering technology which pertain to the manufacturing of electronics from the chip level to the sub-system or circuit board level. System or product assembly, which includes the soldering of connectors and cables will not be reviewed in this text. Also, a detailed discussion on solder joint reliability will not be conducted. The reader is referred to several excellent textbooks for general information[3,4,5,6,7] as well as to the scientific literature for up-to-date research on these topics.

I.A. Manufacturability - Defects.

In a functional sense, "manufacturability" defines the fabrication of a particular item to the specifications called out by the design engineer. Non-conformance to those specifications necessarily implies the presence of "defects" in the assembly. The identification of defects in the device or system must be made so that corrective measures can be introduced into the manufacturing process(es). Cosmetic defects may affect the marketing of a particular product. However, functional defects directly impact product reliability in service. Generally, electronic products are not marketed to customers by the appearance of their electronic "guts"; hence, cosmetic defects are not critical to system quality.

A "universal" defect common to all soldering processes is the inability of the molten solder to wet the base material surface. There are numerous sources for poor wetting: (1) organic contaminants on the surface,
excessive oxidation, (3) poorly active flux, (4) solder chemistry, etc. Nevertheless, it is important to identify the two primary wetting defects: non-wetting and de-wetting. Both defects are illustrated in Fig. 1. Non-wetting is the failure of the molten solder to spread over the metal surface and form a metallurgical bond with the surface. De-wetting describes the instance in which the solder initially wets the surface, and subsequently withdraws from the surface into isolated mounds of solder. Both non-wetting and de-wetting indicate a deterioration in the surface condition of the materials to be joined.

The application of pressure between the two substrates can be used to assist the spreading of solder within the joint; however, the solder has not wet the surfaces unless the metallurgical bond has been formed. The solder may appear to stick to the surface in the absence of such a bond. The adhesion results from the freezing of the solder to surface (mechanical linkage) and is observed to be very weak. A metallurgical bonding is indicated by the formation of a reaction layer between the solder and the substrate. That reaction layer is only visible by sectioning the part and metallographic preparation of the specimen for microscopic examination (clearly a form of destructive testing).

Defects may also be generated by the condition of the particular devices to be soldered into place. For example, leaded packages can cause poor solder joints when the leads are bent or deformed during handling. Non-coplanar leads is of increasingly greater concern as the leads become smaller to accommodate reduced package sizes and greater device functionality (i.e., the requirement for more input/output or "I/O's").

Assuming adequately wettable surfaces, the manufacturing process may also cause defects in the solder joints. Improper heating rates, too high or too low temperatures, can prevent spreading of the solder (an apparent wettability problem) or create other defects such as voids in the solder or solder balls around the joint area.

Defects are a function of the materials used in the joint; in most cases, that means the material's surface and the manufacturing process. However, these two categories are often synergistic in their effects on the manufacturability of a particular component.

Assisting the design and manufacturing engineers to develop a product with minimum defects are a large number of specifications and guidelines provided by the military organizations (e.g., "MIL-STANDARDS" and Federal
Specifications) and by professional organizations (Electronic Industries Association, Institute for Interconnecting ad Packaging Electronic Circuits or IPC, Joint Electron Device Engineering Council or JEDEC, etc.). Although too numerous to list here, documents provided by these organizations cover nearly every aspect of electronics manufacturing: material specifications, design rules for circuit board layout, package size and I/O configurations, cleanliness testing, inspection guidelines, etc.

The following text will describe several of the factors that affect manufacturability. The intent of these sections is not to provide an exhaustive treatise of these categories. Rather, the goal is to illustrate those properties or aspects which will impact the manufacturing process.

II. Materials

The materials used in the solder assembly of electronic devices and systems can be placed into one of the following three categories: (1) the solder alloys; (2) the device package leads or terminations; and (3) the circuit board. Obtaining an "adequate" solder joint is dependent upon the solderability of the circuit board pad and the device lead or termination. Circuit board pad or device lead solderability are, in turn, dependent upon: (1) the solder chemistry, (2) the strength of the flux, and (3) the degree of contamination and/or oxidation of the pad or lead. The geometry of the joint (e.g., lead shape) is also a factor, but its acceptance for use by the designer implies that it is, in fact, solderable. All else being equal, it is most often the surface condition of the circuit board pad or device lead which governs the solderability of a particular joint. The surface condition is a function of the storage environment as well as intrinsic properties of base metal.

II.A. Solders

The thermal, physical, mechanical, electromagnetic, and corrosion properties of solders are critical to the performance of high reliability electronic systems. These properties may be categorized into those which the manufacturing engineer finds crucial to system assembly and yields, and those which the design engineer must consider for adequate reliability of the finished product in service. In the latter case, properties such as monotonic strength, creep resistance, and fatigue strength as well as corrosion resistance
are of particular interest. On the other hand, properties such melting
temperature, surface tension, viscosity, and liquid metal oxidation (i.e., dross
formation) are of concern to the process development engineer and will be
targeted in the discussion.

PROPERTIES.

Shown in Table 1 are the melting properties of several solder alloys
commonly used in the assembly of device packages and circuit boards. The
solder's liquidus temperature, that is the minimum temperature at which the
solder is entirely in a liquid state, is important in the development of
manufacturing processes. However, a "working" temperature is selected for
the solder which is typically 40-50°C above the liquidus temperature to ensure
adequate heating of the parts to be joined (In some processes, the solder may
be the only heat source with which to raise the temperature of the parts).
Properly heated parts will prevent the premature solidification of the solder
prior to final formation of the joint.

The higher working temperature of the solder also lowers its viscosity.
A lower viscosity allows the solder to spread more easily into holes and gaps
that comprise the joint. Spreading is also facilitated by lowering the surface
tension of the solder. However, the surface tension of liquid solder alloys is
not very sensitive to the range of temperatures encountered in typical
assembly processes (Table 2)[8]. Moreover, an important role of the flux is to
lower the surface tension of the solder[9].

The temperature of the solder (and substrate) must be sufficiently high
to activate the cleaning action of the flux. Using the 40-50°C over-
temperature rule, flux activation is not of concern for solders with working
temperatures in excess of approximately 200°C. However, solders such as 58Bi-
42Sn (wt.% or 50In-50Sn (Table 1) may exhibit poor wettability at their
traditional working temperatures (180°C and 170°C, respectively) due to
inadequate activation of a rosin-based flux's corrosion action. The data in
Table 3 clearly show this effect for the wettability of 50In-50Sn using a rosin-
based, mildly activated (RMA) flux[10]. Wettability is quantified by the contact
angle formed at the triple point of the solder, substrate, and flux. Increasing
the working temperature of these particular alloys is required for adequate
solderability, thereby eliminating any benefit derived from their use on heat
sensitive devices or substrates.
Excessively high process temperatures can cause thermal degradation to the flux. This problem is of particular concern in processes which use solder baths (e.g., wave soldering). Deterioration of the flux (also termed charring) may take place prior to spreading by the solder; the result is poor product solderability. High soldering temperatures also cause flux residues to form which are difficult to remove from the assembly surfaces. High temperatures can damage electronic devices as well as the substrate material, particularly, organic-based printed wiring boards. In general, processing temperatures which exceed 250°C and time periods greater than 5-10 sec increase the likelihood of thermal breakdown of rosin-based and many water soluble fluxes, and the subsequent creation of tenacious flux residues[11].

As exemplified by the data in Table 1, solder alloys are available with a wide range of melting points. This resource allows for the use of "step soldering" processes in the assembly of electronic devices and systems. In the step soldering process, multiple soldering stages or steps are used to assemble the product; the solder used in each subsequent step has a lower melting point than that used in the previous stage so that the previously formed joint will not be re-melted. The design of a step soldering process must take account of the working temperature of the next solder, not solely its liquidus temperature. A minimum temperature difference of 40°C should be maintained between the working temperature of the solder and the solidus temperature of the alloy used in the previous step to prevent liquification of the prior joint or its distortion due to excessive soften by its solder. Of course, it should be noted that as the number of steps is increased, the lower is the melting temperature of the solder used in the last stage. It is the melting point of the lowest temperature alloy which will set the maximum service temperature of the final assembly. In addition, the lower melting point alloys typically contain expensive metals such as indium, silver, and gallium, or hazardous metals such as cadmium.

Manufacturing processes which use large solder reservoirs are sensitive to liquid metal oxidation, resulting in the formation of dross on the bath surface. Excessive dross formation not only increases the risk of particulate contamination of the solder joints, but also requires expensive replenishment of the bath and a need for the proper disposal/recycling of large amounts of hazardous waste, particularly lead-bearing solders. Besides solder bath temperature, the creation of solder dross is also a strong function
of the solder composition. For example, tin-bismuth alloys produce large amounts of dross when compared to tin-lead solders, illustrating that dross formation is strongly dependent upon the oxidation properties of the individual constituents in the solder alloy. Solders characterized by significant dross formation should have their pot chemistries monitored frequently to verify that dross removal is not preferentially depleting any one component of the solder alloy.

PASTES

Solders used in paste form, such as in the assembly of surface mount technology circuit boards, have additional concerns for their successful use. A primary factor is the size of the particles. Smaller particle sizes are desirable to achieve precise dimensions, thickness, and registration of the paste deposit on the circuit board by the printing process, particularly for fine-pitch features. However, smaller particles have a larger surface-to-volume ratio, thereby increasing the amount of oxidized material. The excessive oxidation of solder particles, or their corrosion by prolonged exposure to fluxes in the paste, will significantly increase manufacturing defects because the thick oxide skin on the powder particles prevents their coagulation into a single solder mass upon melting. As a consequence, the particles may flow away from the primary solder mass, causing solder balls to form about the solder joint (Fig. 2). Solder pastes containing zinc or indium are particularly susceptible to corrosion by the flux contained in the vehicle during storage. In these circumstances, excessive solder ball formation can be curtailed by keeping the solder powder separate from the vehicle (which contains the flux) until time of use.

Solder paste performance is extremely sensitive to manufacturing process conditions. A solder paste passes through three conditions from the moment that it is introduced to the joint area to the final solidification of the solder joint. The first stage is the "drying" of the paste deposit to remove highly volatile vehicle constituents. When present in the paste during reflow, the rapid vaporization of these constituents causes solder particles to be spattered from the joint area. The resulting solder fillet may contain large voids or "blow-holes" as a result of the rapid gas release. These volatiles are typically released by heating at temperatures below 100°C; the lower the temperature, the longer the required time period to release the materials (and
greater are the chances of over-oxidizing the solder powder). The second stage is activation of the flux which typically occurs in the temperature range of 150°C to 190°C. The fluidity of the flux component increases, permitting it to coat the solderable surfaces. Tarnish layers are removed from the pad and device lead (or termination) surfaces as well as from the solder particles. This latter function allows the solder particles to combine upon melting to form the fillet. The third and final stage is melting of the solder component (at working temperatures of 215°C to 245°C for eutectic and near-eutectic tin-lead solders). The solder particles flow together, wetting the pad and device lead surfaces to form the solder fillet.

Shown in Fig. 3 is a typical temperature profile of a surface mount circuit board processed by infrared furnace reflow, using tin-lead solder paste. Drying of the paste occurs during the initial heating segment. The heating time must be minimized to prevent excessive oxidation of the solder powder; recall that the flux will not as yet have activated so as to limit solder oxidation. The plateau at T1, which is in the range of 170°C to 190°C, serves to activate the fluxes chemical processes to remove tarnish from pads, leads, and the solder particles; the time period also allows the circuit board and devices to heat-up so as to reduce thermal shock when exposed to the solder working temperature. The flux coating provides protection against re-oxidation of the pads, leads, and solder particles. The time period, t1-t2, can be upwards of several minutes, depending on the configuration of the product being assembled. Melting of the solder takes place during the subsequent heating or reflow "spike" to the working temperature (T2). Time at the working temperature (t2-t3) is minimized to prevent damage to devices or substrates as well as to limit poor solderability arising from re-oxidation of surfaces. Excessive temperature exposure is also indicated by excessive, difficult-to-remove flux residues. Solder wetting processes typically require 2 to 5 sec for completion; however, the process profile may show a spike lasting 20 to 40 sec (i.e., the time above the solder liquidus temperature) because of the thermal inertia of the assembly.

HIGH TEMPERATURE SOLDERs-PACKAGING APPLICATIONs

The precious metal solders listed in Table 1: 80Au-20Sn (Teutectic = 280°C), 88Au-12Ge (Teutectic = 356°C), and 97Au-3Si(TEutectic = 363°C) have more specialized applications. These solders are not targeted for circuit board
assembly due to their high melting temperatures (and would hardly be cost-effective). As a matter of fact, the high working temperatures of these solders prohibits their use with traditional electronic fluxes; therefore processes are fluxless. The substrate surfaces have precious metal coatings or films that are readily wet by the solder without the need of a flux. However, the non-precious metal component of these solders (tin, germanium, or silicon) are susceptible to oxidation in air fired processes. As a consequence, melting of the solder is typically accompanied by the retention of an oxide skin on the molten material. The oxide layer will inhibit spreading by the solder such as in a sessile drop configuration. Also, break up of the oxide during soldering will cause some inclusions to be present in the joint.

Oxidation is limited by processing these solders in vacuum. In fact, the gold-based solders are most adaptable to vacuum processes because they do not use fluxes which will contaminate the furnace system. However, their high surface tension (particularly in the absence of a flux) cause their wetting to be sluggish. Pressure between the work pieces will "mechanically" assist spreading by forcing the molten solder into the gap.

The gold-based solders are used in the more structurally-oriented applications of electronic packaging. For example, these materials are used to attach the silicon chip (or "die") to the base of the package that will contain it; the process is often referred to as "die-attach". These solders are also used in the attachment of lids to package frames or "cans" in the final assembly of the part. In either applications, the melting temperatures of the solders and the fluxless attribute of their processing requirements cause the high temperature solders to be well suited for these applications. The higher melting points ensure that the device package will not come apart (or cause hermetic packages to develop leaks) during next assembly using the lower melting temperature tin-lead solders. The absence of fluxes prevents contamination of the package interior, a critical factor for integrated circuit reliability. Also, the precious metal solders are invaluable for the hermetic sealing of packages that require vacuum or special interior atmosphere for functional requirements.

The mechanical properties of the Au-Sn, Au-Ge, and Au-Si solders are shown in Fig. 4[12]. These materials are characterized by high strengths, yet very limited ductility when compared to the traditional tin-lead solders. Therefore, the application of these solders for the joining of parts with vastly
differing thermal expansion coefficients must be thoroughly investigated to prevent cracking of the solder or substrates (particularly ceramic materials) upon cooling to room temperature. The use of simple bi-metal beam theory can be used to obtain a first-order approximation to the stresses expected in the joint area[13]. Finally, processing parameters can be used to limit residual stresses in the joints. During the cool-down process, intermediate hold steps at elevated temperatures will allow creep deformation in the solder to relieve some of the thermal expansion mismatch stresses between the two materials.

II.B. Electronic package configurations.

METALLIC LEADS

Device packages come in many shapes and sizes. Package dimensions and input/output configurations (that is, leads, wires, or terminations or "I/O's") have been standardized by several professional organizations such as the Joint Electronic Devices Engineering Council (JEDEC), the Electronics Industry Association (EIA), and the Institute for Interconnection and Packaging of Electronic Circuits (IPC). Shown in Fig. 5 are package and input/output configurations for typical through-hole and surface mount devices. Through-hole components such as resistors and capacitors have leads or wires emanating from the device body. The leads are typically constructed from copper or copper-coated steel. Leaded surface mount packages are formed of several possible geometries: (1) the gull wing, (2) the "J" lead, and (3) the beam lead (not pictured). The beam lead is simply a strip of conductor emanating from the package frame. Surface mount packages may also be leadless; the solder connection is made to a metallized surface which is connected electrically to the package interior.

In the case of leaded packages, the lead material is frequently a difficult-to-solder material. The most common such materials are the low expansion alloys (Kovar™ or Alloy 42™)[14]. Even copper lead frames readily oxidize in storage and become unsolderable with typical electronic fluxes. The use of strongly active fluxes during circuit board assembly is strictly prohibited in order to prevent latent corrosion of the assembly during service by retained flux residues. Moreover, the large volume manufacturing processes used to assemble printed circuit boards require wettable (or "solderable") substrates to maintain production yields and limit the need for costly rework operations.
Two alternative techniques can be used to ensure wettability of the substrate surfaces. The first approach is to coat the surfaces with solder before assembly of the circuit board. The advantages of solder coating the package leads and circuit board pads individually first, is that highly aggressive fluxes can be used to ensure wetting of the substrate surfaces. Flux residues can be easily removed prior to circuit board assembly. Also, surfaces can be cleaned and immediately hot solder dipped; there is no storage time which typically accompanies circuit board assembly processes. The solder coating of circuit board pads is performed by the hot-air solder leveling (or HASL). In this process (Fig. 6), the printed circuit board is coated with flux and immersed into the molten solder. Upon withdrawal of the board, the excess solder is blown off of the pads by streams of hot air, leaving a smooth solder layer on the conductor surface. The coating of package leads (or "terminations") is termed "hot solder dipping" and as the term implies, the leads are fluxed and then immersed into a bath of molten solder. In the cases of both HASL and hot solder dipping, the critical wetting process has already been achieved; therefore, at the time of circuit board assembly, final formation of the joint simply encompasses re-melting of the solder layer and its mixing with solder added to the joint. Moreover, the solder coating protects the underlying substrate surface from oxidation or contamination, each of which will quickly deteriorate the wettability. Adequate protection is provided by solder thicknesses of >5.1 µm (200 microin.)[15].

The second technique used to improve solderability is the coating of the substrate (lead) surface with another metal which is more readily wettable, either as an inherent property of that particular metal or because of the process by which it is deposited. This coating is termed the "solderable" finish because it is to the surface of this layer that the solder wets. Because molten solder dissolves part of the surface metal to which it wets, the solderable finish must be sufficiently thick so as not to be completely dissolved by the solder. In those cases in which the solderable layer is completely consumed by the molten solder, de-wetting occurs (Fig. 1b) because the solder attempts to wet the underlying base metal which has not been properly prepared for solderability. Typically, the solderable layer is then coated with a "protective" finish. As the term implies, the role of the protective finish is to prevent contamination or excess oxidation of the solderable layer surface. During the wetting process, the solder film may wet the protective finish at the edge of
the spreading front; however, the protective is quickly dissolved into the solder film and wetting proceeds on the solderable layer. This process is shown schematically in Fig. 7. The protective finish must be sufficiently thick so as to offer adequate protection of the solderable layer. However, because the protective layer is dissolved into the solder, its thickness must be minimized so that the physical and mechanical properties of the solder in the joint are not degraded. Table 4 contains a list of recommended solderable and protective finishes for various base metals and alloys[15].

Steels and low expansion alloy leads typically use a solderable coating of nickel and a protective finish of gold. The gold film is typically replaced with a hot dipped tin-lead solder (protective) finish prior to assembly. This step is performed to prevent gold from entering the solder joint; gold can severely embrittles tin-containing alloys when its content exceeds approximately 4 wt%[16]. The likelihood of gold embrittlement increases markedly for surface mount technology because the relatively small solder joints contain a limited amount of solder with which to dilute the gold.

Coatings may also be intentionally added to limit solid-state metallurgical reactions between the solder and the substrate material. For example, copper, which is readily solderable, may be coated with a nickel layer to prevent the excessive growth of copper-tin intermetallic compound layers at the solder-copper interface, particularly in prolonged storage or high temperature service environments. Shown in Fig. 8 is the total intermetallic layer thickness formed between hot dipped 63Sn-37Pb solder and copper as a result of solid state aging at high temperatures. Excessive growth of the intermetallic layer causes it to consume the tin-lead protective finish. The exposed intermetallic surface quickly becomes non-wettable by solder so that joint solderability, and ultimately manufacturing yields, deteriorate.

METALLIZED TERMINATIONS (CERAMIC PACKAGES)

Many devices in surface mount technology use leadless (ceramic) packages. Solder joints are made directly to the package body by means of metallized regions, or "terminations" on the housing surface. Plastic leadless packages are still being developed. The two common package configurations are the leadless ceramic chip resistor (or capacitor) and the leadless ceramic chip carrier (LCCC). Shown in Fig. 9 are scanning electron micrographs and
cross sectional optical micrographs of the solder joints on an LCCC and a chip resistor. Although these are the most common configurations, new leadless package configurations are being developed as other devices are miniaturized and packaged for surface mount applications. For example, also shown in Fig. 9 is the package configuration and solder joint cross section (optical micrograph) for a miniature crystal resonator used in clock circuits. Note that the solder joints are pure lap joints; that is, there is no fillet (which makes inspection for manufacturing control very difficult to perform). Metallized coatings on the ceramic frame form the conductor to which the solder joint is formed. Typically, the metallizations are thick film inks comprised of a mixture of metal particles (the conductor such as Ag-Pt, Ag-Pd, Au-Pt-Pd, etc.) and ceramic or glass particles along with a vehicle to give the paste body. The ink is printed onto the ceramic after which it is fired at elevated temperatures; the glassy phase forms the adhesive bond between the ceramic and the fused conductor film. The metal conductor forms the solderable surface. The conductor layer is thin so that prolonged solder processing at elevated temperatures will cause its dissolution, thereby exposing the glassy layer which is not solderable. Excessive dissolution of the conductor layer is signaled by de-wetting of the solder layer.

The precious metal thick film systems are used on chip devices. The metal coatings are easily wetted by the solder; however, the metal is also readily dissolved into the solder. Therefore, a barrier layer of nickel or copper is plated over the thick film to form the solderable surface (followed with a tin or tin-lead protective finish). The de-wetting of solder films on chip device terminations may indicate a poor quality barrier layer.

Other thick films include the Mo-Mn process and refractory metal systems (Au-W or Au-Mo). In the Mo-Mn system, a thick film ink mixture of molybdenum and manganese is deposited on the ceramic. The ceramic is baked to adhere the thick film to the ceramic. Next, nickel is deposited (by evaporation) onto the Mo-Mn film; the nickel forms the solderable layer. Finally, a protective finish of gold is deposited on the nickel surface. In the refractory metal systems, tungsten or molybdenum is fired onto the ceramic. Then, gold is plated over the tungsten. The system is fired once again at elevated temperature to promote alloying between the gold and refractory metal; the alloyed region forms the solderable layer and the remaining gold serves as the protective finish. Some packages will add a supplemental
solderable layer of nickel followed with a tin-lead protective finish over the gold to improve solderability.

Because ceramic packages which use metallized surfaces for solderable interconnects are being used in surface mount applications, the gold protective layer must be removed by hot solder dipping in order to prevent solder joint embrittlement.

The seal between the ceramic package frame and the cover lid(s) is made to one or more of the metallization coatings noted above, using a gold-based solder (e.g., 80Au-20Sn). The absorption of the gold protective finish into the solder may be sufficient so as to alter the solder's composition and hence, change its melting point. Simple computations will determine the need to increase the processing temperature to account for such composition variations.

From the component solderability view point, the many different material layers that comprise the metallization (thick film, solderable layer, and protective finish). Plating processes used to deposit elemental metal layers (typically "barrel plating") must be well controlled to prevent decohesion between the layers and failure of the solder joint(s).

II.C. Substrate.

ORGANIC MATERIALS (PRINTED CIRCUIT BOARDS)

Printed circuit boards used in electronic products are typically laminated composites. Inside the circuit board is a weave comprised of glass or quartz fibers. The weaving is infiltrated with an organic material that hardens and gives the final circuit board its structural integrity. The organic "binder" is typically either an epoxy, Teflon, or a polyimide. Other weave and binder materials have been developed for applications with particular applications. Copper sheet is then bound to the laminate; this layer will be patterned and built up by metal plating processes to form the pads, traces, and plated through holes for signal transmission in the system. Copper layers may also be added to the interior of the circuit board for more complex electrical functions. The open regions between surface pads and traces may be coated with an organic layer that protects the underlying laminate from chemical solvents and water used in the processing of the assembly. Portions of the lands and traces may also be covered with solder mask to prevent the uncontrolled spreading of molten solder away from pads. This brief synopsis
is not meant to be a detailed thesis on the fabrication of circuit board substrates. Rather, its objective is to make the reader aware of the materials found in the laminate in order to illustrate their role in manufacturing processes. The reader is referred to References 6 and 7 for additional information.

The selection of the appropriate laminate is a function of cost constraints on the product and the anticipated service specifications. For example, laminates of fiberglass weave and epoxy binder are less expensive than those made of quartz and polyimide, respectively. On the other hand, more costlier Teflon glass is preferred to fiberglass epoxy for microwave circuits because the dielectric constant of the former minimizes the degradation of high frequency signals characteristic of these applications.

Because the selection of substrate material is typically determined by the product requirements, the manufacturing processes must adapt to the properties of the laminate. The two primary concerns of circuit board damage by manufacturing products are (1) chemical attack (including absorption of liquid species) by fluxes and cleaning solvents/solutions and (2) heat damage. In the case of chemical damage, properties such as surface resistivity and chemical degradation (including the absorption of solvents and water) can be generalized for particular categories of circuit board materials[17]; however, it is best to refer to the manufacturer's product specifications for actual design guidelines.

On the other hand, heat damage to the laminate is slightly more "elusive" because it can appear as several defects with varying degrees of propensity, depending upon the particular process parameters selected for manufacturing. The property which determines the heat sensitivity of the laminate is the glass transition temperature, \( T_g \), of the organic binder. The \( T_g \) of most epoxies used in circuit board laminates is approximately 110°C to 120°C and that of the polyimide materials, 250°C[17]. As the temperature of the laminate approaches the glass transition point (but does not exceed it), the organic binder weakens, largely due to a loss in the elastic modulus (or stiffness). However, at temperatures which exceed \( T_g \), the binder softens due to changes in the molecular structure of the polymer. The difference between the material weakening at \( T<T_g \) and its softening at \( T>T_g \) is that in the latter case, forces on the circuit board will cause a permanent set or distortion to the laminate after cooling. At temperatures \( T<T_g \), the laminate will return to its
initial configuration upon cooling, as long as the applied forces are not overly strong and the temperature is not very close to the glass transition point.

CERAMIC MATERIALS (HYBRID MICROCIRCUITS)

As opposed to circuit boards assemblies, hybrid microcircuits use ceramics as the base material. Hybrids utilize surface mount technology and integrated circuitry for miniaturization. Such systems are highly reliable because the thermal expansion coefficient of the device packages (which are typically ceramic) very closely matches that of the ceramic substrate, thereby reducing thermal mechanical fatigue damage to the solder in the joints. As a consequence, hybrids are used in high temperature applications, conditions which would degrade the properties of organic laminates (and discrete devices). Traditionally, oxide ceramics are used for the circuit substrate: alumina (Al2O3), beryllia (BeO), magnesia (MgO), and zirconia (ZrO2)[18]. Because of the miniaturization of the electronics and the high power requirements of hybrid circuits, the selection of a particular substrate material is based upon both its thermal properties (conductivity, expansion, heat capacity) and dielectric properties for high frequency application. Often in systems which generate large amounts of heat (e.g., very high frequency circuitry such as for microwave transmission or radar systems), a metal backing plate will be soldered to the underside of the substrate to improve thermal conductivity away from the circuits. Engineered ceramics such as aluminum nitride are also being considered for hybrid microcircuit substrates due to their improved thermal conductivity properties over the oxide ceramics.

Although the ceramic substrates can withstand very high static temperature conditions, they are susceptible to cracking under high heating and cooling rates (thermal shock conditions). This factor must be accounted for when developing soldering processes for hybrids.

Solders do not wet ceramic surfaces. Therefore, metallization coatings are applied to the ceramic to which the solder will bond. These coatings are categorized as either thick films (12-25 μm) or thin films (tens to hundreds of angstroms); thick films are the predominant metallization technique for hybrid microcircuits. The films are created by the deposition of ink material on the ceramic by stencil printing. The ink contains metal powder to act as the conductor. Metals include copper, nickel, gold-palladium-platinum, silver-platinum, etc. The ink also includes oxide powder and glass binders that
promote adhesion of the thick film to the ceramic and organic binders for the printability (or body) of the ink. After printing, the ceramic is fired at elevated temperatures, driving off the binder material and causing the glass and oxide to promote adhesions of the film to the ceramic. The precious metal inks can be fired in air; however, the copper and nickel films (albeit which are less expensive than the precious metal based materials) require non-oxidizing atmospheres during the firing process.

Although readily solderable, the precious metal thick films are susceptible to excessive intermetallic compound layer formation at the thick film/solder interface. The thick intermetallic layer and coincidental consumption of the thick film layer may jeopardize the mechanical integrity of the solder joint. Therefore, assembly processes as well as rework and repair practices must be tightly controlled in order to prevent the loss of metallization to metallurgical reactions with the solder.

III. Manufacturing Processes - Circuit Board (and Hybrid) Products.

The identification of soldering parameters will be highly dependent upon the particular process used to manufacture the device or system, as well as the configuration and specifications of the component, itself. However, numerous guidelines can be used to develop process parameter "windows" for prototype trials as well as assist in the troubleshooting of problems that arise in the course of production. It is the intent of this section to illustrate several of these generalized principles. Several of the particular processes and equipment will also be briefly described.

III.A. Surface preparation and protection.

The solder alloy must wet the substrate surface(s) in order to form the joint. Shown in Fig. 10 are two solder joint configurations. The recommended dimensions of the hole, pad, and wire are provided by numerous design guidelines and specifications; one such document is listed in Reference 19. The substrate surfaces to be wetted by the solder are the copper pad (land) on the printed wiring board or the thick film layer on a ceramic substrate, and the package lead surface. Wetting by the solder forms a mechanical linkage between the package and the circuit board through the lead and pad,
respectively. Since the wetting phenomena requires that the molten solder come into direct contact with the substrate metal, organic contaminants and oxide layers must be removed from the substrate surface(s) prior to performing the soldering process.

Organic films (including mold releases, machining lubricants, lubricating oils, and finger prints) are typically removed through the use of organic solvents such as trichloroethylene and carbon tetrachloride. However, these solvents are being restricted from use by international agreement (Montreal Protocol and its follow-up amendments) due to their potential to deplete the stratospheric ozone layer. Aqueous- and semi-aqueous-based cleaning substances are replacing many of the solvents. Unfortunately, these aqueous materials are not adaptable to vapor degreasing processes.

Caution: **Silicone-based lubricants and coatings are extremely tenacious and should be restricted from contact with surfaces targeted for soldering operations.**

The oxide layer on a metal surface can be described by three general properties which are pertinent to solder processing: (1) thickness, (2) tenacity, and (3) chemical inertness. The thickness of the oxide is a function of the underlying metal as well as the time of exposure and the environmental temperature. Thicker oxide layers are termed "scales" and relatively thin layers are referred to as "tarnishes". Tenacity describes the ability of the oxide layer to adhere to the base metal. Specific volume differences between the oxide layer and the base metal can result in mismatch stresses that cause the oxide to separate (or "spall") from the base metal. Finally, chemical inertness describes the oxide layer's capacity to resist chemical attack.

Two approaches can be used to remove oxide films: (1) mechanical abrasion and (2) chemical cleaning. Mechanical abrasion is used primarily to remove thick scales or thin, yet chemically resistant oxide films (e.g., aluminum, nickel, or stainless steel); its use on electronic packages is extremely limited by possible damage to leads or the package structures. Mechanical techniques, which use grits or particulates, should be followed with a chemical etch to remove embedded particles which can deteriorate solder wetting. Chemical cleaning is frequently categorized as "etching" when the surface is lightly attacked or "pickling" when heavy oxide films must be removed. Chemical removal of oxide layers relies upon the use of
inorganic acids such as hydrochloric, nitric, or sulfuric acids. Stronger acids (or concentrations) are required for thicker layers or more chemically inert films. Metals which quickly form highly protective oxide layers must be soldered immediately following chemical cleaning to prevent re-oxidation of the surfaces.

Generally, organic contaminant layers are impervious to inorganic acids. Therefore, organic films must be removed prior to the use of acids for oxide removal functions.

It should be understood that fluxes are also chemical cleaning agents. Consequently, substrate surfaces must be free of organic contamination. Also, the fluxes used in the assembly of electronic hardware have rather low corrosive activity so as to prevent damage to device packages or leave active residues that may cause general corrosion of metal surfaces during service. Therefore, fluxes are only suitable for removing light tarnish layers.

An alternative approach to obtaining and assuring solder wetting of the particular base material surface by cleaning techniques is to coat the surface with solderable and protective finishes. As noted in the previous section, the solderable coating must be adequately thick so as not to be completely dissolved in the molten solder. In the case of the protective finish, it must be sufficiently thick to prevent contamination of the solderable layer, but not excessively thick so as to contaminate the solder and jeopardize its properties.

III.B. Assembly practices.

The assembly of electronic products includes three primary steps: (1) the placement of solder and devices on to the circuit board, (2) a heating procedure to reflow the solder, and (3) post-assembly steps that include cleaning, inspection, and rework. Device placement and the post-assembly practices are as important in the manufacturing process as is the reflow process, itself.

Solder paste properties and printing techniques through either a screen or stencil (Fig. 11) are critical to yields in surface mount assemblies. Solder paste powder size, vehicle and flux[20,21]; stencil aperture dimensions, material, and side wall geometry[22,23]; as well as printing parameters[24,25] such as blade stiffness and pressure affect the occurrence of defects such as solder bridging between conductors, insufficient solder which causes open
circuits, and solder balls (Fig. 1) that can cause intermittent signal interference due to movement in the assembly.

The placement of devices onto the circuit board for subsequent reflow operations differs between through-hole technology and surface mount technology. In the case of through-hole product, the leads of the device are inserted into the appropriate holes in the circuit board; the holes locate the device's position and maintain it through follow-up processing. In some assemblies, machine insertion has replaced the use of manual operators. The hole diameter should be generally 0.15 - 0.20 mm (0.006 - 0.008 in.) larger than the wire diameter to permit capillary filling by the solder which ensures electrical continuity and adequate mechanical strength. Smaller diameter holes increase the likelihood of interference between the lead and hole wall that can damage the conductive layer on the latter. Design guidelines should be referred to for recommended lead and hole dimensions[19].

Surface mount attachment demands increased concern for part location. The placement of these devices on the circuit board is extremely difficult to perform manually due to their relatively small size, close proximity on high density products, as well as the number of parts populating many assemblies. Therefore, device placement is nearly always automated. Many of the fine pitch, high I/O packages have very delicate leads. It is critical that those leads are not damaged during installation; even the slightest distortion can result in shorted or opened circuits at the solder joints. Devices are placed atop a deposit of solder paste which had been previously printed onto the bonding pads. Machine adjustments (or manual dexterity) should allow the package to gently rest on the paste. Excessive pressure or lateral movement that may smear the paste between pads, can cause short circuits upon reflow.

Generally, the larger, multiple I/O packages such as Small Outline Transistors (SOT), Plastic Leaded Chip Carriers (PLCC) such as shown in Fig. 5 move very little during melting of the solder, except for a slight amount of sinking under the package weight. Therefore, package alignment in these instances is dependent largely on part position at the time of placement.

Smaller surface mount devices, such as ceramic chip resistors and capacitors, rely upon the surface tension of the molten solder to effect their proper alignment on the bonding pads. An in-balance between forces on the two terminations results in the chip being lifted off of one pad (Fig. 12); the defect is known as "drawbridging" or "tombstoning". The source of this defect
includes both the design of the circuit board pad configuration as well as the assembly process parameters[26,27]. Circuit board pad design recommendations include increasing the pad extent under the package and limiting pad extension beyond the end of the termination.

Causes of dissimilar surface tension forces due to processes at the assembly stage are (1) variations in the properties and quantity of solder paste deposited during the printing process and (2) registration error of the package with respect to its corresponding solder paste deposits (by the pick-and-place machine or the operator in manual operations), and (3) the reflow process parameters. Different quantities of solder paste on the two joints increases the likelihood that one joint will reflow prior to the other, giving an immediate surface tension imbalance that pulls the chip to the molten joint, and subsequent tombstoning. The propensity for this scenario increases for pastes that have poor tackiness (the "sticky" factor that holds devices to the circuit board). Finally, the joint with more solder generally has a greater surface tension component acting on the chip. Initial registration of the device over the solder paste deposits is important. Surface tension forces have a limited scope of effectiveness. Should one of the chip terminations be displaced from the solder paste, it becomes increasingly more difficult for the surface tension forces to pull it back into position. The result can be an open circuit or, depending on the orientation of the mis-registration, cause tombstoning.

The reflow process can be developed to prevent tombstoning. Excessive part movement (or "swimming") caused by vaporization of paste volatiles increases the likelihood of tombstoning. Therefore, preheating of the paste should be adequate to remove those volatiles prior to the reflow step. Tombstoning is also cause non-simultaneous melting of the solder in the two joints. Proper pre-heating of the circuit board prior to reflow, as well as the use of slow heating rates, will allow the device, solder, and substrate to have a nearly uniform temperature at the time of reflow.

III.C Process development.

The available soldering processes, whether hand operations with an iron, highly specialized processes using laser energy, or large volume
assembly by wave soldering, all have a similar purpose; that is, *they deliver heat to the joint area*. The various techniques utilize different methods of supplying that heat, e.g., infrared, laser, thermal conduction or convection from a source, microwaves, or the heat of vaporization from liquid condensation. The heating process(es) must produce an acceptable product, not simply acceptable solder joints. After all, perfect solder joints are of no use if the whole assembly will not function properly after the assembly process.

The heat energy applied to the joint area must support several functions. Once these functions are understood, the engineer can develop the correct process cycle to manufacture the particular product. The objectives of the heating for the fabrication of the solder joint are summarized below:

1. Increasing the temperature of the substrate and devices to prevent their damage by thermal shock as well as to prevent heat sinking effects that inhibit melting of the solder.

2. Activation of the fluxes' chemical activity that will remove tarnish layers from the surfaces to be joined;

3. Melting of the solder and the promotion of its metallurgical reaction with the substrate surface.

As in all manufacturing endeavors, process "windows" are established by defects resulting from either excessive or insufficient quantities; in this case, heat energy. Large scale assembly processes such as wave soldering, vapor phase reflow, or techniques that use one of the various types of furnaces are generally characterized by heat energy delivered to the entire assembly, rather than localized heating of the joint area as is the case with hand (manual) or directed-energy processes (laser or fiber-optic infrared). The generic thermal profile of these processes is similar to that shown in Fig. 3.

The first objective of the preheat stage is to activate the flux. The fluxes' tarnish removal reactions, like most chemical processes, increase as the temperature is raised. Fluxes are engineered to have their maximum activity at temperatures below that of the solder so that the surfaces will be wettable when the solder melts. Because the traditional electronic solder has
been the eutectic or near-eutectic tin-lead alloy with a melting temperatures of 183°C and 183-188°C, respectively, the activation temperature range of most fluxes (rosin-based and organic acids) have been engineered to lie in the range of 150-170°C. During the oxide removal process, the flux coats the cleaned surfaces, thereby preventing re-oxidation of the metal surfaces. Fluxes with this activation temperature range will give adequate performance with higher melting temperature solders (although other properties of the fluxes may limit such uses). However, these fluxes may not provide adequate tarnish removal capabilities for lower melting temperature solders. These solders are typically specified for heat sensitive applications (including step soldering) so that simply raising the working temperature of the molten solder in order to activate the flux defeats the intended purpose of the low temperature solders.

The second objective of the preheat stage is to gradually increase the temperature of the substrate (laminate of hybrid ceramic) and devices to prevent thermal shock at solder working temperature. Recall that the working temperature of the solder is typically 40°C above the liquidus temperature. Excessively quick heating of the assembly can cause "hot spots" to develop in organic laminates, causing distortion, or in ceramic substrates (hybrid microcircuits) that cause cracks. In furnace reflow processes, pre-heating intervals are typically on the order of 1-3 min.

Proper control of the time and temperature conditions is required at the preheat stage. Excessively low temperatures or minimal preheat times can ultimately cause poor wetting due to inadequate removal of tarnish layers on the substrates or thermal shock damage to the assembly at the reflow stage. On the other hand, higher than necessary temperatures or prolonged preheat periods can promote re-oxidation of the substrates to an extent such that the flux is ineffective. Moreover, the flux itself may experience thermal breakdown (or "cracking") from extended heat exposure and lose chemical efficacy. Oxidation and flux degradation can be limited by processing under inert atmospheres.

Following the preheat step is the reflow stage (or "spike") of the heating schedule during which the solder melts and wets the substrates to effect formation of the joint. It is important to minimize the reflow time and temperature to which the assembly will be exposed. Therefore, heating and cooling rates to and from the reflow spike, respectively, should be as quick as
possible without excessive thermal shock to the assembly. As noted earlier, the reflow (or working) temperature is typically 40°C above the liquidus point of the solder. This temperature buffer is added to ensure that substrate temperatures are sufficiently high to prevent partial solidification of the solder ("cold joint"). The additional temperature improves the fluidity of the solder and hastens the metallurgical reaction between the solder and the substrate material(s); both factors appear as an improvement in the wetting performance of the solder. The time period at reflow depends upon the particular heating technique equipment, being typically 5-10 sec for wave soldering; 20-30 sec for vapor phase reflow; and 30-90 sec for most furnace operations. Excessive heat exposure is indicated by: (i) damage to devices or substrates (crazing and warpage of laminates or cracking of ceramics); (ii) the presence of difficult-to-remove flux residues caused by thermal degradation; and, (iii) severe oxidation of the solder. Flux degradation and oxidation can be reduced for prolonged reflow cycles by using an inert atmosphere of nitrogen.

The cooling rate of the assembly after the reflow spike is also a critical parameter in the process. Controlling the cooling rate is dependent upon the type of equipment/process in use. As noted earlier, a fast cooling rate is desired in order to minimize thermal exposure to the assembly. However, an upper limit must be put on the cooling rate to prevent thermal shock to the laminate or device structures as well as to lessen residual stresses in the joint. After solidification of the joint, a "rigid" attachment has been formed between the device package, the solder, and the laminate or ceramic substrate so that residual stresses are generated in the joints due to thermal expansion mismatch between these structures. Residual stresses can reach magnitudes which cause cracking in the solder as well as in the device package. Decreasing the cooling rate causes the solder in the joints to plastically deform by time-dependent creep, thereby relaxing the residual stresses below damaging levels.

It has been noted by several investigators that a faster cooling rate of the solder refines the solder microstructure[28,29]. Generally, a finer microstructure improves the mechanical strength of a metal or alloy. However, further studies indicate that the solder's microstructure coarsens[30], and its strength properties decrease (Fig. 13)[31], as a result of
room temperature aging, suggesting that any long term strength benefit
derived by the cooling rate after reflow may be only temporary.

At this point, the application of these guidelines will be illustrated by a
brief outline of four equipment/processes used in manufacture of electronic
assemblies: (1) vapor phase reflow, (2) furnace reflow, (3) wave soldering, and
(4) hand soldering. These technologies not only include the majority of
manufacturing processes used to assemble electronic products, but they also
represent vastly different types of techniques. Limitations on each of the
processes should be taken into consideration with the points made above to
determine the proper processing technique for a particular product from a
technological point of view. Of course, the final decision must also include
economic considerations such as the effects of capital investment for
automated assembly equipment and the cost of manual labor on the customer
price of the assembly.

Vapor phase reflow is the process in which the source of heat
ergy is the latent heat of vaporization released to the assembly when a
vapor condenses into its liquid state. Following a preheating step, the
assembly is placed into a vapor zone. The vapor condenses on the assembly,
bringing its temperature up to the vaporization temperature. Recall that
vaporization/condensation, like melting/fusion, is a phase transformation
during which the temperature (boiling point) remains constant. A safety
feature of this process is that the temperature of the assembly does not exceed
the vaporization temperature of the fluid medium. The traditional fluid used
for reflow of the tin-lead solders is FC-70 ("Fluorinert", 3M Co.) with a boiling
point of 215°C. Fluids with higher boiling points in the range of 220-265°C are
also available. These fluids, as is the case of FC-70, are chloro-fluorocarbons
(CFC) which have recently come under strict regulation as ozone depleting
agents. Vapor phase equipment is available for batch processing (small lots or
prototyping) and as in-line equipment for large volume assembly.

The heating schedule is somewhat difficult to control, particularly
when the assembly is being transported between the preheat stage and the
vapor bath. Also, heating is typically very quick as the unit enters the vapor
cloud. The fast heating rate can cause immediate volatilization of the high
vapor pressure constituents in solder paste. Solder balls and excessive part
movement (and subsequent misalignment) are often observed on assemblies
fabricated through this technique. It is important that the preheat step be of
sufficient duration so as to remove the volatile components in the solder past prior to reflow. The heating rate is so quick that not all devices or the laminate will be at the same temperature; devices typically heat up quicker than the circuit board so that solder wicking of leaded devices is also observed under improperly selected process parameters.

**Furnace heating** is used extensively for large volume manufacturing operations. Heating and cooling rates as well as process temperatures and times can be tightly controlled, depending upon the heating technique(s) and the number of heat "zones" in the furnace. Therefore, furnace processes provide the manufacturing engineer with extensive latitude to reduce the number of solder joint defects in an assembly as well as to handle a wide variety of assembly sizes and configurations. Inert cover gases limit oxidation of the solderable surfaces, thereby improving solderability, particularly with use of the new low residue fluxes developed to eliminate post-assembly cleaning processes.

A wide range of heat techniques exists. These include infrared elements (radiation), circulating hot gases (convection), heated base plates along atop the assembly is dragged (conduction), or any one of a combination of these methods. While infrared heat sources tend to be more energy efficient as opposed to forced, heated air, this technique suffers from selective heating of devices, based upon the material absorptivity of the projected infrared radiation. Hot spots on highly absorbent surfaces can damage device packages while cooler locations (include those areas shadowed by neighboring packages) will inhibit complete reflow and subsequent wetting by the solder. Combining forced convection with the infrared heat sources "smoothes" the temperature gradients across the assembly. It is extremely important to monitor developmental boards with thermocouples as part of the prototyping phase. Thermocouples should be placed at the corners and edges as well as the center of the laminate or ceramic substrate. Devices of extreme sizes or package color and shininess should also be checked for a temperature profile prior to actual product assembly.

**Wave soldering** is a relatively unique approach to attach devices on through-hole and mixed (through-hole and surface mount) technology circuit boards. The process is shown schematically in Fig. 14. Wave soldering is a compromise between global versus localized heating configurations. Although the pre-heating step raises the temperature of the entire assembly,
the actual soldering operation locally heats the laminate to the bath
temperature, creating significant thermal gradients within the substrate as
well as in the package leads of the device. Therefore, although the ensuing
thermal stresses are acceptable for organic laminates, ceramic substrates for
hybrid circuits are subject to cracking and therefore, must be processed by
very controlled procedures.

The wave soldering technique is used largely for through-hole
assemblies. However, relatively simple surface mount devices can also be
attached, as well. Through-hole devices are secured to the board by means of
their leads while surface mount packages must be glued into place prior to
soldering of the circuit board. Unlike through-hole packages which are all
generally amenable to wave soldering, only small outline transistor (SOT)
packages and discrete, leadless chip (chip resistors, capacitors, etc.) surface
mount devices are attached by wave soldering. Larger packages such as leaded
and leadless chip carriers are not wave soldered due to damage by exposure to
the flux and the molten solder, as well as their package configurations causing
a greater number of defects[32].

Wave soldering is an in-line process. The circuit boards are attached to
a conveyor. Mechanical support of organic laminates on the conveyor is very
important in wave soldering because solder bath temperatures typically cause
the laminate to exceed its binder's glass transition point, making the circuit
board very soft. Inadequate support of particularly large boards permits
excessive sagging at the elevated temperatures. On the other hand, anchoring
methods that do not readily permit thermal expansion will place a load on the
board, causing warpage and twisting. Sagging, warpage, and twisting, when
present as the laminate cools through the glass transition temperature, will be
permanently set into the board at room temperature.

In the wave soldering process, the assembly first passes though the
fluxer; flux is applied by means of either an immersion process, a wave system
similar to that for the solder, sprayers, or creating a flux foam that coats the
board. The circuit board is then passed through a pre-heat station in order to
activate the flux and limit thermal shock to the board at the solder wave.
Finally, the board enters the molten solder wave. Noted in the schematic in
Fig. 14 are three regions of the wave denoted by the letters: "A", "B", and "C"
are the entry, interior, and peel-back regions, respectively. The entry region
(A) is typically very turbulent; the goal here is to force the molten solder
around the package bodies, so that it will contact the leads, terminations, and bonding pads. The metallurgical reactions associated with wetting take place in the wave interior region (B). The peel-back region (C) as the term suggests, is where the molten solder retreats from the circuit board surface and releases back into the bath. This portion of the wave plays a crucial role in the type and number of defects (icicles, bridges, and dross particle inclusions) on the exiting assembly.

Wave soldering provides an excellent example of the concept of "design for manufacturing" because defective solder joints are as much a result of poor circuit board layout (design) as they are caused by inadequate process control (conveyor speed, take-off angle, peel-back region geometry, etc.). Hole diameters or clearances of 0.076-0.40 mm (0.003-0.015 in.) provide adequate capillary filling action for the solder and at the same time, permit the escape of flux volatiles upon heating. The spacing between devices as well as the orientation of the leads and terminations with respect to the direction of board travel through the wave significantly affects the number of defects such as solder bridges (shorts) between leads, skips (no solder), and icicles[32,33]. Also, the selection of devices and circuit board laminate must be capable of withstanding the temperatures of the solder (which may be 70-80°C above the liquidus temperature for adequate heat transfer to the assembly). These extreme temperatures coupled with the large scale motion of the solder in the wave increases the amount of base metal dissolution from the circuit board bonding pads and the device leads (be it the base metal or plated coatings). Therefore, the base metal cross sections, and in particular, the thickness of coatings, must be adequate to ensure that sufficient material remains for soldering joint integrity after the wave soldering process.

Finally, proper process development will also help to minimize the defects mentioned above. As an in-line process, wave soldering can accommodate the use of inert atmospheres to minimize re-oxidation of the solderable surfaces which improves the surface wetting of the solder, particularly with use of the less active "low residue" fluxes and limits dross formation on the solder bath. Besides the documented effects of parameters such as pre-heat and reflow temperature or time on defects, the solder wave geometry also has a significant impact. The entry region must provide adequate turbulence to ensure that the solder reaches all of the wettable surfaces. The pull-back region must allow the solder to pull down and away
from each individual joint or conductor surface; otherwise, the solder will be
dragged across two or more leads, forming a bridge. The conveyor speed, take-
off angle of the board relative to the wave, the wave height and velocity, as
well as the surface tension of the solder are all factors that impact the defect
count. For example, Artaki, et al.[34] observed that in the case of wave
soldering with 58Bi-42Sn, the circuit board velocity must exceed that of the
lateral velocity of the solder in the wave at the peel-back region to prevent
dross inclusion and icicling of the conductor traces and bonding pads.
Changing the entry and peel-back region geometries of the wave is obtained
through the use of baffles which alter the flow velocity and configuration of
the molten solder

Hand (or manual) soldering remains a very important technique in
the assembly of electronic products. Hand soldering is used in both the
assembly of electronic products as well as when repair and rework of defective
units is required. Advantages and disadvantages of hand soldering encompass
both technical and economic factors. Hand soldering is often designated for
low volume, very high reliability electronic systems (e.g., spacecraft, weapons
applications, satellites) because the operator can detect defects immediately
and correct them at that time. This attribute reduces the chance that defective
joints will pass undetected through subsequent inspection steps. Hand
soldering is also used to place heat sensitive or oversized devices on a circuit
board - such devices may be incompatible with machine processes - or when
the particular part requires an altogether different solder alloy.

Hand soldering has many limitations as well. Foremost, it tends to be
very costly because it is labor intensive and time consuming relative to mass
assembly techniques. Secondly, the increased miniaturization of electronic
systems have further limited the use of manual processes with a soldering iron
(or hot gas and hot bar techniques, as well). The hand soldering of surface
mount devices is very precarious. The geometry of solder joint fillets can vary
significantly when fabricated by hand soldering because the quantity of
solder is difficult to control by the operator. Reliability of surface mount
solder joints is very sensitive to the configuration of the joint. In addition, the
small size and increased density of circuit board assemblies increases the risk
of both mechanical and heat damage to device packages and leads.

Consideration of the use of hand soldering must necessarily include the
selection of the soldering iron, flux, and solder wire. The soldering iron is
characterized by: (1) the tip temperature, (2) temperature control technique, (3) the tip geometry, and (4) the power rating. Typical tip temperatures for electronic assembly processes are 260-370°C (500-700°F). The optimum feedback control is one which maintains the tip temperature, even when "loaded" by the soldering process. This condition provides the greatest control on heat transfer for reproducible operations. The tip geometry should be of a configuration which matches the lead (or termination) surface, the goal being to maximize conductive heat transfer from the tip to the joint area. The tip geometry should also accommodate the restricted space resulting from neighboring devices on the circuit board. Hand soldering of high-value electronic systems requires a great deal of operator expertise (and therefore, extensive training) because of the damaging potential of the heat source. Finally, the power rating of the iron should match the joint configuration. Simple conductive heat transfer calculations are adequate to approximate the power requirements of a particular joint configuration[35].

The soldering iron provides both the pre-heat and the reflow heat necessary to make the joint, largely through conduction. Therefore, the sequence of fluxing, heat application, and solder introduction to the joint is very important. For typical through-hole solder joints with wire diameters of 0.51-1.0 mm (0.020-0.040 in.) and a 315°C (600°F) soldering iron tip temperature, the first step is to apply flux to the joint area, covering the hole interior, land, as well as the lead surface. Then, the iron is brought in contact with the lead of the device; the soldering iron tip should not contact the land of the circuit board hole (or the conductive thick film of the ceramic substrate on hybrid devices) to prevent its de-bonding from the laminate. The solder wire contacts the lead on the opposite side to the iron. Melting of the solder provides an indication that the lead is sufficiently hot for joint formation to take place. The solder wire should not contact the tip; its premature melting will obscure the temperature condition of the lead. The solder wire and tip should remain on the lead until flow (through the hole if present) has been completed.

The process time should be in the range of 4-7 sec for typical electronics applications. Time periods exceeding 10 sec indicate a possible discrepancy with the process such as inadequate soldering iron power, low tip temperature, or poor solderability of the substrate materials. Soldering times beyond 10 sec. increase the likelihood of heat damage to the device, the flux
coating, and to the circuit board (or ceramic substrate). Reflow will be delayed for devices with larger leads or thicker, multilayer boards that present an enormous heat sink to the soldering iron. In these circumstances, pre-heating the lead with the iron can be performed; however, the flux should not be applied during this pre-heating step as it will be thermally damaged. Pre-heating the circuit board should not be performed unless prior testing has confirmed that it is not damaging to the laminate material.

IV. Assembly Processes - Device Packaging.

Electronic packaging has traditionally encompassed the fabrication of interconnects for signal transmission between silicon chips, higher level devices, circuit board cards, and between external equipment such as power supplies and backplanes. Nevertheless, soldering technology also has a significant role in the construction of packages which contain the first level devices (e.g., the silicon chip). Often, it is necessary that the process engineer be aware of the techniques used to construct the package structure in order to prevent damage to it or its functionality (e.g., hermeticity), by assembly processes such as pre-cleaning, solder processing, or rework and post-assembly cleaning. A brief description will be given of several of the more common packaging approaches for electronic devices with the objective that the processing engineer be aware of the limitations imposed by each configuration.

Although seemingly out-of-date, vacuum tubes are still used for many electronic applications with very exacting performance requirements, yet without restrictions on footprint area or heat generation. Vacuum tubes are heat sensitive due to the glass-to-metal seal between the bulb and the supporting base. Therefore, hand soldering is specified for these applications in which the heat is localized to the joint area only; nevertheless, excessive heat transfer conducted to the glass joint area must be avoided. Finally, the formation of the glass-to-metal seals typically requires the use of low expansion alloys (e.g., Kovar™, Alloy 52™, etc.) as the lead material. These materials are difficult to solder and are typically coated with a solderable finish.

Silicon chip microcircuits may function as a simple transistor (replacing the vacuum tube), or encompass a multitude of electronic functions.
such as in the case of a memory chip or as a microprocessor for computer control. The chip (or "die") must be protected from the service environment and so is mounted in a package. The package has three parts: a base on which the chip is bonded, a frame that forms the walls and has leads, and the lid or cover which encloses the package (Fig.15). The base and the frame may be re-attached. The packaging material is either: a metal "can", a thermosetting plastic (phenolic) or an oxide ceramic (and in the future, a engineered ceramic). The chip can be attached by an organic adhesive (ceramic or plastic packages), a high melting temperature solder (metallized ceramic packages), or by means of solder bumps ("flip chip" [1]) between the die and the package base. The high temperature, precious metal solders: Au80Sn20 (T_{eutectic} = 278°C), Au88Ge12 (T_{eutectic} = 361°C), and Au97Si3 (T_{eutectic} = 363°C) are used for chip (or die) attach to the package. The higher melting temperatures allow next-assembly steps using the traditional tin-lead solders without remelting the chip bond. The precious metal basis of these solders, together with precious metal thick film finish on the ceramics, eliminate the need for fluxes to remove tarnish films to promote wetting. Small wires are attached by thermocompression or ultrasonic bonding, between the chip and the package frame as the first step for conveying electrical signals from the die, through the frame, to the out leads.

In the case of flip chip technology, the silicon die is attached to the package by a series of solder bumps. The solder bumps not only fasten the die to the package but also conduct the electrical signals to the package circuit layout (and eventually to the package I/O's). The high melting temperature lead-tin solders, 95Pb-5Sn and 90Pb-10Sn are used for the solder bumps. Their solidus temperatures, 308°C (590°F) and 275°C (527°F), respectively, allow subsequent installation of the package on the circuit board or ceramic by processing with tin-lead solders.

Finally, the lid is bonded to the frame to enclose the package. Localized heating techniques such as rim sealers for metal cans allow the use of the gold-based solders or the higher melting temperature brazing filler metals for the attachment of the cover to the frame. Soldering can provide a hermetic seal, particularly for ceramic packages. Thick film metallizations form the solderable coatings on the lid and frame. Ceramic packages may also be hermetically sealed, using a gold thermocompression bonding technique. However, temperatures of the entire package may exceed 350°C during this
bonding process. Plastic molded packages may be sealed by the use of adhesives or plastic "welding" of the lid and frame.

The number of leads exiting the frame is selected, based upon the functionality of the chip inside. Increased miniaturization coupled with increased device functionality have required packages to have higher lead counts, but with smaller, more closely spaced leads. Smaller leads increase the likelihood of them being damaged in handling and device placement. The spacing between leads is referred to as the "lead pitch". Ceramic packages with low expansion alloy lead material are used to meet hermeticity requirements. Glass-to-metal seals at the lead/frame junction must not be damaged by subsequent solder processing. Plastic packages with copper leads are specified for nearly all other applications that do not have hermetic or high temperature (e.g., "burn-in") requirements.

V. Post-Assembly Cleaning

Of the many facets which comprise the soldering process, none has changed to the extent that post-assembly cleaning technology has over the past 5-10 years. This revolution is due in large part to the destructive effect of chlorofluorocarbon (CFC) solvent-generated gases on the stratospheric ozone layer. CFC solvents, such as 1,1,1-trichloroethane, trichloroethylene, and carbon tetrachloride have been the "workhorse" cleaning agents for the removal of flux residues on soldered electronic assemblies. In response to the environmental concern, newer safe cleaning processes (based upon aqueous and semi-aqueous solutions) are being implemented by the electronics industry to meet state, federal, and international regulations on the use of ozone depleting substances (ODS).

While always considering the economic details of each of these methods, the manufacturing engineer must regard the technical aspects of the cleaning processes: (1) its effectiveness to remove residues in order to prevent as loss of service reliability by corrosion damage and (2) deterioration of laminate and package materials by contact with the cleaning solution. Standardized test methods have been established to evaluate the efficacy of cleaning techniques to remove both ionic and organic residues[36,37,38,39]. However, data on material compatibility with new cleaning agents and processes may not be readily accessible to the process engineer, thereby
requiring prototype testing on site. Some situations which may require
attention include the following: Ceramic materials used for packages, hybrid
microcircuit substrates, or discrete chip resistors and capacitors have a
tendency to absorb water. Particular to chip capacitors, the absorbed water
may affect the capacitance value of the device. Absorbed water can damage a
ceramic (as well as the plastic in packages and circuit board laminates) if
present during the soldering process due to the violent vaporization of water
into steam. The water used in aqueous cleaning processes can be desorbed by a
pre-assembly annealing treatment to prevent such damaging effects. In the
case of hermetic packages, the glass-to-metal seal on the leads (or used to fix
the lid to the frame) may be very sensitive to degradation caused by the pH of
aqueous solutions. General degradation to the solder joints by cleaning
solutions can include the following mechanisms: galvanic corrosion of leads,
pads and the solder; the swelling and distortion of organic materials (plastic
packages, solder mask, and circuit board laminate); thermal damage to
materials from the use of heated solutions; mechanical damage to the delicate
leads on fine pitched packages from the use of high pressure sprays and jets;
and the durability of markings on packages and the circuit board.

VI. Inspection

The inspection of finished assemblies can have two objectives: (1) the
certification that only defect-free units are reaching market and (2) quality
control of the manufacturing processes. Although both objectives can be met
using lot sampling techniques, reliability specifications will determine the
extent of inspection required for products leaving the factory. Needless to say,
inspection is costly to the company, more so if it is performed manually.
Automated inspection will gradually increase its applications as the associated
equipment grows in sophistication. While most products with very high
reliability requirements will nearly always require 100% inspection, many
inspection procedures can be eliminated through proper process control.
Tighter control of the assembly process and inventory quality will not only
limit the expense of inspection, but also reduce the amount of scrap generated
in production as well as limit possible damage to the assembly caused by
rework and repair procedures.
Because of reliability requirements on a particular product as well as the need for quality control, inspection will never be completely eliminated. Therefore, it is important to identify solder joint defects which are critical to the functionality of the device. Defects which do not impact the performance requirements of a particular product should not be sought (or corrected in rework); such endeavors simply add to the product cost and scrap of the manufacturing process.

An inspection criteria of particularly ambiguous value is the surface quality of the solder in the joint fillet. Smooth, shiny tin-lead solder joints have been preferred to those with rough or "grainy" surfaces. Many product specifications have called for the rework of solder joints with a grainy appearance, based on a cosmetic criterion alone. This is acceptable practice when product marketing requirements place particular emphasis on the solder joint appearance (albeit, few consumers look at the solder joints before purchasing a computer). However, the effect of the surface finish, itself, on solder joint reliability is uncertain. On the other hand, solder surface texture can provide an important indication of contamination in the solder bath (e.g., wave soldering, drag soldering and hot-dipping solder baths). Excessive levels of gold, copper, and iron (from fixturing) impart a grainy appearance to the solder surface; the morphology reflecting the presence of needles and blocky features indicative of the formation of intermetallic compounds between tin and these elements. Of course, larger surface irregularities can signify lead movement during solder solidification. Finally, the physical metallurgy of the newer, non-lead bearing solders being considered in response to pending environmental regulations on the use of lead-containing solders does not promote the formation of smooth, shiny solder joints. In these instances, solder surface texture must be fully assessed for its effect on performance; if the effect is insignificant, then surface appearance should be discarded as an inspection criterion.

Other solder joint defects and a list of their possible root causes appear below:

- **incomplete filling of holes**: poor hole solderability, inadequate amount of filler metal, flux entrapment (which also poses a corrosion problem), low working temperature, and poor hole design (too large or too small a diameter for the lead configuration).
• **Poor fillet formation**: inadequate solderability, low working temperature, and insufficient coverage by the flux.

• **Base metal oxidation/discoloration**: excessive heating of the joint area (which is also indicated by difficult-to-remove flux residues).

• **Cracked solder joints**: part or lead movement during solder solidification, solidification shrinkage of the solder, or residual stresses caused by extreme thermal expansion mismatch between the device, circuit board, and the solder (Recall for through-hole circuit boards that the thermal expansion coefficient in the thickness direction can be nearly an order of magnitude higher than the in-plane value).

Visual inspection has provided the primary means of identifying solder joint defects. Criteria for such inspection are typically dependent upon the particular product being manufactured. General guidelines for the evaluation of common solder joints have been documented (e.g., Refs. 36 and 37). However, the objectivity (and variability) of manual inspection, the intensive labor cost, as well as the further miniaturization of devices and increased density of circuit board assemblies have lead to the development of automated inspection techniques. For example, X-ray laminography can provide a three dimensions view of the solder joint volume, revealing cracks and voids which are not visible at the surface. Laser surface profiling generates a three-dimensional image of the fillet configuration. Solder joints with poor fillet formation (resulting from one of the root causes listed above) are quickly identified for the inspector by the image analysis system. Computer software is becoming sufficiently advanced so as to be able to recognize defective solder joints (imaged by one of the techniques noted above) to automatically count defects on a particular device or product.

Although the non-destructive techniques noted above are the preferred means of inspecting production assemblies, destructive testing in the early prototype development stages or on a lot sampling program of production units, can provide important data with which to assess quality control. Destructive testing includes the metallographic cross sectioning of solder joints to examine the microstructure of the solder and solder/base material
interface as well as mechanical testing to quantify the strength of the solder joint. Shown in Fig. 16 are micrographs exemplifying (a) a surface mount solder joint with thermal cycling induced crack formation and (b) the solder/substrate interface of a joint formed between copper and 95Sn-5Sb solder, aged for 40 days at 205°C (401°F). While microstructural analysis provides the most direct tool with which to assess solder joint integrity, its limitations must always be considered as part of the analysis. Sample preparation techniques must not introduce artifacts (such as cracks) into the section. Solder joints are traditionally some of the most difficult samples to prepare and observe due to the disparity of material hardnesses between substrates and the solder alloy. Secondly, the cross sectional view of the solder joint is through only one plane in a three-dimensional structure. Artifacts may be present in the joint which have simply avoided being seen in a particular section.

Mechanical testing of devices on the circuit board are typically in the form of either a tension test in which the measured force acts perpendicular to the board, or as a shear test in which the force is applied parallel to the board surface. Leadless devices are typically pulled from the circuit board (tension test) while leadless devices receive a shear test. Shear strength data from 1206 chip resistors (dimension in the inset) are shown in Table 5 for the as-soldered condition and after thermal cycling[40].

Once the pertinent defects and suitable inspection techniques have been identified, a program must be established to quantitatively analyze the defects for statistical assessment of the product design or manufacturing process. The guidelines for statistical process control, such as lot sampling protocols and quality conformance envelopes, have been established[41, 42, 43]. However, it is the role of the design and manufacturing engineer to establish reasonable criteria for those statistics, based upon the service requirements of the product (design engineer) and the characteristics of the manufacturing process (manufacturing engineer). Very loose quality limits cause an excessive amount of defective units to reach the customer; subsequent dissatisfaction results in the loss of follow-up sales. On the other hand, overly tight limits on quality drive up the cost of the product due to the generation of excessive scrap and/or the need for labor-intensive inspection and rework operations.
The statistics generated by inspection are used not with the goal of controlling the quality of the product leaving the plant, but also to control the manufacturing process itself. The latter objective is achieved by an in-depth analysis of the defects identified in the inspection operation. First of all, defects indicate a problem with either the materials used in the assembly (e.g., poor solderability of package leads or circuit boards, defective flux, etc.) or an improperly controlled process (inadequate preheat temperature, poor wave configuration, etc.). Once failure analysis has identified the root cause of the defect, corrective measures are implemented, using the defect statistics as an indication of the effectiveness of those remedial actions. The defect statistics are then used, once again, to monitor the materials and processes.

VII Logistics of prototyping soldering processes.

Often, the need arises to alter an existing soldering process or develop an entirely new process to accommodate a new product line or simply to improve the cost effectiveness of an existing manufacturing procedure. The fabrication of a new product or an existing one using new processes and/or new materials is preceded by an interim period of "process development" or "prototyping" activities.

In the case of solder processing, changes can come about through the following factors: (1) solder alloys, (2) fluxes, (3) surface finishes, (4) package configuration (lead shapes) and/or bonding pad geometry, (5) manufacturing processes, and (6) product service requirements. New solder alloys are being developed to meet potential restrictions on the use of lead-bearing solders as well as to accommodate harsher service environments being asked of an increasingly larger number of electronic products (e.g., automobile and chemical process control systems as well as down-hole oil exploration sensors). Alternative solders require different surface finishes on devices and circuit boards. Flux development is being pursued in response to the ban on the use of chlorofluorocarbon cleaning solvents. Evolving package configurations and circuit board design are answering the need for further device miniaturization and increased functionality.

Prototype development is separated into two primary tasks: (1) manufacturing feasibility and (2) service reliability. Manufacturing feasibility pertains to the ability to fabricate defect-free solder joints at a yield
level which is acceptable to the particular product's producibility requirements. Manufacturing feasibility is assessed by identifying defects on prototype units. Defects include solder joint properties (voids, cracks, etc.) as well as damage to the circuit board (or thick film on ceramic) or devices by processing conditions. "Six-sigma" process control is often assessed in the feasibility exercise.

Service reliability describes the capacity for the properly formed solder joint to withstand the product service environments without a loss of functionality (electrical continuity, mechanical integrity, or both). Service reliability is often predicted by accelerated testing designed to exacerbate failure mechanisms known to be potentially active. For example, thermal-mechanical fatigue of surface mount solder joints is a leading cause of failure due to the thermal expansion mismatch between the package and the circuit board[44]. Therefore, thermal cycling of test assemblies is used to predict solder joint reliability. The failure of electronic systems in smart munitions is most likely caused by high impact loading rates. Shock and vibration tests are best suited to duplicate these conditions. Solder joint functionality is typically measured by electrical continuity, strength by mechanical testing, or microstructural changes by metallographic cross sectioning.

It is important to appreciate the following guideline: Manufacturing feasibility must be established prior to the start of the reliability assessment. That is, the reliability study must be performed on properly formed solder joints. If the soldering process is not under control so that defective joints are being used in the reliability study, then the reliability data will most certainly be obscured by premature (or infant mortality) failures of the defective solder joints.

Referring to the six factors noted earlier which pertain to the soldering process, i.e.: (1) solder alloys, (2) fluxes, (3) surface finishes, (4) package configuration (lead shapes) and/or bonding pad geometry, (5) manufacturing processes, and (6) product service requirements, the question is raised: If one of these factors is altered, is a manufacturing feasibility assessment necessary only, or must the reliability tests be performed as well (after feasibility has been clearly demonstrated)? Generally, the use of alternative fluxes (2), surface finishes (3) and manufacturing processes (5) need be assessed solely for feasibility. Each of these factors is critical to the formation of the solder joint. Once an adequate joint configuration has been established (without
damage to the device or substrate), these factors have little bearing on the
service performance of the solder joint. Perhaps the only exception is the flux
and the corrosive potential of its residues if not properly removed in the
cleaning step. On the other hand, solder alloy selection (1), package
configuration (4), and product service requirements (6) will impact the
reliability of the solder joints. The mechanical properties of the particular
solder will affect its susceptibility to thermal mechanical fatigue under
thermal cycling. Reliability is also a function of the geometry of the joint as
determined by the package or lead configuration and bonding pad dimensions.
And, of course, reliability testing must accommodate any changes to the
service requirements of the product.

In summary, prototype development activities are based upon
establishing manufacturing feasibility and service reliability of the solder
joints. The need to perform both a feasibility and reliability analysis will
depend upon those factors being altered in the product or its assembly process.
However, if the individual tasks are properly planned and executed, the
desired data will be obtained at a minimum cost to the development effort.

VIII. Summary

Soldering provides a versatile means for joining several different types
of materials together. Its adaptation to the assembly of electronic components
has supported the high volume manufacturing processes responsible for low
cost, high quality products. More importantly, soldering is clearly a
technology, rather than an art. Properties such as fatigue strength, corrosion
resistance, and wettability can be controlled by the design and manufacturing
engineers, through the proper selection of materials, surface finishes, and
processing parameters.

IX. References


[14] Kovar and Alloy 42, and Alloy 52 are trademarks of Carpenter Technologies.


[34] I. Artaki, A. Jackson, and P. Vianco, unpublished data.
[39] ANSI/IPC-S-815A, "General Requirements for Soldering Electronic Interconnections".

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VIII. **Figure Captions**

**Fig. 1** 60Sn-40Pb on bare Kovar showing (a) non-wetting and (b) de-wetting. *courtesy Sandia National Laboratories*

**Fig. 2** Solder balls formed on a surface mount solder joint. *(courtesy Sandia National Laboratories)*

**Fig. 3** Typical temperature profile for solder paste reflow of surface mount circuit boards.

**Fig. 4** Mechanical properties of the gold-based, precious metal solders.

**Fig. 5** Package and input/output configurations of typical through-hole and surface mount devices.

**Fig. 6** Schematic diagram of the hot-air solder leveling (HASL) process.

**Fig. 7** Solder wetting of the solderable and protective finishes on a substrate material.

**Fig. 8** Solid state intermetallic compound growth of hot dipped 63Sn-37Pb solder on copper. *(courtesy Sandia National Laboratories)*

**Fig. 9** Scanning electron micrographs and cross sectional micrographs of (a) a leadless ceramic chip carrier and (b) a ceramic chip resistor. Also shown is (c) the package configuration and solder joint cross section for a quartz resonator package. *(courtesy Sandia National Laboratories)*

**Fig. 10** (a) Surface mount device and (b) through hole device lead showing the surface to which the solder must wet in each case.

**Fig. 11** Schematic diagram of the screen printing technique for the deposition of solder paste on the circuit board or ceramic substrate.

**Fig. 12** Optical micrograph of the drawbridging phenomena observed with leadless ceramic chip components. *(courtesy Sandia National Laboratories)*

**Fig. 13** The shear strength of 63Sn-37Pb solder, 0.2 mm (0.008 in.) thick copper lap joints as a function of room temperature aging.

**Fig. 14** Wave soldering process of a mixed technology circuit board.

**Fig. 15** Microcircuit silicon chip package assembly.

**Fig. 16** (a) Cracking in a tin-lead solder joint from a surface mount package subjected to thermal cycling. (b) 95Sn-5Sb solder/copper interface showing the intermetallic compound layer growth after thermal aging at 205°C (401°F) for 40 days *(courtesy of Sandia National Laboratories)*.
IX. Table Titles

Table 1 Melting Temperatures of Typical Electronic Solders.
Table 2 Surface Tension of 63Sn-37Pb as a Function of Temperature.
Table 3 Temperature Dependence of 50In-50Sn Wettability (Contact Angle).
Table 4 Solderable and Protective Finishes for Selected Metal Substrate.
Table 5 Shear Strength of 1206 Chip Resistor Solder Joints.
You might need to make a comment in the caption for this figure about T_1 and T_2 in some cases.
Solder wets the "protective" finish

"Protective finish dissolves into advancing solder film

Solder wets the "solderable" coating
Screen (Stencil) Printing
<table>
<thead>
<tr>
<th>Solder Alloy wt. %</th>
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<tr>
<td>52In-48Sn</td>
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<td>118/125</td>
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<td>138/138</td>
<td>(281/281)</td>
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<td>143/163</td>
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<tr>
<td>Temperature °C</td>
<td>Surface Tension dyne/cm</td>
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<td>211</td>
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<td>63±6</td>
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<td>SUBSTRATE</td>
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<td>PROTECTIVE LAYER µm (micro-in.)</td>
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<td>Copper</td>
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<td>Electroplated gold (2) 1.3-2.5 (50-100)</td>
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<td>Electroplated silver 3.8-8.9 (150-350)</td>
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<td>Electroplated copper 3.8-7.6 (150-300)</td>
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<td></td>
<td>Electroplated palladium-nickel 1.3-3.5 (50-150)</td>
<td>• • •</td>
</tr>
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</table>

(1) Thicker layers 2.5-7.8 µm (100-300 micro-in.) permitted for improved coverage; electroless nickel 1.3-3.0 µm (50-120 micro-in.) or 2.5-5.1 µm (100-200 micro-in.) permitted on non-flexible substrates; layer adhesion and solderability require close monitoring.

(2) Thicker layers 2.5-7.5 µm (100-300 micro-in.) permitted for solderable layer protection; however thinner layers are recommended and solder joints should be monitored for embrittlement.

(3) Not contained in MIL-STD-1276D

(4) Trademarks of Carpenter Technologies
<table>
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<th>Test Identification</th>
<th>Shear Strength</th>
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<tr>
<td>As - fabricated</td>
<td>84 ± 8</td>
<td>(19.0 ±1.7)</td>
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<tr>
<td>300 thermal cycles</td>
<td>72 ± 6</td>
<td>(16.2 ±1.3)</td>
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<tr>
<td>100 thermal shock cycles</td>
<td>97 ± 4</td>
<td>(21.9 ±1.0)</td>
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Resistor dimensions: 0.105 x 0.050 x 0.0018 in. (2.67 x 1.27 x 0.457 mm)
termination width: 0.010 in. (0.25 mm)

Thermal cycle: -55°C to 125°C (-67°F to 257°F); 120 min hold period;
6°C/min (11°F/min) ramp.

Thermal Shock: -55°C to 125°C (-67°F to 257°F); 10 min hold period;
liquid-to-liquid transfer

Displacement rate: 10 mm/min (0.41 in/min)