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Complementary GaAs Junction-Gated Heterostructure Field Effect Transistor Technology

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Abstract — The first circuit results for a new GaAs complementary logic technology are presented. The technology allows for independently optimizable p- and n- channel transistors with junction gates. Excellent loaded gate delays of 179 ps at 1.2 V and 319 ps at 0.8 V have been demonstrated at low power supply voltages. A power-delay product of 8.9 fJ was obtained at 0.8 V.

INTRODUCTION

GaAs complementary logic offers the potential for greatly reducing the power consumption of digital integrated circuits while maintaining speeds between those of conventional digital GaAs and Si CMOS. While a number of approaches have been proposed for GaAs complementary logic [1-6], new approaches are worthwhile if they offer the potential for improved speed or reduced power consumption. In the present work, a new GaAs complementary logic technology is described and basic complementary integrated circuits are demonstrated.

TECHNOLOGY DESCRIPTION

This new GaAs complementary logic technology integrates a modulation doped p-channel heterostructure field effect transistor (pHFET) with a junction gate, and a fully ion implanted n-channel JFET [7], as illustrated in Fig. 1. This approach permits the independent optimization of the p- and n-channel devices, including the ability to independently set threshold voltages. A weak link in GaAs complementary technology is the poor performance of the pFET relative to the nFET. Although modulation doping may make sense for pHFETs, this type of design has been little explored because in conjunction with an n-channel epitaxial device, it typically requires common epitaxial layers or a stacked epitaxial design [3]. In our approach, epitaxial doping, material composition, and layer design can all be varied to optimize the p-channel device, since none of these layers will be shared with the n-channel device.

The all GaAs n-channel device was chosen to be a self-aligned n-channel JFET [8,9] fabricated in the GaAs buffer of

Figure 1. Schematic device cross sections of the complementary nJFET and pHFET devices. These devices are independently optimizable.

an epitaxially grown substrate for the following reasons. A JFET allows operation with low gate leakage up to 1 V, which is important in minimizing static power. In addition to the usual benefits of self-aligned processing, the self-aligned refractory JFET also offers important advantages over a conventional JFET as illustrated in Fig. 2. The conventional JFET suffers excess gate capacitance from metal overhang as well as junction broadening. This typically leads to a rf penalty in the conventional JFET compared to MESFETs of the same gate length. The self-aligned JFET with a coincident or slightly undercut junction gate region achieves comparable rf performance to a MESFET of the same gate length with the added advantage of a higher gate turn-on voltage [9].

Figure 2. A comparison of self-aligned (a) and non self-aligned (b) JFETs. The self-aligned JFET results in reduced parasitic gate capacitance.

MASTER

FABRICATION

The junction gate pHFETs are based on a modulation-doped AlGaAs/InGaAs/GaAs strained quantum-well material with 35% AlAs and 18% InAs grown by molecular beam epitaxy. The 100 Å InGaAs quantum well is designed to be thermodynamically stable to remain dislocation free during the high temperature processing. In the present design modulation doping on both sides of the quantum well has been employed. A self-aligned refractory gate process based on tungsten or tungsten silicide gate metal has been used to fabricate the FETs. The 13 mask fabrication sequence is briefly: 1) pHFET active area definition by wet chemical etching, 2) nJFET active area implants (gate, channel, and backside) [9], 3) thermally stable isolation implant [10], 4) tungsten refractory gate deposition, patterning, and reactive ion etch in SF₆:Ar, followed by a wet junction etch, 5) Si implantation for self-aligned n⁺ source and drains, 6) Zn implantation for self-aligned p⁺ source and drains and rapid thermal activation anneal, 7) p-ohmic metal definition and alloy using AuBe, 8) n-ohmic metal definition and alloy using GeAuNiAu, 9-12) 2-level interconnect process with 3 μm lines and 2 μm spaces based on silicon nitride dielectric and TiPtAu interconnects, and 13) passivation. The gate length was 0.7 μm as measured by scanning electron microscopy.

DEVICE RESULTS

DC transfer characteristics are shown for both devices in Figs. 3-6. The nJFET shows a maximum transconductance (g_m) of 230 mS/mm and maximum drain current (I_{DS}) of 200 mS/mm. At a 1.0 V gate and drain bias typical of circuit operation, the g_m and I_{DS} are approximately 170 mS/mm and 90 mA/mm, respectively. Likewise, the pHFET shows a maximum g_m of 43 mS/mm and I_{DS} of 42 mA/mm and operating values of 29 mS/mm and 20 mA/mm. The nJFET

Figure 3. I_{DS} - V_{DS} for a self-aligned 0.7x20 μm nJFET.

Figure 4. I_{DS} - V_G and g_m - V_G at drain biases of 0.5, 1.0, and 1.5 V for a self-aligned 0.7x20 μm nJFET.

Figure 5. I_{DS} - V_{DS} for a self-aligned 0.7x20 μm pHFET.

Figure 6. I_{DS} - V_G and g_m - V_G at drain biases of -0.5, -1.0, and -1.5 V for a self-aligned 0.7x20 μm pHFET.

shows f_t of 19 GHz and $f_{\max}$ of 36 GHz [9]. The pHFET shows an f_t of 3.5 GHz. The subthreshold characteristics for each device is shown in Figs. 7-8. The subthreshold slope is 90 mV/decade for the nFET. The pHFET has not been fully optimized, as it shows soft pinchoff and excessive subthreshold current which contribute to higher than desired static power.

The junction gates turn-on voltages are -1.1 V for the p-channel device and 1.0 V for the n-channel device at 1 mA/mm of gate current. These turn-on voltages are adequate for low static power operation at 1.0 V power supply and below.

CIRCUIT RESULTS

Loaded 31-stage ring oscillators were fabricated using a 2-level metal process and silicon nitride dielectric. The ring oscillators were loaded with 200 μm of wire in 2nd metal which was interdigitated with grounded 1st metal to provide a high capacitance load between each stage. Fan-in and fan-out are both 1 and the devices are 20 μm wide. Maximum speed was obtained at a supply voltage of 1.2 V with gate delays of 179 ps and a power-delay product of 28 fJ. The maximum speed was obtained at a voltage beyond the onset of gate conduction and the power is dominated by gate leakage. A minimum power-delay product of 8.9 fJ was obtained at a power supply of 0.8 V and a speed of 319 ps/stage. The power consumption is largely static power due to soft pinchoff of the p-channel transistor. Under these conditions it is not yet possible to determine the dynamic power.

The modulation-doped pHFET does not offer state of the art performance at this time with g_m only 29 mS/mm at operating circuit bias conditions. Yet these loaded ring oscillators demonstrate excellent speeds at low power supply voltages and even better results are expected with a redesigned pHFET.

CONCLUSION

A promising new GaAs complementary logic technology has been presented and complementary ring oscillators have demonstrated excellent speeds at low power supply voltages.

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Figure 7. I_{DS} - V_G characteristic at drain biases of 0.5, 1.0, and 1.5 V for a self-aligned 0.7x20 μm nFET.

Figure 8. I_{DS} - V_G characteristic at drain biases of -0.5, -1.0, and -1.5 V for a self-aligned 0.7x20 μm pHFET.

Figure 9. Waveform of 31-stage complementary ring oscillator loaded with 200 μm of wire and operating with a power supply of 1.2 V.

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