AJIM

Association for Information and Image Management

1100 Wayne Avenue, Suite 1100
Silver Spring, Maryland 20910
301/587-8202

Centimeter

Inches

MANUFACTURED TO AJIM STANDARDS
BY APPLIED IMAGE, INC.

1 of 1

GA-A21247
UC-406

USER'S MANUAL FOR THE CDC-1 DIGITIZER CONTROLLER

by
J.R. FERRON

Work prepared under
Department of Energy
Contract DE-AC03-89ER51114

GENERAL ATOMICS PROJECT 3466
DATE PUBLISHED: SEPTEMBER 1994

MASTER

REPRODUCTION OF THIS DOCUMENT IS UNLIMITED

User's Manual for the CDC-1 Digitizer Controller*

J.R. FERRON
General Atomics
San Diego, California 92186-9784, U.S.A.

Abstract

A detailed description of how to use the CDC-1 digitizer controller is given. The CDC-1 is used with the CAMAC format digitizer models in the TRAQ series (manufactured by DSP Technology Inc.), the DAD-1 data acquisition daughter board, and the Intel i860-based SuperCard-2 (manufactured by CSP Inc.) to form a high speed data acquisition and real time analysis system. Data can be transferred to the memory on the SuperCard-2 at a rate as high as 40 million 14-bit samples per second. Depending on the model of TRAQ digitizer in use, digitizing rates up to 3.33 MHz are supported (with eight data channels), or, for instance, at a sample rate of 100 kHz, 384 data channels can be acquired.

*This is a report of work sponsored by the U.S. Department of Energy under Contract No. DE-AC03-89ER51114.

Contents

Abstract	iii
1. Introduction	1
2. System Overview	3
3. Installation of the CDC-1 Controller	7
4. Common Combinations of the Configuration Options	13
4.1. A Typical Feedback Control System Application	13
4.2. Continuous Data Acquisition with Low Speed Digitizers	15
4.3. Continuous Data Acquisition with High Speed Digitizers	15
5. Front Panel Connections	17
6. An Overview of CDC-1 Operation	19
7. Details of the Configuration Options	21
7.1. Switches	21
7.2. Jumpers	22
7.3. Jumpers that Set Options for the Start Trigger Signal	23
8. Acknowledgments	25

Figures

1. Block diagram of the data bus connections between the digitizers, the CDC-1 controller, and the DAD-1 data acquisition daughter board	4
2. Layout of the 40-wire cables on the CDC-1 circuit board	8
3. Installation of digitizers and the CDC-1 controller in the CAMAC crate	9
4. Connections to the back of the digitizers as viewed from above the CAMAC crate	10
5. Labeling scheme and correct digitizer address settings for an example with two digitizer modules on each of the eight data buses	11

Tables

1. Correspondence between the CDC-1 connectors and data bus name	5
2. Summary of the TRAQ family digitizers supported by the digitizer interface module	5

Tables (Continued)

3. Proper delay count switch and jumper settings for the TRAQ family digitizers	13
4. Switch and jumper settings for a feedback control application	14
5. Switch and jumper settings for a data acquisition application with low speed digitizers	15
6. Switch and jumper settings for a data acquisition application with high speed digitizers	16

1. Introduction

This document describes how to use the CDC-1 digitizer controller as part of a high speed data acquisition and processing system. In addition to the digitizer controller, this system includes the following three components.

- CAMAC format digitizer modules from the TRAQ family manufactured by DSP Technology Inc.
- The General Atomics DAD-1 data acquisition daughter board for the SuperCard-2.
- The SuperCard-2 VME format processor board manufactured by CSP Inc.

The CDC-1 controller serves as the interface between digitizers in the TRAQ family and the DAD-1 daughter board. Details of the CDC-1 circuit operation are given in *Circuit Operation Manual for the CDC-1 Digitizer Controller*.

The DAD-1 daughter board is capable of serving as the interface between the SuperCard-2 and a variety of sources of digital data. For the details on the use of this board the reader is referred to *User's Manual for the DAD-1 Data Acquisition Daughter Board for the SuperCard-2*.

The TRAQ digitizers and the SuperCard-2 are described in literature provided by the manufacturers of those products.

Sections 2, 3, 4, and 5 provide the essential information for setting up and using the CDC-1 controller. Section 2 provides a description of the complete acquisition and processing system and describes the organization of the data transfer between the CDC-1 and the DAD-1. This section will be useful for programmers and other users who need to understand the mapping between the digitizer channel numbers and the location of data in the SuperCard-2 memory. Section 3 describes the installation procedure for the CDC-1 and Sec. 4 gives several commonly used combinations of the CDC-1 configuration options, one of which should be suitable to copy for most applications. Section 5 describes each of the front panel connectors.

The last sections (Secs. 6 and 7) in this manual give a detailed description of the configuration options and some background on operation of the CDC-1 controller which should allow the reader to customize the CDC-1 configuration. An understanding of these sections will usually not be necessary in order to use the CDC-1.

2. System Overview

Figure 1 illustrates the data connections between the digitizers and the DAD-1 daughter board. Data from the digitizers are transferred to the first-in, first-out (FIFO) memory on the DAD-1 daughter board through line drivers (indicated by the triangle symbols) under the control of the CDC-1 digitizer controller. From there the data are transferred to memory on the SuperCard-2; this process is described in the DAD-1 user's manual. The i860 processor on the SuperCard-2 performs whatever data manipulation is required, and can provide output to the host processor or to other input or output modules that reside on the VME bus.

The TRAQ family digitizers are used differently here than in a CAMAC-based system provided by DSP Technology Inc. A complete CAMAC-based TRAQ system as normally provided by DSP Technology Inc. includes a controller module, one or more memory modules and one or more digitizer modules, all manufactured by DSP Technology. The controller is responsible for copying digitized data from the digitizer over a digitizer bus and then transferring the data to the memory module over a separate memory bus.

In the system of Fig. 1, only the digitizer module is used and the CDC-1 controller is used to control the data transfer from one or more digitizers over the digitizer bus to the DAD-1 data acquisition daughter board for the SuperCard-2. The CDC-1 is a very simple digitizer controller, with a rather fixed function. It is constructed in a CAMAC format module, but it is not programmable and there is no CAMAC interface included. The only CAMAC bus connections used are power and ground. There are some switches on the board that can be set in order to choose among a few different modes of operation. Typically, the switch settings would be fixed for a particular application and would not be changed often.

Figure 1 illustrates the structure of the data buses connecting the digitizers, the CDC-1 controller and the DAD-1 daughter board. There are eight separate data buses that connect the digitizers to the data acquisition system. When data is transferred from the digitizers to the DAD-1 daughter board, eight data values are transferred in parallel. There can be multiple digitizer modules connected to each of the eight data buses.

The data buses are labeled in Fig. 1 according to the naming scheme used by the DAD-1 daughter board. In this scheme, there are two groups of four data buses, labeled group 1 and 2. Within each group the four data buses are labeled A, B, C, D. On the CDC-1 circuit board there are eight 40-pin connectors, one for each of the eight data buses. The connectors are labeled J1 through J8. The correspondence between these connectors and the data bus labels is shown in Fig. 1 and is summarized in Table 1.

FIG. 1. Block diagram of the data bus connections between the digitizers, the CDC-1 controller, and the DAD-1 data acquisition daughter board.

The CDC-1 is compatible with TRAQ family digitizers operating at sampling rates up to 3.33 MHz. Table 2 contains a summary of the maximum number of channels and the maximum sampling rate as a function of TRAQ family digitizer model number. The

Table 1
Correspondence Between the CDC-1 Connectors
and Data Bus Name

40-pin Connector Label	Data Bus Label
J1	1A
J2	1B
J3	1C
J4	1D
J5	2A
J6	2B
J7	2C
J8	2D

shortest time interval between successive sample triggers allowed by the CDC-1 controller is $0.2 \times N + 0.1 \mu\text{sec}$ where N is the number of digitizer channels connected to each data bus. For instance, the maximum possible digitizing rate is obtained with one channel attached to each data bus (for a total of eight channels on the eight data buses on the system), so that the time interval between the sample triggers must be greater than $0.2 \times 1 + 0.1 = 0.3 \mu\text{sec}$.

Table 2
Summary of the TRAQ Family Digitizers
Supported by the Digitizer Interface Module

TRAQ Model Number	Maximum Sample Rate	Maximum Number of Channels at the Maximum Sample Rate
2812	100 kHz*	384
2814	100 kHz	384
2824	2 MHz	16
2825	500 kHz	64
2860	1 MHz	32

*Nominally the model 2812 digitizer has a maximum sample rate of 100 kHz. Depending on the ECO level of the digitizer module, a slightly higher rate, up to 140 kHz in some cases, is possible. ECO level 1001 will operate at 140 kHz. ECO level 1009 will operate at 116 kHz.

Each time a sample trigger is received by the CDC-1 controller, one sample of data from each of the digitizer channels is transferred to the DAD-1 daughter board. The sample trigger can come either from the front panel input (described in Sec. 5) or from the DAD-1 daughter board. A transition from 0 to 1 of the CSRSAMPDC bit in the CSR2 register of the DAD-1 daughter board generates a sample trigger for the CDC-1 controller.

The logic circuits in the CDC-1 controller and in the digitizer modules connected to it are initialized when the CAMAC crate power is turned on. Also, when the CSREXTRESET bit in the DAD-1 CSR2 register is set to 1 the CDC-1 controller and the digitizer modules are held at this initial state (the modules are "reset"). When the CSREXTRESET bit is 1 the CDC-1 and the digitizers are prevented from acquiring data.

3. Installation of the CDC-1 Controller

Before installing the digitizers in the CAMAC crate, ensure that the proper terminating resistors are installed. The last digitizer on each of the eight digitizer buses (i.e., only one digitizer per bus) must have the jumper installed that connects a terminating resistor to ground (approximately 120 Ω) on the three signals called "Done," "CVT," and "DACPT." Refer to the DSP Technology Inc. Manual for the digitizers to find the locations of these jumpers.

To install the CDC-1 controller do the following.

1. Set the switch and jumper options on the CDC-1 circuit board. Refer to Sec. 4 to choose a configuration of the switch and jumper options.
2. Connect the eight 40-wire cables provided with the CDC-1 controller to connectors J1 through J8 on the CDC-1 circuit board. Note that the connectors are not located in exact numerical order on the circuit board. The cables that attach to the lower row of connectors (J1, J2, J3, J4) must be folded twice in 90 degree bends so that the cables can pass through the opening at the top of the CDC-1 back panel. The eight cables pass through the back of the CDC-1 in a stack with the cable connecting to J1 closest to the circuit board, followed by the cables connecting to J4, J3, J2, J5, J8, J7, and J6. The proper installation of these eight cables on the CDC-1 circuit board is illustrated in the photograph in Fig. 2.
3. Install the CDC-1 controller in the CAMAC crate. The controller module can be in any slot in the crate, but should be located on the right-hand-side of the digitizers. This is illustrated in the photograph in Fig. 3.
4. Connect the 40-wire cables to the connectors on the back of the digitizers. This is shown in Fig. 4. In order to have the digitizers located in numerical order in the CAMAC crate (as illustrated in the example in Fig. 5), the cables must cross each other in several places.
5. Connect the two, high density 100-wire cables and the single high density 40-wire cable between the CDC-1 digitizer controller and the DAD-1 daughter board, as illustrated in Fig. 3. The top 100-pin connector on the CDC-1 must be connected to the top 100-pin connector on the DAD-1. The middle 40-pin connectors must be connected, and the bottom 100-pin connector on the CDC-1 must be connected to the bottom 100-pin connector on the DAD-1.

FIG. 2. Layout of the 40-wire cables on the CDC-1 circuit board (A, digitizers; B, CDC-1; C, SuperCard-2; D, DAD-1; E, 40-wire cables, F, high density ribbon cables).

6. Set the front panel address switches on the digitizers. One module on each of the eight data buses (i.e., one of the digitizer modules connected to each of the 40-wire cables) should have its address set to zero, with the other digitizer modules on a given data bus set to addresses in increasing sequential order, 1 through the number of digitizer modules on each bus minus 1. As an example, Fig. 5 illustrates the digitizer addressing, channel

FIG. 3. Installation of digitizers and the CDC-1 controller in the CAMAC crate (A, digitizers; B, CDC-1).

numbers, and correspondence to the eight data buses for a case with two digitizers on each data bus, each with eight channels.

FIG. 4. Connections to the back of the digitizers as viewed from above the CAMAC crate.

FIG. 5. Labeling scheme and correct digitizer address settings for an example with two digitizer modules on each of the eight data buses.

4. Common Combinations of the Configuration Options

There are switches and jumpers on the CDC-1 circuit board that must be set properly for the data acquisition system application. There are several standard configurations for the CDC-1 controller that satisfy the most common applications. These are detailed in this section.

The switches and jumpers on the CDC-1 controller, when used with two optional external input signals (last address and start wait), can be used for a certain amount of customization of the controller function. These options are discussed in Sec. 7. Neither of the two optional external inputs is used for the setup combinations described in this section.

4.1. A Typical Feedback Control System Application

To use this configuration, set the switches and jumpers as indicated in Tables 3 and 4. This configuration has the following characteristics (familiarity with the content of the DAD-1 user's manual will help in understanding this list).

Table 3
Proper Delay Count Switch and Jumper^a Settings for the TRAQ Family Digitizers

TRAQ Model No.	S2 Value (hex)	S1 Value (hex)	E28 to E29	E27 to E28
2812 ^b	2	9	open	connected
2812 ^c	c	f	connected	open
2812 ^d	f	f	connected	open
2814	not yet determined	not yet determined	connected	open
2824	0	c	connected	open
2825	not yet determined	not yet determined	connected	open
2860	not yet determined	not yet determined	connected	open

^aThe E27, E28, E29 jumper connections are not available on CDC-1 Revision P1. In this case, set only the switches S1 and S2.

^bFor sample frequencies up to 100 kHz, the normal specification for model 2812.

^cFor sample frequencies up to 140 kHz with the digitizer modules with the proper ECO level (older modules, e.g., ECO 1001).

^dFor sample frequencies up to 116 kHz. This should be appropriate for the more recent ECO levels (e.g., ECO 1009).

Table 4
Switch and Jumper Settings for a Feedback Control Application

Switch/Jumper	Setting
S1: delay count lower half	from Table 3
S2: delay count upper half	from Table 3
S3: last address lower half	f (hex)
S4: last address upper half	f (hex)
E3 to E4	open
E7 to E8	open
E8 to E9	connected
E10 to E11	connected
E12 to E13	connected
E22 to E23	connected
E23 to E24	open
E27, E28, E29	from Table 3

1. Data from the digitizers is provided in bursts to the SuperCard-2 processor. Each burst contains one sample from each of the digitizer channels, and one burst of data is transmitted each time a sample trigger is received.
2. The time interval between successive sample triggers must be larger than $0.2 \times N + 0.4 \mu\text{sec}$ where N is the number of digitizer channels connected to each data bus. For instance, if there are 16 channels attached to each data bus (for a total of 128 channels on the eight data buses on the system), then the time interval between the sample triggers must be greater than $0.2 \times 16 + 0.4 = 3.6 \mu\text{sec}$.
3. The start trigger signal is used to start the DMA transfer of data to the SuperCard-2 (i.e., the DAD-1 daughter board is programmed for start mode 1).
4. The combination of an inactive start trigger signal and an empty FIFO memory is used to stop the DMA data transfer to the SuperCard-2 (i.e., stop mode 0 is used by the DAD-1 daughter board).
5. The digitizer "data available" handshake signal is used by the CDC-1 controller to determine how many digitizer channels are present. The "last address" switch is set to a high value and its function is not used.

4.2. Continuous Data Acquisition with Low Speed Digitizers

This application differs little from the case described in Subsec. 4.1. The switch and jumper settings are given in Tables 3 and 5. Here it is assumed that there is a continuous external sample trigger and that one sample from each digitizer channel is provided to the DAD-1 daughter board after each sample trigger. The interval between sample triggers satisfies the same restriction as is given in Subsec. 4.1.

Table 5
Switch and Jumper Settings for a Data Acquisition Application
with Low Speed Digitizers

Switch/Jumper	Setting
S1: delay count lower half	from Table 3
S2: delay count upper half	from Table 3
S3: last address lower half	f (hex)
S4: last address upper half	f (hex)
E3 to E4	open
E7 to E8	open
E8 to E9	connected
E10 to E11	connected
E12 to E13	connected
E22 to E23	connected
E23 to E24	open
E27, E28, E29	from Table 3

4.3. Continuous Data Acquisition with High Speed Digitizers

If the interval between sample triggers is short then the start trigger signal must be changed to its "short" mode of operation. This becomes necessary if the time interval between sample triggers is less than that described in Subsec. 4.1. For example, if there are two channels attached to each data bus (for a total of 16 channels on the eight data buses on the system), and the time interval between sample triggers is $0.5 \mu\text{sec}$ (2 MHz sample frequency) then the sample interval is larger than the minimum value allowed for the CDC-1 (specified in Sec. 2) but shorter than the value given in Subsec. 4.1 so the short mode of start trigger operation must be used.

In addition, when the sample trigger interval is shorter than that specified in Subsec. 4.1, the data available signal from the digitizers cannot be used to automatically determine the number of digitizer channels. The maximum digitizer address must be set explicitly with the "last address" switches. For this purpose, the address starts at 0 so the last address switch must be set to $N - 1$ where N is the number of digitizer channels on one of the eight buses.

The switch and jumper settings for this case are given in Tables 3 and 6.

Table 6
Switch and Jumper Settings for a Data Acquisition Application
with High Speed Digitizers
*Here N is the number of digitizer channels
connected to one of the eight data bases*

Switch/Jumper	Setting
S1: delay count lower half	from Table 3
S2: delay count upper half	from Table 3
S3, S4: last address	$N - 1$ (hex)
E3 to E4	open
E7 to E8	open
E8 to E9	connected
E10 to E11	connected
E12 to E13	open
E22 to E23	connected
E23 to E24	open
E27, E28, E29	from Table 3

5. Front Panel Connections

There are six coaxial LEMO connectors and three ribbon cable connectors on the front panel of the CDC-1 controller. These connections are described here. There is also a pilot light that indicates the presence of CAMAC crate power.

The three ribbon cable connectors are the interface to the DAD-1 data acquisition daughter board. The ribbon cables are attached as described in Sec. 3.

The six LEMO connectors are all inputs, all require TTL level signals, and the input load is either a high impedance or a standard TTL gate input. All inputs are terminated with a 10 k Ω resistor connected to the 5 V power supply. The functions are the following.

start wait: This is an optional input used in custom configurations to control the behavior of the start trigger signal. See Sec. 7 for more details. Normally there would be nothing connected to this input.

last address: This is an optional input used in custom configurations to activate or deactivate the function of the "last address" comparison. See Sec. 7 for more details. Normally there would be nothing connected to this input.

sample trigger: A rising edge on this input causes the digitizers to be triggered and the resulting digital data to be transferred to the DAD-1 daughter board.

clock reset: A rising edge on this input causes the value in the clock counter on the DAD-1 daughter board to be set to zero.

1 MHz clock: This signal is transmitted to the DAD-1 daughter board where it is used to increment the value of the clock counter. As detailed in the DAD-1 manual, this clock signal must be present before the value of the clock counter can be recorded. Despite the name of this signal, it is not restricted to 1 MHz. The maximum frequency is specified in the DAD-1 manual.

counter latch: This is an optional input that is provided for use in custom configurations. If the proper CDC-1 circuit board jumper is set (see Sec. 7), a TTL low level on this input causes the value of the DAD-1 clock counter to be recorded in the DAD-1 TR register (i.e., this input should be normally at a TTL high level). If the CDC-1 jumper is connected to deactivate this input, then the DAD-1 clock counter is recorded in the DAD-1 TR register at the beginning of each digitizer convert cycle.

6. An Overview of CDC-1 Operation

The basic job of the digitizer controller circuit is to command the digitizers to start an analog to digital conversion at the appropriate time, wait for the conversion to complete, and then to command the digitizers to transmit the digital data to the DAD-1 daughter board. A burst of data consisting of one value from each of the digitizer channels is transmitted to the daughter board each time a sample trigger is received.

The digitizer interface circuit executes a complete cycle every time a "sample trigger" is received. An outline of a cycle is as follows.

1. The sample trigger is received, causing a cycle to start. A sample trigger can come from either the front panel input or from a signal transmitted by the DAD-1 daughter board when the CSRSAMPDC bit in the DAD-1 CSR2 register is set.
2. The digitizers are given a "convert" pulse. This causes the digitizer to sample the analog input signal and convert it to digital form. This conversion process takes a fixed time, typically between 0.5 and 10 μ sec, that depends on the type of digitizer.
3. The digitizer interface circuit executes a "wait" cycle. During this cycle, the interface circuit simply waits a fixed time while the analog to digital conversion is completed. The duration of this wait period is set by a switch and a jumper to a value between 0.13 and 17.2 μ sec.
4. After the wait cycle ends the interface circuit begins a "read" cycle, during which the data is transferred from the digitizers to the DAD-1 daughter board.
5. At the beginning of the read cycle, the DAD-1 daughter board is optionally triggered using the "start trigger" to indicate that a new data acquisition cycle is starting. There are a couple of possible different modes of operation for the start trigger chosen by setting jumpers and/or switches.
6. Each set of digitizer channels is addressed in turn, beginning at address 0 and counting up, causing their data to be gated out onto the data bus.
7. Each time new data are placed on the data bus, the DAD-1 daughter board is triggered using the "data accept trigger" to signal it to acquire the new data.
8. When the digitizer address reaches the preset value given by the "last address" switches or the "data available" signal provided by the digitizers becomes false, indicating that there are no more digitizer channels to be addressed, the start trigger signal is (optionally) negated to indicate to the DAD-1 daughter board that a complete set of digitized data has been acquired, and the "done" line is activated to indicate to the digitizers that all of the data have been acquired.

9. This is the end of the read cycle and the end of a complete controller cycle.

A wait cycle and a read cycle can be executed simultaneously. This allows a new analog to digital conversion to be started while the read of the data from the previous conversion is still in progress.

The time delay between the sample trigger and the moment that all of the digitizer data has been transferred to the DAD-1 daughter board is the duration of the wait cycle plus $0.2 \times N + 0.2 \mu\text{sec}$ where N is the number of digitizer channels on each of the eight data buses. For instance, if there are 16 digitizer channels on each data bus (as illustrated in Fig. 5), and the model 2812 digitizer is in use (which requires in some ECO levels a $7 \mu\text{sec}$ wait cycle), the delay is $7 + 16 \times 0.2 + 0.2 = 10.4 \mu\text{sec}$.

7. Details of the Configuration Options

The configuration options of the CDC-1 fall into three categories.

1. The duration of the wait cycle must be set to match the type of TRAQ family digitizer that is in use.
2. The "last address," equivalent to the largest channel number, of the digitizers to be accessed can be set specifically or the hardware can automatically determine the address of the last digitizer channel using the "data available" signal provided by the digitizers.
3. The behavior of the start trigger signal can be adjusted to the application.

The remainder of this section lists the configuration jumpers and switches. The provisions of the CDC-1 for application customization (i.e., applications other than those described in Sec. 4) are described here briefly, but in order to implement a custom application the details of the circuit operation must be considered (see *Circuit Operation Manual for the CDC-1 Digitizer Controller*).

7.1. Switches

S1, S2 The nine-bit "delay count" must be set with switches S1 (least significant four bits) and S2 (next most significant four bits) and jumpers E27 to E29 (on revision level P1 the counter is eight bits and E27 to E29 do not exist). The jumpers set the most significant bit. The two switches and jumpers specify a hexadecimal value equal to the number of cycles of a 30 MHz clock for the delay between the sample trigger and the beginning of the read cycle, that is, the duration of the wait cycle. The required value is a function of the digitizer model number. Table 3 summarizes the proper settings for S1 and S2 and the jumpers as a function of TRAQ digitizer model number. In general, the nine-bit delay count should be equal to $30 \times t - 3$ where t is the A/D conversion time in microseconds.

S3, S4 The value of the eight-bit "last address" is set using switches S3 (lower four bits) and S4 (upper four bits). During a read cycle, the digitizer channel address is incremented from 0 until either the channel address is equal to the "last address" or the DAV control signal from the digitizers indicates that the current address does not correspond to an existing digitizer channel.

For the highest speed digitizers (such as the model 2824) the last address must be set equal to the address of the highest numbered digitizer channel. The data available signal cannot be used to end a data acquisition cycle with the highest speed digitizers. For slower digitizers, use of the last address function is optional. If it is not used, set the switches to the hex value FF. Specifics are given in Sec. 4. The range of sample intervals for which the last address comparison must be used is discussed in Subsec. 4.3.

In another application, if a digitizer module contains multiple channels, and it is not desired to address unused channels in the digitizer (a process that wastes time and data storage memory), the last address can be set to the address of the last channel in use.

Finally, the last address function can be turned on and off with an external signal connected to the last address front panel connector. By toggling this signal, the last channel addressed can be changed between the last valid channel (as indicated by the digitizer "data available" signal) and the value given by the "last address" switch setting.

Note that for the purposes of setting this switch, the digitizer channels are numbered starting at 0.

7.2. Jumpers

E7-E9 Jumper E7, E8, E9 must be set to enable or disable the external control of the last address comparison operation. Set the jumper to E8,E9 to have the last address comparison always enabled. Set the jumper to E8,E7 to have the last address comparison under the control of the last address front panel input signal. If the jumper is set to E8, E7 and there is no external input then the last address comparison is always disabled. A TTL high level on the external input disables the last address comparison, while a low level enables the comparison.

E22-E24 The source of the signal that causes the content of the DAD-1 daughter board clock counter to be latched can be set with jumper E22, E23, E24. When set to E22, E23 the "counter latch" signal, that causes the clock counter to be latched, is generated each time a new digitizer conversion cycle is started. When the jumper is set to E23, E24, the counter latch signal is under the control of a front panel input signal counter latch.

E27-E29 These jumpers set the most significant bit of the wait cycle delay counter. Connect E28 to E29 to set the most significant bit to 0. Connect E27 to E28 to set the most significant bit to 1.

For the explanation of the remainder of the jumpers, see Subsec. 7.3.

7.3. Jumpers that Set Options for the Start Trigger Signal

The start trigger signal, generated by the digitizer controller circuit, can be used in several ways by the DAD-1 daughter board.

1. Start trigger, when low, causes the value of the P mask counter, used by the DAD-1 daughter board input multiplexer circuit, to be loaded with its initial value (which is equal to the value programmed into the DAD-1 CSR register). When the start trigger is high, this counter is decremented on each cycle of the data accept trigger, that is, after each data transfer.
2. The low to high transition of the start trigger can trigger the start of a DMA write cycle by the DAD-1 daughter board, if the daughter board start mode is 1.

If the daughter board stop mode is set to 0, the falling edge of the start trigger signal indicates that the DMA cycle in progress should end when the FIFO memory is empty.

The way the DAD-1 daughter board uses the start trigger in a given application affects how the digitizer interface circuit jumpers should be set.

E12-E13 If the start trigger is used to start and stop a DMA cycle, then the "normal" length of the start trigger pulse must be used. For this, insert jumper E12, E13.

If high speed digitizers are in use, such as model 2824 operating at 2 MHz, then a "short" pulse of the start trigger must be used (see Subsec. 4.3). In this case the start trigger cannot be used to start and stop DMA cycles, it can only be used to cause the P mask counter to be loaded. In this application remove jumper E12, E13.

E3-E4 In some applications, it may be desirable to control the value of the start trigger externally. For instance, it may be desirable to hold the P mask counter at its initial value for awhile, and then let it count down to 0. This could have the effect of allowing all eight of the DAD-1 daughter board data buses to be in use initially, followed by a hardware controlled transition to a situation where some of the data buses are ignored by the DAD-1 daughter board input circuits.

To allow this external control, insert jumper E3, E4. With this jumper inserted, when the **start wait** external input is low, the start trigger is always low. The high state of the **start wait** external input can cause one of two behaviors.

E10-E11 With jumper E10,E11 inserted, when the **start wait** external input is high, the start trigger is pulsed in the normal manner during each read cycle.

E10-E11 With jumper E10,E11 removed, when the **start wait** external input is high, the start trigger is held high. This can cause a transition from all of the eight data buses in use always to only a specified set in use always.

8. Acknowledgments

The author would like to acknowledge the very valuable assistance in this project of J. Broesch, E. Brown, G. Campbell, J. Land, E. McKee, A. Nerem, G. Phelps, C. Parker, J. Phillips, and T. Smith.

This is a report of work sponsored by the U.S. Department of Energy under Contract No. DE-AC03-89ER51114.

**DATE
FILMED**

11 / 9 / 94

END