Silicon-FilmTM Photovoltaic Manufacturing Technology

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Introduction

Project Overview

The goal of AstroPower's PVMaT-2A project is to develop an advanced, low-cost manufacturing process for a new utility-scale, flat-plate module. This process starts with the production of continuous sheets of thin-film, polycrystalline silicon using the Silicon-Film™ process. Sheets are cut into wafers that are nominally 15 cm on a side. 56 of these wafers are then fabricated into solar cells which are strung together in a 170 watt module. Twelve of these modules form a 2 kW array. The module, array, and solar cells have features described in Table 1.

Table 1. Silicon-Film™ Large Area PVMaT Products

Solar Cell Size	225	cm ²
Solar Cell Power	3.15	watts
Module Size	1.4	m ²
Module Power	170	watts
Array Power	2041	watts

The program has three main components:

1. Development of a Silicon-Film™ wafer machine that is capable of manufacturing wafers that are 225 cm² in size at a rate of 3.0 MW/yr with a total product cost reduction of 70%.
2. Development of an advanced solar cell manufacturing process that is capable of turning the Silicon-Film™ wafer into a 3.15 watt solar cell.
3. Development of an advanced module design based on these large area silicon solar cells with an average power of 170 watts for 56 solar cells and 113 watts for 36 solar cells.

Silicon-Film™ Technology

The Silicon-Film™ Process is a method for fabricating silicon wafers by the production of continuous sheets of thin film silicon on a low cost substrate which are then cut to size. Because these sheets are produced at the desired thickness, ingot sawing and associated mounting and cleaning steps are eliminated resulting in a significant reduction in cost. For the Silicon-Film™ Process, silicon cost is determined by the material quality, silicon thickness, wafer breakage, and kerf loss during sawing. In developing a low cost process, the focus is on limiting the consumption of high quality silicon, reducing sawing steps, and utilizing a high yield continuous manufacturing technology. The continuous manufacturing process produces the volume to reduce the per wafer cost of capital equipment and labor while improving process control.

PVMaT Project Goals

Development of a Silicon-Film™ manufacturing technology requires the successful achievement of the following three objectives leading to the milestones listed in Table 2:

- design, construction, and demonstration of a production machine that generates sheets of Silicon-Film™ at a wafer production rate capable of 3.0 MW/yr.
- development of a low cost fabrication process that fabricates 3.15 watt solar cells that are 15 cm by 15 cm.
- development of a large area module production line that produces both 113 Wp, 0.9 m² modules and 170 Wp, 1.4 m² modules.

Table 2. Specific PVMaT Goals for Phase I through Phase III

	Phase I	Phase II	Phase III
Wafer Machine			
Production Rate	400 kW/yr	1.3 MW/yr	3.0 MW/yr
Material Use Efficiency	75%	85%	90%
Solar Cell Size*	a) 10 cm x 10 cm b) 15 cm x 15 cm	b) 15 cm x 15 cm c) 15 cm x 45 cm	b) 15 cm x 15 cm c) 15 cm x 45 cm
Solar Cell Power	a) 1.1 watts	b) 2.25 watts 2.5 watts	b) 2.8 watts 3.15 watts
Module Power	-----	b) 72 watts 84 watts	b) 98 watts 170 watts

* a) AP-100, b) AP-225, c) AP-675

The two solar cell and module powers shown in Table 2 for Phase II and Phase III indicate improvements in performance targeted for those phases. For example, a 2.8 watt cell is the target for the first six months of Phase III, whereas a 3.15 watt cell is the target for the last six months of Phase III.

Key Results

During the first six months of Phase III, AstroPower made significant advances in developing the prototype machines and processes toward reliable manufacturing counterparts. Our key achievements in the first half of Phase III are detailed in the sections that follow.

Wafer Machine Performance Benchmarks

Wafer machine development in the first half of Phase III was focused on improving machine reliability and increasing wafer throughput while increasing material use efficiency and material quality (in terms of diffusion length). Our efforts were successful in improving machine reliability and increasing wafer throughput, while material use efficiency remained relatively unchanged.

By performing several 14+ hour production runs we were able to identify component failure modes which only occurred under extended operation. Component design was then modified to eliminate the identified failure modes. As a result, visual and mechanical yield during 14+ hours of production was improved from 64% to 82%. During the typical 8 hour production runs, material use efficiency (MUE) was 84%; plans for improving MUE to over 90% will be discussed in detail.

Through adjustments in thermal profile and heat extraction, a significant increase in production rate capability was achieved. By the end of the sixth month of Phase III, we had reached a production rate capable of 3.7 MW/y; this is 106% over the 1.8 MW/yr representative of the beginning of Phase III, and 23% over the 3.0 MW/yr goal for Phase III. The thermal changes required to support this production rate also led to an improvement in material quality as measured by diffusion length. At the end of Phase II, median diffusion lengths of unhydrogenated material hovered at approximately 18 μm . Median diffusion lengths of similarly doped, unhydrogenated Silicon-Film™ material grown at the 3.7 MW/yr production capacity are currently 27 μm . As further optimization of thermal profile and heat extraction is achieved, we expect diffusion lengths to continue to improve.

Solar Cell Efficiency Achievements

Solar cell fabrication processes have been developed along two parallel paths: (i) a baseline process, and (ii) a champion cell process. The objective of the baseline process is to build the lowest cost process capable of producing average lots of 2.5 watt or better solar cells. The objective of the champion process is to capture the full potential of the material leading to a 3.15 watt solar cell.

To date, Phase III baseline process efforts have focused on incorporating a gettering diffusion, reducing grid shading, and increasing performance and throughput of the anti-reflection coating deposition process. The best baseline cell we have measured during Phase III was a 1.9 watt, 240

cm² device. We expect to achieve the 2.5 watt baseline goal by improvements in doping, diffusion length, and fill factor.

Phase III advanced processing efforts have focused on improving device performance through enhancement processes such as forming gas anneal, hydrogenation (RF or ion-implanted hydrogen), and gettering. Although gains from individual processes have been achieved, these enhancement processes have not yet been successfully integrated into a high performance process. At this time, the best solar cell fabricated had a open-circuit voltage of 560 mV and a short-circuit current of 26.3 mA/cm². Efforts to optimize and successfully integrate the individual processes are continuing.

Module Assembly Achievements

Efforts in module line assembly have focused on investigating automated process steps and accommodating the larger 56 cell module due for fabrication at the end of Phase III. Automated tabbing of front and back contacts and automated module transfer to lay-up are being investigated; details on the plans and status are provided. The width dimension of the 56 AP-225 cell module is the same as the width dimension of our current laminator. As a result, it was necessary to perform feasibility tests to ensure that the 56 cell module could be laminated with our present equipment; these tests were successfully completed.

Silicon-Film™ Process

Process Capability

The capability of the Silicon-Film™ Process is described in this section. The wafer formation process is briefly presented followed by calculations describing the areal generation rate and material use efficiency planned and achieved during the first half of Phase III. Finally, a discussion of the details of yield and machine operation are presented.

Wafer Formation Process

A setter transports the raw materials through the active layer growth process. The setters are transported in a manner that permits the continuous application of the raw materials and the continuous growth of the active layer; there is only one beginning and one end of the sheet as established by the beginning and the end of the production run. The sheet is cut to the desired length as it exits the machine.

The growth of the active layer is accomplished in a system purged with an inert gas to reduce the effects of oxidation. The linear sheet speed, gaseous ambient, and the axial and transverse thermal profiles of the machine are fundamental parameters that are critical to achieving the desired sheet properties.

There are two key performance benchmarks in wafer machine development: wafer machine rate and material use efficiency. The Phase III goal for these benchmarks is to demonstrate a wafer machine operating rate capable of producing 3.0 MW per year and to demonstrate a material use efficiency of 90%. In the following paragraphs, we describe how these benchmarks are measured, progress towards these goals, and our plans to meet the targeted goals.

Wafer Machine Rate Calculation

The machine rate goal for Phase III is to demonstrate an areal generation rate capable of producing 3.0 MW/year. Figure 1 illustrates the geometry for a Silicon-Film™ sheet on the setter. Production rate is the product of the following set of factors: the areal machine growth rate, M_r , in m^2/hr , the number of operating hours per year, N_o , and the solar cell efficiency, Eff .

Figure 1. Silicon-Film™ sheet geometry

The equation for the definition of the production rate is:

$$PR = M_r * N_o * Eff * 10^{-5},$$

where

PR	=	production rate, MW/year
M_r	=	machine rate m^2/hr
N_o	=	number of production hours per year
Eff	=	resultant solar cell efficiency, %.

Given the highest efficiency measured by NREL on a solar cell fabricated from representative material, 8000 production hours per year (based on continuous operation of the machine), and the current baseline areal generation rate (M_r), we calculate that our current machine rate is capable of a production rate of 3.7 MW/yr. The areal generation rate is based on finished wafer area generated per hour as shown in Figure 2.

Material Use Efficiency Calculation

The material use efficiency measures the amount of silicon which ends up in the finished wafer compared to the amount of silicon introduced at the beginning of the wafer formation process. Figure 3 shows the relevant geometric considerations for the calculation of the material use efficiency.

Figure 2. Definition of dimensions for calculating finished wafer area

Figure 3. Measurement of plank geometric yield for a typical 8 hour production run

This efficiency depends on the details of the wafer formation process and can be resolved into the product of three factors: the applicator yield, Y_a , the edge trimming and kerf yield, Y_g , and the wafer visual and mechanical yield, Y_{VM} .

The equation which defines the material use efficiency is

$$MUE = Y_a * Y_g * Y_{VM},$$

where

MUE	=	material use efficiency
Y_a	=	application yield
Y_g	=	geometric yield
Y_{VM}	=	visual and mechanical yield.

Wafer Process Improvement (Task 17)

Central to the achievement of the Silicon-Film™ solar cell is the development of the wafer machine and the related wafer production process. The development of a wafer process capable of manufacturing depends on establishing control of the key process variables. During the first half of Phase III, the wafer production process went through significant transformations leading to a new version machine and improvements in parameter control.

Wafer process improvements focused on the following areas:

- machine reliability
- wafer throughput
- thermal control
- environmental control

Machine Reliability

In an effort to test and improve machine reliability of the Silicon-Film™ production machine, we performed several 14+ hour production runs. The longer run time allowed component failure modes to be identified and eliminated. As a result, wafer yield on the longer runs was significantly improved. Three 14+ hour production runs were performed between February 10 and March 8, 1994. Table 3 shows details of these runs including wafer yield.

Table 3. Wafer Yield for 14+ Hour Production Runs

Run #	Date	Length of Run (Hr:Min)	Rate (MW/yr)	Potential Wafers	Wafers on Visual/Mechanical Spec	Y _{VM}
797	2/10/94	15:10	2.1	1360	880	64%
804	2/24/94	15:28	2.3	1445	1162	80%
808	3/8/94	14:03	2.3	1270	1045	82%

The "Potential Wafers" column in Table 3 refers to number of wafers that could be cut from the total length of sheet produced. "Rate" refers to the production rate inferred by the areal generation rate, full production capacity, and 10.3 % efficient solar cells. Y_{VM} refers to visual and mechanical yield.

After the first production run #797, we identified setter joints and transport system alignment as a problem area; after about 9 hours of operation, visual and mechanical yield severely dropped due to discontinuity of the sheet at setter joints. Efforts were then made to improve the design of setter joints and the alignment of the transport system to maintain close coupling of setter joints throughout production. The results of these improvements are shown in the yields tabulated for Run #804 and #808.

We have planned specific machine changes to the current production machine and its components that are expected to result in increased visual and mechanical yield above the demonstrated 82% for a 14+ hour production run. These changes will be completed in June 1994; the new version machine is referred to as SF3M-P. The changes include improvements in precision alignment and leveling of the transport system to ensure close coupling of setter joints and improved thermal profile stability over prolonged operating hours. Currently, alignment and leveling of the transport system cannot be accomplished externally; the planned machine changes will allow slight adjustments to transport positioning while the system is operating. Inadequate insulating layers in the present system lead to slight fluctuations in thermal profile over time periods of several hours. Provisions for improved insulation are an integral part of the planned machine changes.

Some of the planks of Silicon-Film™ produced during the February production runs are shown in the photograph of Figure 4. As the sheet exits the machine, it is scribed into lengths that can be easily handled and stored (approximately 1 meter). The planks are stored on edge until cut to size. Figure 5 shows a wafer bin containing several hundred wafers awaiting solar cell fabrication.

Figure 4. Photograph of: (a) Silicon-Film™ continuous sheet exiting machine
(b) Silicon-Film™ planks stored on edge

Figure 5. Photograph of Silicon-Film™ 15-cm x 15-cm wafers and solar cells

Wafer Throughput

Improvements in visual and mechanical wafer yield leading to increased wafer throughput were previously discussed. Further increases in wafer throughput were achieved by increasing areal generation rate. From the beginning to the midway point of Phase III, we increased areal generation rate by 106%. This relates to machine production rates from 1.8 MW/yr to 3.7 MW/yr given no changes in number of production hours per year, resultant solar cell efficiency, or sheet width. As in Phase II, no degradation in material performance (as determined by the material's diffusion length as well as solar cell performance) was correlated with the increased areal generation rate. In fact, improvements in material performance were often associated with higher areal generation rates.

As shown in Table 4, mesa performance in terms of Voc, Jsc, and diffusion length (Ln) improved after an increase in areal generation rate (extrapolated to production rate); all other machine parameters were kept constant including gas ambient mixture. At this point, results indicate that the level of heat extraction associated with the 3.7 MW/yr machine rate led to the improvement in material performance. A set of experiments was performed where heat extraction was varied while keeping the machine rate constant at 2.3 MW/yr; the same improvement in material performance was achieved.

Note that mesas are fabricated across the entire width of the Silicon-Film™ sheet using the baseline solar cell fabrication process. No process enhancements such as gettering, front contacts, anti-reflection coating, surface passivation, or hydrogenation are used. Each device has an area of 0.2 cm².

Table 4. Median Mesa Performance as a Function of Production Rate

Run (date)	# of Mesas	Production Rate* (MW/yr)	Doped	Median Voc (mV)	Median Jsc (mA/cm ²)	Median Ln (μms)
838 (4/21/94)	31	2.3	Yes	478	17.2	18.5
844 (5/2/94)	32	3.7	Yes	516	17.6	20.7
839 (4/22/94)	32	2.3	No	461	18.1	29.9
843 (4/28/94)	32	3.7	No	487	18.7	29.4

* based on full production capacity, and 10.3 % efficient solar cells (best cell measured at NREL to date)

Thermal Control

Thermal control of the wafer production process is necessary to achieve the temperature ramp-up of materials prior to growth, to control the active layer growth, and minimize defects that can occur during the thermal ramp-down of the grown layer. These three zones and their

relative size (as of the beginning of Phase III) are shown in Figure 6. During the first half of Phase III changes were made to the relative sizes of all three zones. The final profile, as affected by the new modifications, SF3M-P, due for completion in June 1994 is shown as dotted lines.

Figure 6. Shape and relative size of thermal zones along the length of the Silicon-Film™ machine

Changes in areal generation rate lead to changes in the thermal environment that significantly affect material performance. An example of this was cited in the previous section. Hence, precise thermal monitoring during a production run and comparison of production run thermal profiles is critical to optimizing process control parameters.

During the first half of Phase III, monitoring of thermal profile was accomplished by both thermocouples and an infrared linescan camera. Thermocouples have been the core monitoring device due to their low maintenance, high reliability, and durability. Contact and close proximity thermocouples are both employed depending on the feasibility of contacting the heated surface. An IR scan camera was procured and installed to monitor the thermal profile along the width of the machine (and sheet) at one critical location along the machine length. The instrument scans the width of the plank up to 25 times per second. We find that the IR scan camera gives us improved thermal monitoring in real time. The ability to store the thermal profile either on computer disk or as a color print out allows us to monitor the consistency of the thermal profile from run to run as well as continually during one run. Eventually this instrument will be used in a feedback/control mode to reduce labor costs associated with operator control.

Environmental Control

The only recognized environmental variable is the gas that is present during sheet formation. The sources of the gas components are those that are intentionally introduced, and those that are generated during processing. We have experimented with three different intentionally introduced gases. Mixtures of these gases have also been investigated. Performance improvements

correlating to gas ambient mixtures have been observed, but are not as consistent as the improvements correlated with areal generation rate. These inconsistencies in addition to initial test case observations indicate potential performance improvements by separately controlling the gas environment between the ramp-up and growth zones of the wafer machine. The new version SF3M-P machine will provide this capability.

Wafer Process Boundary Conditions

The productivity of the Silicon-Film™ wafer process is determined by the square meters produced per hour (throughput) that meet the product performance specification. The critical element in determining the productivity of the present wafer manufacturing line is the active layer formation step, specifically the linear process speed and the width of the generated sheet and associated boundary conditions. The following sections describe the present productivity status of the Silicon-Film™ wafer machine including the issue of material use efficiency.

Linear Process Rate

The Phase II wafer production machine (SF3M) was designed to run at a production rate capable of 1.3 MW/year. It was empirically determined that higher speeds could be handled with some modifications to the current design. We were able to test and achieve a production rate capable of 3.7 MW/yr for operating times of approximately 4 hours.

To date, it has been found that linear sheet speed is machine design dependent. We have not yet approached an upper limit.

Process Length and Width

An important step in improving process yield was made in Phase II by transforming the Silicon-Film™ sheet process into a truly continuous process. Process length is determined by the duration of the production run and the linear sheet speed. To date, it has been found the width of the sheet is machine design dependent. We have not yet examined the possibility of an upper limit. We intend to investigate sheet widths of 16.0 cm wide during the 2nd half of the Phase III program in an effort to improve material use efficiency.

Large Area Wafers

Throughout the first half of Phase III, standard solar cell areas of 15 cm x 15 cm were handled. Larger solar cell areas of 15 cm x 45 cm were also fabricated to show future capabilities of the process. Full tooling to support manufacture of the 45 cm long cells is considered a premature investment for the technology and will not be a focal point of the Phase III effort.

Material Use Efficiency

Conversion to a continuous process led to a significant improvement in material use efficiency. Prior to this development, the areal yield of product was strongly influenced by the growth commencement and termination zones of each sheet. These zones comprised a significant portion of the sheet length. Now that the sheet is continuous, commencement and termination zones occur only once a day and are not a significant percentage of the generated area of sheet.

The applicator yield measures the amount of silicon material applied compared to the amount that is moved into the growth zone. The applicator yield throughout the first half of Phase III was 100%. This improvement from 99% in Phase II is due to smoother setter transport achieved by improving setter joints and guide rail connections. The geometric yield is based on the number of wafers that could be obtained from the as-grown planks compared to the amount of material applied. Throughout the first half of Phase III, 16.5 cm wide planks were produced which were cut into 15 cm x 15 cm cells. Based on a typical 8 hour production run and 30 cm of lost material at the beginning and end of the sheet, the ideal yield calculated from geometric considerations is 93%. The visual and mechanical yield accounts for the losses of wafers due to a variety of defects as well as to mechanical breakage. The visual and mechanical yield during our best 8 hour production run was 90% leading to a cumulative material use efficiency of 84%. This is not a significant change from Phase II's MUE of 86%.

To reach the Phase III material use efficiency goal of 90%, we plan on narrowing the grown sheet from 16.5 cm to 16.0 cm. Reducing the edge loss in this manner would bring the geometric yield to 96%. In combination with an increase in visual and mechanical yield to 94%, a 96% geometric yield and a 100% applicator yield would bring the overall material use efficiency to over 90%.

Wafer Machine Building Block Design (Task 18)

Experimentation during the first half of Phase III led to important information correlating machine parameters to material quality. Identification of critical parameters and the current capability of the present version wafer production machine (SF3M) led us to design a system upgrade (SF3M-P) to accommodate and control these critical parameters.

The new version machine planned for completion in June 1994 provides the environment we have established as critical to further process development. It provides the following capabilities:

- longer ramp up and anneal zones for 16 hour operation at production capacities from 3.7 to 4.7 MW/yr
- 88% larger cross-sectional area to accommodate additional insulation and provide a stable thermal environment
- precision external alignment and leveling of the transport system
- gas separation between the ramp-up and growth chambers
- modular chambers for easy chamber additions required by increases in areal generation rate

Material Quality Requirements

The most important electrical parameter determining the level of quality of the Silicon-Film™ active layer is minority carrier diffusion length. Both the magnitude of the minority carrier diffusion length and its spatial uniformity are important in establishing the utility of any photovoltaic material. This section describes the level of solar cell performance achieved and planned with present Silicon-Film™ material, indicates the known causes that limit performance in this material, and demonstrates the high degree of spatial uniformity achieved in the material and device parameters.

Expected Performance

The best measure of potential solar cell performance is minority carrier diffusion length. Figure 7 summarizes the predicted power from the 15 cm x 15 cm Silicon-Film™ solar cell as a function of diffusion length and solar cell design. The "present baseline process" refers to the baseline processing used for the deliverables at the beginning of the Phase III program including screen-printed contacts and automated spray antireflection coatings. The "optimized baseline process" refers to improvements expected from improved screen-print processing (less grid obscuration), improved fill factors due to improvements in contact firing, and improved open-circuit voltages associated with optimized bulk doping. The advanced design refers to the champion cells which incorporate evaporated contacts, a grid shading of 3.2%, improved blue response including surface passivation and improved emitter design leading to a 12% increase in current, an increase in voltage to 600 mV, and a fill factor increase to 0.74 leading to a 3.15 watt 15 cm x 15 cm solar cell.

Figure 7. Predicted power as a function of L_n

Characterization

The main characterization tool used during the Phase III program was the small area mesa test device. These devices are processed using the same baseline fabrication sequence used in making large area cells. The processing sequence is provided in Table 5.

Table 5. Processing Sequence Used for Fabrication of Mesa Test Devices

Surface prep - <i>sandblast</i> - <i>NaOH etch</i> - <i>HCl:H₂O clean</i> - <i>HF:H₂O etch</i>
Diffusion - <i>POCl₃ source</i>
HF: H ₂ O etch
Aluminum paste back contact
Isolate devices by dicing
Test

Mesas are fabricated edge to edge across a 15.5 cm width of a Silicon-Film™ sheet using the above baseline solar cell fabrication process. Comparing edge to edge performance provides important information on material quality uniformity. No process enhancements such as gettering, front contacts, anti-reflection coating, surface passivation, or hydrogenation are used. Each device has an area of 0.2 cm². Testing includes Jsc, Voc, and Ln measurements (from quantum efficiency measurements). Additional characterization includes quantum efficiency spectra, EBIC imaging, LBIC imaging, dark I-V measurements, and capacitance-voltage measurements for estimations of base carrier concentration.

An example of how mesa performance relates to AP-225 large area (240.25 cm²) device performance (before AR coating) is shown in Figure 8. The higher performance of the mesa devices over the AP-225 solar cells is due to the lower current density of the AP-225s most likely due to grid shading. Note that the mesa devices do not have front contacts. The quick turnaround mesa device has been an important qualification tool in determining which material lots should be processed into large area solar cells.

Figure 8. Correlation between AP-225 solar cell $J_{sc} \cdot V_{oc}$ product and mesa test device $J_{sc} \cdot V_{oc}$ product

Causes Limiting Performance

Determining the material properties that limit the minority carrier diffusion length, fill factor, and open circuit voltage has been a main focus of the Phase III program to date.

Minority Carrier Diffusion Length

Figure 9 shows the improvement in material quality (for unintentionally doped material) as measured by median mesa diffusion length during Phase III. Note that the diffusion lengths shown represent a median value derived from a particular mesa set; an average mesa set consists of 29 devices, each having an area of 0.2 cm^2 which are fabricated consecutively across the width of the Silicon-Film™ sheet. Diffusion lengths are estimated by quantum efficiency measurements on pre-hydrogenated material. The current median mesa diffusion length was around $27 \text{ } \mu\text{m}$; some individual mesa devices have $50 \text{ } \mu\text{m}$ diffusion lengths.

Figure 9. Median mesa diffusion length for mesa lots fabricated throughout first half of Phase III (material was not intentionally doped)

The improvement in diffusion length from a median of 18 μm early in Phase III to the present 27 μm diffusion length is due mainly to improvements in controlling heat extraction during crystal growth. Further increases in diffusion length are expected given further optimization of heat extraction control. In addition, increases in diffusion length are expected and have been demonstrated through post-growth processing steps such as hydrogenation and forming gas anneal. Significant effort is underway to use these post-growth processing steps to attain the largest possible gain in diffusion length and solar cell performance. These processes are further discussed in the Section titled "Solar Cell Fabrication Processes".

Diffusion length is periodically measured across the width of the Silicon-Film™ sheet to evaluate the spatial uniformity of across the width of the sheet. Figure 10 shows representative profiles of diffusion lengths measured on test devices across the width of a typical sheet from Phase II (Run #746) and a typical sheet recently grown in Phase III (Run #854). As shown, the magnitude of the diffusion length profile has improved while the uniformity across the sheet has remained relatively unchanged.

Note that the measurement error on our diffusion length estimates via QE is 10% which may account for some of the jagged edges in Figure 10. Efforts are continuing to both increase and smooth the level of the performance across the sheet. Data show that the thermal profile across the width of the sheet can be improved, and plans for improvement are underway.

Figure 10. Diffusion length measurements on test devices fabricated across the width of Silicon-Film™ sheets demonstrating current level of spatial uniformity

Fill Factor

Early in Phase III, fill factor was a dominant limitation to achieving a high yield, high performance device fabrication process. Average fill factors per lot for the screen printed cells ranged between 0.48 and 0.68 depending on the process parameters and the purity of the raw material. Evaporated contact cells fabricated from the most pure raw material had fill factors up to 0.73 leading us to the conclusion that both processing and raw material quality were the cause of the low fill factors. Action plans to purify the raw material and improve the screen-print solar cell process parameters were therefore put into place.

By eliminating a feedstock known to have deleterious impurities, we were able to pull the average fill factor per lot to over 60. In terms of processing, the fill factor of screen-printed solar cells has shown to be related to wafer weight. Contact firing parameters of temperature and time depend on wafer weight; heavier cells require higher temperatures and longer soak times. Efforts to sort wafers by weight led to a second increase in average fill factor per lot to the mid to high 60s. Further improvements in fill factor are expected from tightening the weight range of wafers produced and further improving material quality.

Open-Circuit Voltage

Midway through the first half of the Phase III effort, device performance results indicated a change in the correlation between bulk resistivity and open circuit voltage for intentionally doped material. We suspected that the machine improvements we had made to improve the quality of crystal growth had changed the manner in which the intentional dopant was incorporated. Although the diffusion length and device performance of undoped material improved due to the machine changes, the added improvement in voltage expected from intentional low level doping did not follow. In an effort to discover the cause of this inconsistency, we focused on isolating specific process parameters and studied their effect on the bulk resistivity and voltage of intentionally doped material. Thermal profiles, gas ambient, method of dopant incorporation, and device processing techniques were all investigated. Initial results from this study indicate that specific changes in gas ambient and thermal profile were causing the lower than expected voltages. In addition, a direct correlation between the defect clusters as observed by EBIC and the growth ambient was also found. Our current focus is optimization of these parameters (thermal profile and gas ambient) for maximum power from resulting devices.

Figure 11 shows the median mesa performance of 5 representative mesa sets at three different periods in the Phase III program; each median data point represents an average set of 29, 0.2 cm² mesa devices. Early in Phase III, doping provided the expected increase in voltage. By the end of the first quarter of Phase III, the same doping level resulted in lower than expected voltages. Efforts to identify which process parameters caused the low voltage problem led to the third, recent set of data.

Figure 11. Mesa device Voc and Jsc during the first half of Phase III, illustrating period of low voltage, intentionally doped material

As shown, open-circuit voltage values have improved; short-circuit current values have improved over the early Phase III values. Device modeling shows that an open-circuit voltage of 517mV is expected at the present bulk resistivity of 0.9 ohm-cm and diffusion length of 20 microns. We plan to continue to optimize diffusion length and bulk resistivity to attain a targeted 545 mV mesa device that with performance enhancement processing will lead to a 600 mV AP-225.

Statistical Process Control (Task 19)

An effective SPC system requires that: (i) there is a parameter representing the unit produced that can be easily quantified and which will provide a measure of the quality of that unit, and (ii) the process is one in which statistical methods can be applied. There are many critical parameters representing the AP-225 wafer and solar cell which could be used to measure the quality of the unit; wafer weight, solar cell performance parameters such as Jsc or Voc, and yield numbers such as geometric yield or visual and mechanical yield are a few examples. However, to date, we have not performed multiple, identical production runs consecutively which would provide the statistical base required for effective SPC. Growth parameters or machine components are usually modified or adjusted between runs in response to test device or AP-225 solar cell performance feedback. However, we expect to perform a group of at least 10 consecutive and identical production runs during the month of July. During the first half of the Phase III program, we set up a wafer quality specification station in preparation for the July production runs. Wafers are visually checked and measured following the outline below:

1. Cracks, chips, holes
2. Front surface texture
3. Back surface texture
4. Flatness, warping
5. Conductivity type
6. Wafer weight
7. Size

MINITAB for Windows® statistical software is currently used on individual production runs to gain experience on how best to collect the required data for SPC. We have identified the following 4 parameters which will be measured for SPC analysis of consecutive production runs:

1. Wafer weight
2. Mesa Jsc, Voc, Ln
3. AP-225 Jsc, Voc
4. AP-225 Power

Contact firing temperature is based on weight and has a dramatic effect on fill-factor. Therefore, wafer weight is an important parameter significantly affecting solar cell performance. Until the wafer production process is optimized, every wafer will be weighed and then sorted and fired

according to weight. Once the wafer production process is optimized, the spread of weights will become much tighter allowing a single firing temperature. At that time, a sample of wafers per run will be weighed and the results plotted as $\bar{X}$ -R charts via MINITAB for Windows®.

Mesa performance parameters of J_{sc} , V_{oc} , and L_n are available soon after the material is produced and is an excellent indicator of material quality and potential. These parameters are currently used to screen material lots for AP-225 solar cell fabrication. Two randomly chosen wafers from each run will be sent through the mesa process. The median and lowest value of each run will be plotted in a manner similar to $\bar{X}$ -R charts. Data are also available from the final test of AP-225 wafers. $\bar{X}$ -R charts will be used to track the performance and consistency of the production run wafers.

Processing parameters such as contact firing temperature have significant impact on fill factor and therefore power measurements for the AP-225 solar cell. This impact reduces the effectiveness of power as an indicator of material quality. Power will be therefore used as an indicator of the manufacturing process and will be monitored via $\bar{X}$ -R charts.

Solar Cell Fabrication Processes

Solar Cell Fabrication (Task 20)

This project relies on the parallel development of three technologies: (i) a growth technique that produces high quality, polycrystalline silicon sheets at high areal generation rates, (ii) a solar cell fabrication technique that captures the material's potential while qualifying as low cost manufacturing, and (iii) a module fabrication process that efficiently integrates the solar cells into a utility-scale power source. The first and third are discussed in the separate sections, while solar cell fabrication will be discussed in the sub-sections that follow. In developing a low cost solar cell fabrication technology, a baseline process is established while investigating advanced processes in parallel. Advanced processes that improve solar cell performance and are manufacturable at a reasonable cost become part of the baseline process; a process that provides a 5% increase in power can impact module cost by no more than 5%.

Current Baseline Process

At the end of the first half of Phase III, the baseline solar cell fabrication process incorporated the steps listed in Table 6.

**Table 6. Baseline Solar Cell Fabrication
Process Steps**

1) Surface Preparation (Sandblast + NaOH)
2) Gettering Diffusion
3) Etch Gettered Junction
4) Standard Shallow Junction Diffusion
5) PSG Removal
6) Print/Dry/Fire Back Aluminum paste over entire back Ag (98%)/ Al (2%) bus bars
7) Print/Dry/Fire Front Silver ink grid
8) Isolate edges
9) H+ Passivation
10) AR Coating
11) Test

Gettering Diffusion

It was found that a double diffusion process led to better overall performance than a standard single step diffusion. The double diffusion process involves a standard diffusion step (40 ohm/□), followed by etchback (in NaOH) of the diffused surfaces, followed by a second standard diffusion step (40 ohm/□). Two sets of AP-225 solar cells, all from the same wafer fabrication lot (#804), were fabricated using (i) a single diffusion process, and (ii) a double diffusion process; the rest of the processing was identical for both sets. As shown in Table 7, the median performance of the double diffused cells was higher in Voc, Jsc, and Power. No antireflection coatings were used.

Table 7. Device Performance of 15 cm x 15 cm Solar Cells Fabricated with Standard versus Double Diffusion Processes (no AR coating)

Diffusion Process	No. of Cells	Average Voc (mV)	Average Jsc (mA/cm ²)	Average FF (%)	Average Power (mW/cm ²)
Single	17	450	16.1	58.2	1.01
Double	17	462	16.6	61.7	1.13
% Improvement		2.7 %	3.1 %	6.0 %	11.9 %

It is believed that the improved performance is due to a gettering mechanism. The initial diffusion getters a significant number of impurities to the emitter, which is removed by etching. The second emitter is then formed in material of higher purity. Efforts are now underway to optimize the second diffusion to improve the blue response without sacrificing the low sheet resistance needed for screen printed contacts.

Grid Shading

During the first half of Phase III, the front contacts of our AP-225 solar cells were evaluated in detail. Two representative cells with different front contact processes were evaluated. Table 8 compares the characteristics of these cells.

As shown in Table 8, a typical screen-printed cell has a total shading loss of 8.8 %. The additional shading over the evaporated contact is due to the grid width. Efforts to lower total shading of the screen-printed contact to 6.0 % involve optimizing the screen-print application and drying process to reduce paste spreading. Process parameters (e.g. application parameters, screen design, paste thickness, drying parameters and firing temperature) affecting contact resistance and line width are all under investigation.

Table 8. Comparison of Two Representative AP-225 Solar Cells with Different Front Contact Processes

Property	Evaporated Contact Cell	Screen-Printed Cell
Metal Resistivity (ohm-cm)	3.4E-6	3.8E-6
Inter Grid Spacing (cm)	0.294	0.323
Metal Line Width (um)	100	200
Metal Line Height (um)	12	12
Number of Bus Bars (#)	2	2
Side Dimension (cm)	15.5	15.5
Bus Width (cm)	0.2	0.2
Tab Thickness (mil)	5	5
Emitter Sheet Rho (ohms/sq)	50	35
Device Power (watts)	2.5	2
Total Device Area (cm²)	240	240
Jsc w/Shading (A/cm²)	0.0224	0.0217
Resistive Losses	5.87 %	5.77
Shading Loss (total)	5.99 %	8.78 %
Shading Loss (grid, bus)	3.40 %, 2.58 %	6.20 %, 2.58 %

Hydrogenation

Efforts are underway to eliminate the need for hydrogenation in the baseline process. Post-hydrogenation gains have been linked to fill factor and wafer weight. As previously mentioned in this report, we currently sort wafers by weight and perform contact firing in groups defined by weight range. By optimizing the contact firing temperature of these weight ranges, we have improved pre-hydrogenation performance and reduced hydrogenation gains. Elimination of hydrogenation step from the baseline process will occur once the wafer weight range is tightened to a single category and post-hydrogenation gains are insignificant.

Anti-Reflection Coating

An automated spray anti-reflection coating (TiO₂) machine was built during the first part of Phase III. Process parameters were optimized offering uniform AR coating over the 15 cm x 15 cm solar cells at a throughput of 490 cells per hour. At these parameters, the typical power gain is 37% which is similar to our PECVD anti-reflection process. The throughput of the production line PECVD Si₃N₄ anti-reflection process is significantly lower offering only 210 cells per hour.

Encapsulation gain was evaluated for the spray AR coating versus the previous standard Si₃N₄ deposited via PECVD. A comparison was performed of reflection spectra for the visible wavelength range of 400 to 700 nm for typical cells with spray TiO₂ AR coating versus Si₃N₄ coating deposited via PECVD. It was found that an encapsulation gain of 2 to 6% is typical from

the spray AR coating, whereas the effect of the Si_3N_4 coating is less reproducible with a maximum potential gain of less than 2%. Figure 12 shows a comparison of post-encapsulation reflection and illustrates the benefits of the spray AR process over the PECVD Si_3N_4 process.

Figure 12. Comparison of post-encapsulation reflection of typical cells with TiO_2 spray AR coating and typical cells with Si_3N_4 PECVD AR coating

In conclusion, we consider the spray AR coating process to have successfully replaced the PECVD Si_3N_4 AR coating process, due to the significantly higher throughput of the process and the consistent power and encapsulation gains of the coating.

Baseline Solar Cell Performance

The best performance of a single cell to date using baseline processing is 1.93 watts. The best median (or average) performance of a lot of 32 wafers was 1.84 watts. We expect that the median (or average) baseline solar cell performance will improve to 2.0 watts once we achieve higher open-circuit voltage values (to 520 mV) associated with optimally doped material and higher fill factors (to 0.69) due to improved contact firing. Improvements up to a 2.5 watt cell are expected as a result of improved material quality leading to diffusion lengths in excess of 50 μm .

Advanced Processes

During the first half of Phase III, the advanced solar cell fabrication process incorporated the steps listed in Table 9. We have been using this process to fabricate the champion cells to be delivered during Phase III.

Table 9. Champion Cell Fabrication Process Steps

1) Surface Preparation (CP etch)
2) Getter Diffuse
3) Strip Junction
4) Aluminum Deposition on Backs (0.5 μm)
5) "Sandia-like" Diffusion
6) Forming Gas Anneal
7) Evaporated Contacts
8) RF Hydrogenation
9) CVD SiO ₂ passivation layer
10) CVD SiN AR Coating
11) Test

The **CP etch** surface preparation involves etching the cells in a mixture of $\text{HNO}_3\text{:HF:CH}_3\text{COOH}$ in a ratio of 15:2:5. This provides the smooth surface required by evaporated contact photolithography. The preliminary **gettering diffusion** is identical to that used in the baseline process; however, the second diffusion step is not. The second diffusion step is patterned after the work of Basore [1], and is referred to as the "**Sandia-like**" **diffusion**, the effect of which is described below. The purpose of the 0.5 μm thick **aluminum layer**, step 4, is primarily to act as a back contact, however, some secondary aluminum gettering during the high temperature diffusion step may occur.

Figure 13 shows the internal quantum efficiency (IQE) curves for two 1-cm² solar cells made on Silicon-Film™ material and compares: the results of a standard emitter diffusion schedule (855°C for 35 min) and the results of a "Sandia-like" emitter diffusion. The purpose of the modified diffusion schedule is to improve device blue response using a passivating oxide created during the diffusion process. These IQE data indicate an enhanced blue response for samples that received the modified diffusion. Device modeling indicates that the improved blue response can be expected to lead to a 5% improvement in device power.

The applicability of this modified process to present baseline solar cell manufacturing process hinges on the ability to make contact to the top passivator/emitter using a screen-printing process.

The two major issues are the need to have sufficient carrier concentration at the emitter surface to reduce contact resistance, and the need to establish contact through the passivating layer.

Figure 13. Internal quantum efficiency (IQE) curves for two 1 cm² solar cells made on Silicon-Film™ material with two different diffusion schedules

Figure 14 on the next page shows the doping profiles, measured by spreading resistance, for silicon single crystal wafers having (a) the standard diffusion schedule, and (b) the modified diffusion schedule that effected the enhanced blue response in the Silicon-Film™ material. These results suggest that:

- a) if the concentration at the surface is the key factor in establishing effective screen-printed contacts, then the modified diffusion should be "screen-printable", and
- b) if a deeper junction depth is advantageous in reducing junction "punch-through" (and subsequent shunting) during contact firing, then the modified diffusion could be beneficial.

The next step in this process development is to employ an engineering lot to establish the expected improvement in the present production-process.

a. standard diffusion

b. modified diffusion

Figure 14. Doping profiles in single crystal silicon measured by spreading resistance

The **forming gas anneal** process has demonstrated a significant gain in red response. Diffusion length gains of 72% are typically demonstrated.

To date, using **RF hydrogenation** has led to blue response degradation negating all gains realized by the Sandia-like diffusion. Thermal and/or CVD SiO₂ passivation layers have failed to recover the lost blue response to an acceptable level. Presently, we are considering an ion implanted hydrogenation step from the back surface similar to that demonstrated by Yagi [2] to attain the diffusion length gain required by a 3.15 watt solar cell.

Path to Demonstration of a 3.15 watt Solar Cell

The current median diffusion length of as-grown Silicon-Film™ material with a carrier concentration of $9.2 \times 10^{16} \text{ cm}^{-3}$ is 27 μm . Assuming a 72% increase in diffusion length as demonstrated in Phase II using a forming gas anneal process, the diffusion length would improve to 46 μm . Using these values in standard solar cell modeling leads to a 2.8 watt solar cell with Voc of 560 mV, Jsc of 29 mA/cm², and a fill factor of 0.73. Accordingly, we expect to demonstrate a 2.8 watt cell shortly.

Further improvements in the crystal growth process planned for the 2nd half of Phase III are expected to lead to longer diffusion lengths and higher voltages. Coupled with advanced processing enhancements such as a doubling of diffusion length by combining gettering and hydrogenation from the cell's back, we expect to attain the 3.15 watt solar cell deliverable using 50 μm as-grown material.

Material Cost Reduction (Task 21)

The purpose of this task is to reduce the material costs of the Silicon-Film™ solar cell process and reduce the hazardous waste produced. Progress is being made in both areas. Our main focus during the first half of Phase III was the NaOH surface preparation process.

As identified in Phase II and the beginning of Phase III, there are three inherent problems with this process:

1. unmonitored solution concentration,
2. accumulation of reaction side-products in the etching tank,
3. accumulation of etchant residues on wafer carriers.

Our present plan is to install both sodium ion and pH probes directly in the NaOH solution. Operators will be trained to continually monitor the sodium ion and pH readout displays and to replenish the etch bath as indicated.

To effectively monitor the concentration of the NaOH solution via sodium ion probe and provide the most reproducible etching conditions, the NaOH + silicon reaction side-products must be

continually removed. The reaction side-products composed primarily of sodium silicates contain sodium ions that will affect the probe reading and give false information as to the concentration state of the NaOH solution. To date, these side-products have been allowed to accumulate throughout the life of the etch bath. When the bath was determined to be exhausted, the entire bath including the by-products was appropriately neutralized and sent to waste tanks. This method not only prohibited effective monitoring of the NaOH concentration, it also led to premature disposal of viable NaOH solution.

The sodium silicates are polymeric, viscous masses that can easily be removed by a constant filtration of the bath. Plans are underway to design and fabricate this filtration system in-house.

The combination of monitoring etchant concentration and continual side-product removal will lead to significant reduction in cost, material usage, and waste as well as an improvement in wafer yield. These practices extend the life of the bath and allow us to reproducibly process more wafers per milliliter of etchant than was previously possible. The actual dollars saved is difficult to predict, but will be computed once control improvements are installed and operating smoothly.

An additional improvement to process control will be the comprehensive periodic cleaning of wafer carriers. To date, there has been no established plan to remove residues which accumulate on wafer carriers. There is a possibility that accumulated residues can transfer to the wafer and cause a change in wafer surface properties. We have established a weekly cleaning plan for wafer carriers that involves boiling them for 30 minutes in de-ionized water followed by baking them at 150°C for 30 minutes. We expect to implement this plan during the next several months.

Device Equipment/Process Automation (Task 22)

Automation of the wet chemical surface preparation process has been investigated. We expect that our transition to automation will be a slow one. As indicated above, improvements in process monitoring and control, reproducibility, and cost are required before a fully specified automated system could be implemented. Although we do not expect to achieve full automation of the wet chemical surface preparation process before the end of this PVMaT Phase III program, we do expect to be able to specify an appropriate system by that time.

As previously discussed, a fully automated spray anti-reflection coating machine was designed, fabricated, and operated in the processing of PVMaT deliverables. This automated machine demonstrated a throughput of 490 AP-225 solar cells per hour, yielding a higher throughput, a similar solar cell power gain, and an improved encapsulation gain over our PECVD Si₃N₄ process at a significantly lower capital cost.

Module Fabrication Process

AstroPower's module line handles ten different module designs. 90% of the modules planned for fabrication during 1994 consist of single crystal silicon cells with areas of 150 cm². The remaining 10% will be Silicon-Film™ modules; 12 of these to be delivered to NREL under this PVMaT contract and 312 to be delivered to the PVUSA site in Davis, California. Fulfilling the PVUSA order will generate the volume required to fully test automation projects planned for handling the AP-225 wafers. The baseline module fabrication process is flexible enough to handle any Silicon-Film™ wafer size we provide. The only limitation is the dimensions of the current laminator.

For this Phase III program, two AP-225 Silicon-Film™ modules are planned for fabrication: (i) the same 36 cell, 6 cell by 6 cell, module design fabricated and tested in Phase II, and (ii) a 56 cell, 8 cell by 7 cell, module design. The 56 cell module design, targeted for 170 Wp power will provide important feasibility information for a 112 cell module/panel under consideration for future development.

56 Solar Cell Module Fabrication Feasibility

A 56 cell module with 127.4 cm by 111.4 cm glass was fabricated during the first half of the Phase III program. Because this size module is nearing the limits of our present laminator, we began experimentation with this large area lamination early on. We found that all 56 cells structurally survived lamination. However, some shifting of individual cells during the process led to uneven cell spacing. Future 56 cell modules will eliminate cell shifting by securing solar cells to EVA prior to lamination.

Module Equipment/Process Automation (Task 23)

Three areas of automation are currently being investigated: (i) tabbing of front contacts, (ii) tabbing of back contacts, and (iii) module transfer to lay-up. The status and plans of each of these projects are outlined below.

The module team in conjunction with the accounting team are analyzing cell tabbing costs and the cost benefits associated with automatic cell tabbing. Results of this analysis and design options for automated cell tabbing equipment are expected to be complete in July.

In terms of the back contact, we are looking for a technology that will attach standard copper ribbon to an all aluminum-coated silicon surface. We currently use an Al-coated back with silver stripes on which tabbing material is hand-soldered. The advanced processing team has investigated three alternatives for automating back contact tabbing application: (i) ultrasonic welding, (ii) wire bonding, and (iii) ultrasonic welding pens which use fluxless solder. To evaluate the first approach, a visit was made to a plant that manufactures automated ultrasonic welding equipment for the fabric industry. Experiments using plant equipment resulted in broken cells; modification of this equipment to handle the brittle (relative to fabric) solar cells would be necessary. AP-225s have been sent to an automated wire bonding equipment manufacturer for

tabbing tests which are not yet complete. The ultrasonic welding pens will be our fall-back alternative if the first two options fail. If viable, these welding pens can be built into automated equipment designed and built in-house.

Plans for automating module transfer to lay-up have resulted in a drawing package scheduled for completion by May 31st. The decision to build the prototype lay-up assembly in-house or to contract to a local machine shop has not yet been made. However, completion of this automation project including testing is expected before the end of the contract.

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