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A PIPELINED SUPERCONDUCTING DIGITAL PROCESSOR†*

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A team consisting of groups from TRW, Conductus, Stanford University, the University of California at Berkeley, and the National Institute of Standards & Technology (NIST) at Boulder, Colorado is building a high performance superconducting digital signal processor. This processor is based on advanced superconducting digital technology, low temperature semiconductor technology, optical communications technology and multi-chip module packaging technology. In this abstract, we describe this system, referred to as the hybrid Josephson Junction Digital Signal Processor (JJDSP). This system has been designed to maximize the benefits of Josephson Junction (JJ) logic, while minimizing the restrictions imposed by its limitations.

Figure 1. *Proposed Hybrid Processor with 10 GHz FFT Engine. All data paths are 32 bits wide unless otherwise indicated*

Superconducting Josephson digital integrated circuits can offer significant advantages for digital processors [1], provided circuits can be built to provide the requisite level of complexity and

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system-level performance. Fujitsu [2] and others [3] have demonstrated niobium based digital circuits with gate delays as low as 1.5 ps and power dissipation of only a few mW for a 5-10,000 gate chip. TRW is designing JJDSP logic circuits based on 4°K JJ latching logic, with RSFQ used where it has both a demonstrable performance advantage and can provide the level of complexity required.

The hybrid processor design, shown in Figure 1, was chosen to take advantage of the strengths of superconducting logic, while working around weaknesses. The core processor, at 4°K, is similar in concept to a "data flow" design, where processing is determined by the availability and flow of data, rather than instructions as in a traditional computer. This architecture is ideal for superconducting logic, because it uses extensive pipelining, allowing low fanout logic designs to be used, and also because it can be configured for serial, first in/first out (FIFO) buffers instead of RAM storage. Instructions and status outputs move with the data through parallel pipelines, so there are no complex, out-of order instructions or branches. Programming can be done once, archived in standard libraries in CMOS SRAM as shown in Fig. 1, and appended to the data as it is fed to the 4°K processor.

The 4°K core processor is implemented with an arithmetic unit and FIFO. The multiple, cross connected FIFO chips are designed to allow processing of data in one set of FIFOs while the other set is being loaded from the relatively slow 77°K silicon SRAMs. This architecture is optimized for performing the Fast Fourier Transform (FFT) and other commonly used DSP operations. The coefficients for the FFT are stored in a separate set of FIFOs, while the control stream is contained in a single 16 bit wide FIFO. This design requires four basic chips: FIFO, multiplier (MULT), arithmetic logic unit (ALU) and a "glue" chip, which contains miscellaneous support functions. A full 32 bit JJDSP can be constructed with less than 50 chips, with each chip containing from 5,000 to 15,000 equivalent latching logic gates.

The 77°K section includes a large, 1 ns CMOS SRAM, which will buffer the data input and output from the 4°K section. A widely used DSP controller chip (e.g.: TI 320C40) is used as system controller, since it also provides an extensive library of DSP functions and is can easily be programmed to perform specialized functions. The 77°K interface operates at 1 GByte per second or 1 byte/nsec, which is the clocked access time of the fastest available CMOS SRAM operating at 77°K.

The JJDSP is designed to deliver high performance for industry standard, widely recognized operations. A common industry benchmark is the 1024 point, complex FFT. With the 100 ps clock of the core processor, and a latency through the core processor of approximately 10 pipe stages, the execution time required for a 1D FFT will be about 1 μ s for the 1024 point FFT. A 2D FFT of the same size will require 2.1 ms. This compares very favorably with 683 ms and 1.39 s, respectively, for conventional silicon DSP chips [4]. One potential application for the JJDSP is in medical imaging, specifically computed tomography (CT) or magnetic resonance imaging (MRI). In order to derive CT images in real-time, the processor must perform a $1K^3$ reconstruction in less than 32 seconds. This requires a 1K FFT speed of less than 2.5 μ s, which will be achievable with the JJDSP operating at 10 Ghz.

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