SPICE Macromodel for a 1-Megawatt Power MOSFET Switch

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Abstract - This paper presents a SPICE [1] macromodel for a 1-megawatt high power electrical switch which uses power MOSFETs as the active switching elements. The model accurately predicts the time dependent switching current and provides a reasonable representation of the time dependent switch resistance and voltage drop across the switch. Techniques for extracting model parameters for commercial power MOSFETs are discussed along with suggestions for extending the model to spark gaps and other high power switches.

Introduction

Many explosive systems such as conventional armaments are electrically activated. To fire the systems, charge is stored on a capacitor and then suddenly switched so that the capacitor discharges through electrical detonators. As it is often both expensive and difficult to simply build and test systems, simulation of the explosive electrical system is becoming an important activity. To perform these simulations with available electronic circuit simulators, some type of model which accurately depicts the switching characteristics of available switch components is required. As none of the commercially available simulators have a built in capability for high energy (high voltage, high current) switches, a macromodel approach is necessary.

The macromodel development presented in this paper is for high power switch elements such as power MOSFETs operated in the avalanche breakdown mode. Each parameter set developed is very specific to the power MOSFET and external circuit elements used. However, the basic macromodel is rather simple and the approach used to extract circuit-specific model parameters from experimental data is presented.

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Background

Typical applications of high energy switches in explosive systems require the switch to hold off potentials of 1000 V or more stored on special low inductance capacitors. Then, on command, the switch is required to pass on the order of 1000 A with very low power losses in the switch itself. This requires the switch to go from approximately an open circuit to a conducting state with resistance on the order of 0.1Ω and to make this transition within a few tens of nanoseconds.

The circuit of immediate interest was operated with 2000 V stored on a 120-nF capacitor. This potential was held off with two 1000-V power MOSFETs placed in series. Also in series with the switches and the storage capacitor was the detonator with an approximate impedance of 0.25Ω . This circuit is essentially equivalent to the same capacitor charged to 1000 V with a single 1000-V power MOSFET in series with the detonator. Therefore we will restrict the discussion to the equivalent 1000-V circuit.

Power MOSFETs typically can switch from a few amps to a few tens of amps at voltages ranging from a few tens of volts up to as much as 1000 V. On-state resistance for MOSFETs varies considerably among manufacturers and processes; but, for the higher voltage devices, on-state resistances of 0.5Ω to a few ohms are common.

In the normal conduction mode, power MOSFETs cannot switch sufficient power to fire detonators. However, if the MOSFET is holding off a voltage approximately equal to its rated breakdown voltage, and if the net reactance of the other circuit elements is on the order of about 0.25 to 0.5Ω with typically 100 nH of inductance, then the power MOSFET will enter an avalanche breakdown mode and conduct hundreds to thousands of amps with a very low on-state resistance.

Any attempt at modeling the avalanche mode power MOSFET requires the model to behave like a normal power MOSFET during the initial portion of the switching, and then transition to the avalanche mode for the remainder of the capacitor discharge and any subsequent ringing of the circuit.

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Model Development

Circuit Behavior

An example of the drain-source voltage (VDS) and current (IDS) characteristics of a power MOSFET conducting in the avalanche breakdown mode in a high energy electrical switch is presented in Figure 1. Note that during the initial "normal" conduction mode, the current peaks in the low hundreds of amps. Then, suddenly, the slope of the current waveform increases sharply; IDS rises to around 1000 A; and VDS falls off sharply. The circuit then begins to ring with the characteristics of an LCR circuit.

Figure 1. Drain-Source Voltage and Current Characteristics

When the current and voltage suddenly change, the MOSFET enters what has been called an "avalanche breakdown mode" (though this is not thought to be a result of impact ionization). Analysis of the firing of numerous MOSFETs suggests that the onset of avalanche breakdown occurs when current passing through the MOSFET reaches some approximately fixed threshold value. Once this current threshold is reached, the MOSFET switches modes and conducts a much greater current with very low voltage drops.

Modeling Approach

Any model developed would need to approximately duplicate these firing characteristics, including the time dependence of the initial current, the threshold current value, and the current and voltage characteristics during avalanche mode.

A schematic of the avalanche mode power MOSFET macromodel is presented in Figure 2, while a netlist for a model designed to simulate a particular switch is presented in Table 1. The netlist in Table 1 includes both the subcircuit AVALMOS (which represents the actual MOSFET) and the external circuitry (a resistor, an inductor, and a capacitor) used to simulate the appropriate lab circuit.

Figure 2. Avalanche MOSFET Macromodel Schematic

— VDS
— IDS

FIGURE 1.

FIGURE
2.

Table 1. Netlist for Entire Laboratory Circuit, Including Avalanche MOSFET Subcircuit

Because the MOSFET in the switch had two distinct areas of operation, the modeling approach was to create a subcircuit (AVALMOS) containing two level-1 MOSFETs in parallel to represent one actual MOSFET. The first MOSFET in the subcircuit is MOSNORM; it simulates the actual MOSFET conducting in its normal mode and exhibits higher drain resistance (RD) than the other MOSFET in the subcircuit. Voltage source VIDSMON in conjunction with current-controlled voltage source HLATCH monitors the total current flowing through the circuit. Once the threshold current is reached, the sensing circuit activates a latch circuit that initiates conduction through the second MOSFET (MOSAVAL). The lower RD of MOSAVAL simulates the real MOSFET operating in the avalanche breakdown mode. Once this low-resistance MOSFET turns on, it remains on. The schematic in Figure 2 clearly shows the parallel MOSFET structure, the current sensing components, and the latch circuit.

Parameter Extraction

Parameter extraction for the model is straight forward and requires values of known circuit elements, measurements from laboratory data, and a series of simple calculations.

Parameter calculations for the model require knowledge of the following values from the actual lab setup: the capacitance and initial voltage of the external capacitor, and the value of the load resistance.

Also required are "ring down" measurements from the actual laboratory MOSFET circuit. The ring down measurement consists of digitized traces of the MOSFET's VDS and IDS as a function of time. An example of ring down data appear in Figure 1 and are specific to the actual laboratory components used.

Model parameter values are initially calculated using the method outlined in Table 2 and later fine tuned to improve the accuracy of the simulations. For example, for the IDS waveforms, target characteristics of the fine tuning process include peak values, initial frequency, and ratios of maxima.

```

Avalanche MOSFET Modeling
XAVAIL      1  2  3  3  AVALMOS
*           |  |  |  Substrate/Bulk
*           |  |  |  Source
*           |  |  |  Gate
*           |  |  |  Drain
LEXT        5  1  38nH
CEXT        5  4  0.12uF
RGND        4  0  100M
REXT        3  4  0.1
VGSNORM     2  3  PWL(0s 0v 10ns 0v 70ns 10v 2us 10v)
.IC V(5,4)=1000V
***** BEGIN SUBCIRCUIT *****
.SUBCKT AVALMOS 10 20 30 30
VIDSMON     10 11 0
MNORM        11 20 30 30 MOSNORM
MAVAL        11 25 30 30 MOSAVAL
EGSAVAL      25 30 300 0 1
CDS          11 30 95nF
** Begin Latch Circuit **
HLATCH      100 0 POLY(1) VIDSMON -1420 10
DLATCH      100 200 DLATCH
R1           200 300 1
CLATCH      300 0 10n
RLATCH      300 0 50k
DCLAMP       0 300 DCLAMP
** End Latch Circuit **
.MODEL MOSNORM NMOS ( LEVEL = 1 VTO = 3 RD = 6
**PSPICE (MICROSIM)-SPECIFIC PARAMETER FOLLOWS
+ W = 1000
**ALL MOSFET PARAMETERS BELOW ARE INCLUDED FOR THEIR DEFAULT VALUES ONLY
+ AF=1 CBD=0 CBS=0 CGBO=0 CGDO=0 CGSO=0 CJ=0 CJSW=0
+ DELTA=0 FC=0.5 GAMMA=0 IS=1E-14 KF=0 KP=2E-5
+ LAMBDA=0 LD=0 MJ=0.5 MJSW=0.33 NFS=0 PB=0.8
+ PHI=0.6 RS=0 RSH=0 TPG=1 UO=600
+ VMAX=0 XJ=0 XQC=1
**PSPICE (MICROSIM)-SPECIFIC PARAMETERS FOLLOW
+ JSSW=0 L=1E-4 N=1 PBSW=0.8 RB=0 RDS=1E32 RG=0
+ TT=0 WD=0
**NSUB AND NSS HAVE NO DEFAULTS IN PSPICE (MICROSIM)
**PSPICE (MICROSIM)-SPECIFIC DEFAULT FOLLOWS
+ JS=0 )
.MODEL MOSAVAL NMOS ( LEVEL = 1 VTO = 1 RD = 0.3
**PSPICE (MICROSIM)-SPECIFIC PARAMETER FOLLOWS
+ W = 1000
**ALL MOSFET PARAMETERS BELOW ARE INCLUDED FOR THEIR DEFAULT VALUES ONLY
+ AF=1 CBD=0 CBS=0 CGBO=0 CGDO=0 CGSO=0 CJ=0 CJSW=0
+ DELTA=0 FC=0.5 GAMMA=0 IS=1E-14 KF=0 KP=2E-5
+ LAMBDA=0 LD=0 MJ=0.5 MJSW=0.33 NFS=0 PB=0.8
+ PHI=0.6 RS=0 RSH=0 TPG=1 UO=600
+ VMAX=0 XJ=0 XQC=1
**PSPICE (MICROSIM)-SPECIFIC PARAMETERS FOLLOW
+ JSSW=0 L=1E-4 N=1 PBSW=0.8 RB=0 RDS=1E32 RG=0
+ TT=0 WD=0
**NSUB AND NSS HAVE NO DEFAULTS IN PSPICE (MICROSIM)
**PSPICE (MICROSIM)-SPECIFIC DEFAULT FOLLOWS
+ JS=0 )
.MODEL DLATCH D ( IS = 1E-12 N = 0.1 BV = 20k
**ALL DIODE PARAMETERS BELOW ARE INCLUDED FOR THEIR DEFAULT VALUES ONLY
+ AF=1 CJO=0 EG=1.11 FC=0.5 KF=0
+ M=0.5 RS=0 TT=0 VJ=1 XTI=3
**PSPICE (MICROSIM)-SPECIFIC PARAMETERS FOLLOW
+ IBVL=0 IKF=1E32 ISR=0 NBV=1 NBVL=1 NR=2 TIKF=0
+ TBV1=0 TBV2=0 TRS1=0 TRS2=0
**PSPICE (MICROSIM)-SPECIFIC DEFAULT FOR IBV FOLLOWS
+ IBV=1E-10 )
.MODEL DCLAMP D ( IS = 1E-10 N = 0.1 BV = 15
**ALL DIODE PARAMETERS BELOW ARE INCLUDED FOR THEIR DEFAULT VALUES ONLY
+ AF=1 CJO=0 EG=1.11 FC=0.5 KF=0
+ M=0.5 RS=0 TT=0 VJ=1 XTI=3
**PSPICE (MICROSIM)-SPECIFIC PARAMETERS FOLLOW
+ IBVL=0 IKF=1E32 ISR=0 NBV=1 NBVL=1 NR=2 TIKF=0
+ TBV1=0 TBV2=0 TRS1=0 TRS2=0
**PSPICE (MICROSIM)-SPECIFIC DEFAULT FOR IBV FOLLOWS
+ IBV=1E-10 )
.ENDS
***** END SUBCIRCUIT *****
.TRAN 0.005u 2u
.END

```

TABLE
1

- ω_0 = IDEAL RADIAN FREQUENCY = NATURAL FREQUENCY OF AN L-C CIRCUIT = $2\pi f = 2\pi(1/T) = (L \cdot C)^{-1/2}$
- f = FREQUENCY OF IDS CURRENT WAVEFORM = $1/T$
- T = PERIOD OF IDS CURRENT WAVEFORM, MEASURED FROM LAB DATA
- a = ALPHA = $R_{total}/(2 \cdot L)$
- C_{EXT} = TOTAL CAPACITANCE; EQUAL TO EXTERNAL CAPACITANCE ADDED TO LAB CIRCUIT; VALUE IS ENTERED INTO NETLIST
- L_{EXT} = TOTAL INDUCTANCE; VALUE FOR NETLIST IS FROM CALCULATION BELOW
- ω = REAL RADIAN FREQUENCY = $(\omega_0^2 - a^2)^{1/2}$
AN APPROXIMATELY SELF-CONSISTENT SET OF PARAMETERS HAS
 $\omega_0 \cong \omega$, THAT IS $a \ll \omega$.
- $IDS, MAX1$ = VALUE OF THE FIRST IDS CURRENT PEAK AFTER AVALANCHE
- $IDS, MAX2$ = VALUE OF THE SECOND IDS CURRENT PEAK AFTER AVALANCHE
- DR = DECAY RATIO = $IDS, MAX1 / IDS, MAX2$
- R_{total} = EFFECTIVE TOTAL RESISTANCE OF CIRCUIT IN AVALANCHE = $R_{EXT} + R_{para}$
- R_{EXT} = VALUE OF THE EXTERNAL LAB RESISTOR (CURRENT-VIEWING RESISTOR OR LOAD RESISTOR); VALUE ENTERED INTO NETLIST
- RD_{norm} = THE MEASURED DRAIN RESISTANCE VALUE (FROM DIGITIZED LAB WAVEFORMS); ENTERED AS RD FOR THE NORMAL MOSFET MODEL STATEMENT (MOSNORM)
- RD_{aval} = THE CALCULATED DRAIN RESISTANCE VALUE; ENTERED AS RD FOR THE AVALANCHE MOSFET MODEL STATEMENT (MOSAVAL)
- R_{para} = THE PARALLEL RESISTANCE COMBINATION OF RD_{norm} AND RD_{aval}

Order of Calculations

- C_{EXT} IS KNOWN
- T IS MEASURED FROM LAB DATA
- $\omega_0 = 2\pi/T$
- $L_{EXT} = 1/(\omega_0^2 \cdot C_{EXT})$
- DR IS MEASURED FROM LAB DATA
- $R_{total} = [\ln(DR) \cdot 2 \cdot L_{EXT}]/T$
- $a = R_{total} / (2 \cdot L_{EXT}) = [\ln(DR)]/T$
- R_{EXT} IS KNOWN
- $R_{para} = R_{total} - R_{EXT}$
- RD_{norm} IS MEASURED
- $RD_{aval} = 1/[1/(R_{para}) - 1/(RD_{norm})]$

Table 2. Model Parameter Calculations

Values for the drain resistances in the MOSFET models are extracted as follows. An initial value for RD in the MOSAVAL statement (" RD_{aval} ") is calculated to give a proper total resistance during avalanche (see Table 2). MOSFET parameter RD in the MOSNORM statement (" RD_{norm} ") is the most difficult to accurately calculate. Its "values" are determined by dividing IDS into V_{DS} just prior to avalanche, can vary by two orders of magnitude, and steadily decrease

with time. An initial best guess for R_{Dnorm} is supplied to the macromodel; usually, R_{Dnorm} is then slowly decreased until the critical current for avalanche is reached.

Parameter Extraction Difficulties

Some complications exist in lab data which make a simple macromodel of avalanche MOSFET behavior difficult to create. Both R_{Dnorm} and R_{Daval} are dynamic over time. The changes in total resistance of the laboratory circuits dramatically affects the frequency of oscillation as seen in IDS waveforms. Also, the decay of IDS is only approximated as being purely exponential.

Model Evaluation

Simulation Performance

The overall performance of the macromodel exceeded our requirements. Actual applications relied on the drain current supplied through the load. Consequently, this work concentrated on accurate simulation of IDS. Measured laboratory data and simulated PSpice [2] data are shown in Figure 3 for IDS waveforms from the first switching circuit of interest (Circuit 1). Figure 4 shows measured and simulated waveforms for both current (IDS) and voltage (VDS) from a second circuit (Circuit 2) that used a different type of MOSFET. Figures 3 and 4 both show good IDS simulation results in the following areas: (1) the threshold current level for the onset of avalanche; (2) the change in slope of the IDS waveform at the onset of avalanche; and (3) the peak values, decay characteristics, and ring down frequency of IDS.

Figure 3. Measured and Simulated MOSFET Drain Current Waveforms for Circuit 1

Figure 4. Measured and Simulated MOSFET Drain-Source Voltage and Current Waveforms for Circuit 2

As seen in Figure 4, the simulation of VDS for Circuit 2 was qualitatively correct before avalanche. Drain-source capacitor CDS is added to create the "shelf" seen in the

FIGURE
3.

FIGURE
4.

simulated VDS waveform just prior to avalanche in Circuit 2. The simulation of VDS did have some problems, though. The greatest shortcoming of the model (as seen in Figure 4) is the phase difference between the measured and simulated VDS curves. This may be due to a lack of inductance in the subcircuit representing the MOSFET.

Despite the model's need for improved voltage simulations, it still has important uses. The model allows a designer to explore some variations in fireset circuit capacitance, inductance, and detonator resistance. Making such variations in a simulation will help designers to optimize the fireset circuit design analytically without having to resort to slower and more expensive laboratory bench testing.

Model Achievements

This model is believed to be both new and novel. It is the only attempt we know of at modeling power MOSFETs operating in the avalanche breakdown mode. The model relies on a novel combination of two MOSFETs with different resistances in parallel, combined with a latch and sensing circuit to control the firing of the low-resistance MOSFET. While this model does not exactly represent the firing characteristics of spark gap type high-energy switches, its performance is sufficiently close to allow a designer to replace the MOSFET in a circuit with a spark gap, take data, and extract model parameters.

Compatibility with SPICE Version 2G.6

A model that is SPICE2G.6 [3] compatible will be of use in the broadest range of circuit simulators. Although every effort was made to keep this model SPICE2G.6 compatible, PSpice's MOSFET channel width parameter W was used to improve the accuracy of the simulations. The only other deviation from the 2G.6 format is the unique default that PSpice uses for the diode model parameter IBV (current at breakdown voltage). While PSpice uses 1E-10 as its default value, SPICE2G.6 uses 1E-3. As indicated in the subcircuit listing of Table 1, the parameters which are specific to PSpice--which, with one exception, have been left at their default values to minimize changes in the model's performance when used in 2G.6 compatible simulators. Also, any parameter whose default value is infinite has been set equal to 1E32 in the netlist of Table 1.

Summary and Conclusions

We have developed and demonstrated the operation of a SPICE compatible macro circuit model for high energy switches. The model accurately simulates the firing characteristics of the drain-source current of a commercial power MOSFET operating in an avalanche breakdown mode. The model parameters are relatively easy to extract from measured ring down data taken on actual components. Slight modifications of the model would allow it to be used to approximately simulate the firing characteristics of a spark gap high energy switch.

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