Integrated Circuits for Managers*

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MASTER

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ABSTRACT

The organization and structure of a course on integrated circuits designed specifically for managers is described. Semiconductor device and circuit characteristics necessary for planning and understanding systems employing these devices were presented. The major part of the material concerned MOS devices, but enough bipolar theory and discussion was presented to allow comparison between the technologies. The techniques used to cover a very broad range of topics in a one week course are discussed. The unique concept of a "hardware diploma" and its utilization as a motivational tool is described.

INTRODUCTION

The need for continuing education in rapidly advancing fields such as engineering is clear and is being provided by professional societies, universities, the government, and private industry. Managers who are required to lead their advancing fields have a particular need to remain abreast of

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the capabilities of the technologies being developed and of the potential applications of these technologies. On the other hand the demands on the manager's time are compelling and he may feel that he does not have the time to take courses. This paper describes a course that was specifically designed to meet the needs of managers and which provides the high degree of motivation required to make the manager feel it is worth the investment of his time.

PREPARATION FOR THE COURSE

A set of pre-course required reading material was prepared and distributed approximately six weeks prior to the first lecture. The purpose of requiring this reading was to allow the entire class to start from a common base. It was felt that this common base needed to be established due to the wide range of backgrounds possessed by technical management personnel at Sandia Laboratories.

The course was structured to run 20 hours, four hours each morning for five consecutive days. During the afternoon and evening several hours of homework and study were required. This structure is better suited to deal with the types of demands a manager has on his time than the typical course structure with classes meeting once or twice a week over a

three month period. By having the class scheduled well in advance, it is considerably easier to block out a solid week of time than it is to protect the many smaller intervals associated with the conventional course structure. As a result of this scheduling, nearly all class members attended every session and did all of the required homework.

THE COURSE

This course was intended for all management at Sandia Laboratories and, therefore, it covered a very broad range of integrated circuit design and application areas. The course could not be focused on a limited segment of the integrated circuit technologies, but was forced to cover the entire spectrum as indicated in the course outline given below:

I. Introduction - Description of Simple Digital System.

B. Brief History of Solid State Devices.

1. Unipolar Devices

- a. Physical Description of Operation
- b. MOSFETS - Enhancement and Depletion
Devices, PMOS, CMOS, MNOS
- c. Gate Thresholds
- d. Field Inversion

2. Bipolar Devices

- a. Physical Description of Operation
- b. P-N Junctions

3. Special Devices Including Charge Coupled Devices, Microwave Devices, Light Emitting Diodes, etc.

C. Processing

1. Masking and Photolithography
2. Oxidation and Chemical Vapor Deposition
3. Diffusion and Ion Implantation
4. Metallization

D. Problems and Discussion

II. General Applications

A. Linear Circuits - Bipolar and Unipolar

B. Digital Circuits

1. Brief Review of Digital Logic
2. Discussions of Common Bipolar and Unipolar Logic Families

a. RTL

b. DTL

c. TTL

d. ECL

e. I^2L

C. Logic Simulation and Computer-Aided Design

D. Problems and Discussion

III. MOS Integrated Circuits

A. MOS Design Considerations

1. Voltage Levels
2. Shift Rate Limitations
3. Noise Immunity
4. Power Consumption
5. Clock Requirements

B. PMOS Circuits

1. Logic Inverter
2. Logic Gates
3. Counters
4. Shaping Circuits
5. Comparators
6. Code Converts
7. Dynamic and Static Shift Registers
8. Multiphase Clocking Systems

C. NMOS Circuits

1. Memories

D. CMOS

1. Complementary Inverters and Transmission Gate
2. NAND and NOR Configurations
3. CMOS Flip-Flops, Counter and Register

E. Problems and Discussions

IV. Hybrid Circuits, Reliability, and Radiation Effects

A. Reliability

B. Radiation Effects

- C. Hybrid Microcircuits
 - 1. Thin Film
 - 2. Thick Film
- D. Problems and Discussions
- V. Packaging, Digital Clock Review, Laboratory
 - A. Packaging
 - B. Digital Clock Review
 - C. Future Reading
 - D. Laboratory

The challenge of covering this spectrum in one week is obvious. It was clear that the extensive use of prepared visual aids would be required in order to minimize the time spent drawing or writing during the lecture. It was also clear that simply showing slides and discussing them would not provide the student with any record for future reference or study since he would not be able to take adequate notes. Extensive note taking would also tend to diminish the effect of lecture reinforcement and hinder the learning process. To solve this apparent dilemma, a ring binder of class notes was prepared and provided to each student. The class notes included a copy of each visual used by the lecturer. In most of the areas the visuals were accompanied by supporting written material and references which were of special interest to Sandia managers. The binder was constructed so that when opened, the visual or written material appeared on the

left-hand page while the right-hand page was blank and available for notes referring to the specific information being presented. The class notes eliminated the need for the student to copy any material presented as a visual and allowed him to associate any brief notes taken on a specific visual with that visual in his binder. Thus, the student could concentrate on what was being said as the lecturer amplified on the information shown on the visual. Two instructors were used to present the course material. They had written and edited the class notes and were equally familiar with the material. While one lectured (usually not more than one hour at a time) the other one sat in the class and was able to determine whether the material was being understood by the participants. When it became obvious that communication was lacking, the observer would ask a question or make a clarifying comment.

In deciding on the specific material to be covered in each of the areas listed above, the guiding principle was: What information will a manager need in order to properly direct projects for which he is responsible? This produced a considerably different course than would have resulted if the guide had been: What will a designer or processor need to perform his job adequately? One example of the course difference was that the description of the operation of solid state devices was based on physical intuition rather than the complete mathematical formulation of band theory.

THE DIPLOMA PROJECT

During the first lecture the participants were introduced to a complete digital system--a digital clock. It was explained that this system would actually be built and would jointly serve as a learning vehicle and as a diploma for those who successfully completed the course. They were also told that a description of the clock was about to be given, that terms would be used that they might not understand, but that all of the terms would be defined and described during the course. They were also shown a working model of the clock, shown how it was constructed so that it was easy to demonstrate and further told that they would be able to give essentially the same presentation by the time they had completed the course. The following is an excerpt from material then presented.

One of the most exciting advances in solid state technology has been the development of LSI. The digital clock to be described uses an LSI device and LED readouts. The single LSI package together with LED readouts and other packages containing transistors and resistors makes up the complete clock, all on two simple printed circuit boards. Figure 1 below shows the schematic diagram of the complete LSI digital clock. The normal readout configuration for the LED units is

shown at the right side of Figure 1. R_1 couples the 60 Hz signal into the LSI circuit. Circuits within the LSI package divide the 60 Hz signal down to 1 Hz for the clock counting circuits.

A multiplexed arrangement is used to drive the LED display units. With this mode of operation, the individual cathodes for each readout segment are connected in parallel and driven by transistor switches Q_1 through Q_7 . The anodes of each readout unit are driven sequentially by Q_8 through Q_{19} . A switching rate of about 1 kHz is set by C_3 and R_2 making the readout unit appear as though they are constantly energized.

A photograph of the clock chip is shown in Figure 2 and an overlay with blocks and pin numbers identified is shown in Figure 3.

The many unfamiliar terms introduced during the discussion of the clock operation encouraged the students to ask questions repeatedly throughout the remainder of the course because they realized that an understanding of these terms was required to fully understand their own "diploma." To further aid in this understanding the lecturers especially covered all of the terms introduced in the first lecture, either in the following lectures or in the homework problems.

THE LABORATORY

During the last period prior to the laboratory the material presented earlier about the clock was repeated and new details were added. This was an exceedingly active session in that each manager wanted to understand the circuit in order to successfully deal with any problems encountered during the construction period, and they also wanted to be able to explain their "diploma" to visitors to their offices.

A clock kit was constructed to make the assembly easy and fast (approximately 2 hours) yet require the participants to complete a few of each of the steps required to construct a more conventional kit.

Figure 4A is a photograph of a completed clock and Figure 4B shows the clock "drawer" in the open position. The faceplates were individualized for each participant from silver-plated, turquoise colored printed circuit board material. Figure 5A is a drawing of the display board and Figure 5B shows the mother board and the location and orientation of the special dual-in-line packages (DIPs) used to speed up the assembly process. Figure 6 schematically shows the DIPs and their relation to the total circuit.

Each participant had to insert the seven-segment displays and the DIPs into pre-attached sockets; solder in four LEDs for

colons, a 500 μ fd power supply capacitor, a fuse, and the power cord; mount the mother board and switches on the drawer portion of the case; and install the display board before applying power.

The laboratory was set up in a room adjacent to the lecture room. Each participant was supplied with the necessary tools. Again, the excitement was very high. There was some competitive spirit about who would finish first, but a much stronger spirit of whose clock would work properly first (in essence who would be first to receive their diploma).

The participants learned that too much heat will cause the printed conductor to separate from the board, that great care must be taken in handling p-channel MOS devices which are sensitive to static discharge damage, that IC Dual-in-line package leads were fragile and that the leads must be inserted into the socket with care, and that too much solder will bridge to another conductor and cause a short.

Two regular course instructors and a technician were available during the lab to assist any who experienced difficulty and to help them trouble shoot.

Most of the participants finished in the allotted time and all agreed it was one of the highlights of the course.

EVALUATION

A questionnaire was prepared for the participants to complete after the course was over. There were two main parts to the questionnaire. The first part was general and solicited comments about the following topics (a) reasons for taking the course, (b) the participants educational and professional background, (c) usage of math in the course, (d) out of class assignments, (e) the laboratory, (f) the organization of the course, (g) the relative difficulty of the course, and (h) whether the course should be continued. The second part of the questionnaire was specifically on the course content. The participants were asked to check one of four choices (too much material, about right, too little material, or eliminate completely) about the following topics: (a) Solid State Physics, (b) Device and IC Processing, (c) Computer Aided Design, (d) Logic Design, (e) Analog Design, (f) Bipolar Devices, (g) MOS Devices, (h) Applications of IC's, (i) Reliability and Radiation, (j) Packaging, (k) Hybrid Technology, and (l) Digital Clock. An example tabulation from one of the classes is given below.

	Too Much Material	About Right	Too Little Material	Eliminate Completely
Solid State Physics	(1)	(5)	(3)	
Device & IC Processing	(3)	(4)	(2)	
Computer-Aided Design	(1)	(7)	(1)	
Logic Design	(2)	(4)	(3)	
Analog Design		(5)	(3)	
Bipolar Devices	(3)	(5)	(1)	
MOS Devices	(2)	(5)	(2)	
Applications of ICs	(1)	(8)		
Reliability & Radiation	(2)	(7)	(1)	
Packaging		(8)		
Hybrid Technology		(9)		
Digital Clock	(1)	(5)	(1)	

The spread between too much material and too little material was to be expected because of the widely different backgrounds of the participants. The course was offered four times for a total of 40 participants. Each one was slightly different from previous ones because the constructive comments made by the participants were integrated into the course.

CONCLUSION

As the need for continuing education becomes increasingly more acute, especially among managers and top executives, a course such as this can be exceedingly valuable. Every participant felt that it was a good investment of his time. The hardware "diploma" was enthusiastically accepted by the class.

A possible disadvantage of such a course is the cost of tailoring the class notes and laboratory material to a

particular company's managers. However, in most cases, when these costs are compared to the expenditures the managers influence, the preparation costs are insignificant.

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Figure 1. Schematic of LSI Digital Clock

Figure 3. Function Identification Blocks of Clock Chip.

Figure 4A. Completed Clock

Figure 4B. Clock in Open Position

Figure 5A. Display Board

Figure 5B. Clock Mother Board