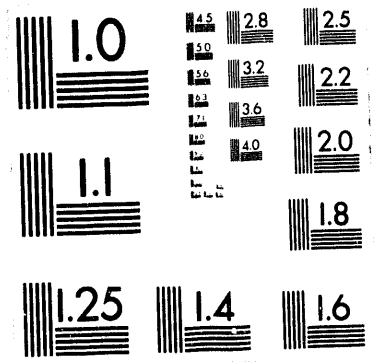
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# HIGH TEMPERATURE SUPERCONDUCTING DIGITAL CIRCUITS AND SUBSYSTEMS

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## ABSTRACT

The advances in the fabrication of high temperature superconducting devices have enabled the demonstration of high performance and useful digital circuits and subsystems. The yield and uniformity of the devices is sufficient for circuit fabrication at the medium scale integration (MSI) level with performance not seen before at 77K. The circuits demonstrated to date include simple gates, counters, analog to digital converters, and shift registers. All of these are mid-sized building blocks for potential applications in commercial and military systems. The processes used for these circuits and blocks will be discussed along with observed performance data.

## INTRODUCTION

Superconducting digital technology has long held the promises of high speed and low power, first in low temperature superconductors (LTS) and more recently, in high temperature superconductors (HTS). The basis for such technology is in the Josephson junctions and other active elements. Relatively recent improvements in these basic devices in HTS have led to circuit demonstrations of modest complexity made from $YBa_2Cu_3O_7$ (YBCO) and operating at 77K. There building blocks form the basis for systems applications and are the subject of discussion in this paper.

## THE TECHNOLOGY

All of the circuits to be described are fabricated with a maximum of 7 mask levels. One or two superconducting levels are used with dielectrics, normal metal wiring, contact levels, and material modification layers. Most of these steps are quite standard in the industry and will not be discussed here. The devices, two varieties of Josephson junctions and a flux flow transistor, do warrant discussion since they form the basis for the digital technology.

One of the Josephson technologies is a superconductor-normal-superconductor (SNS) edge structure[1] shown in Fig. 1. This junction structure was chosen because of its relatively straightforward process flow and useful junction parameters. This junction structure uses a $CaRuO_3$ or doped YBCO normal metal layer separating two YBCO layers in an edge geometry shown in Fig. 1. These are desirable barrier layers for a number of reasons. Both are cubic perovskites with a lattice parameter of 3.85 Å which falls between the *a* and *b* lattice parameters of YBCO. They are metallic and can be grown in conditions compatible with YBCO. Also, $CaRuO_3$ is chemically compatible with YBCO and its conductivity does not appear to be strongly dependent on doping or oxygen concentration. Both the YBCO and the barrier films are laser ablated. An edge geometry was used to keep the critical currents reasonable since the barrier conductivity is quite high. Current -voltage (IV) curves for these junctions closely follow that predicted by the standard resistively-shunted junction model[2] with critical currents at 77K of 80-100 μA and normal state resistances ($R_n$) of 1.5-2 Ω. From DC tests on large numbers of junctions, the expected absolute spreads are about ± 30-40% on critical current and ± 10% on $R_n$. The more recently used doped YBCO normal metal layers produce junctions with critical currents of 300-800 μA and normal state resistances of 0.1-0.5 Ω. The spreads on the critical currents in these devices is about ± 22% on $I_c$ and ± 9% on $R_n$.

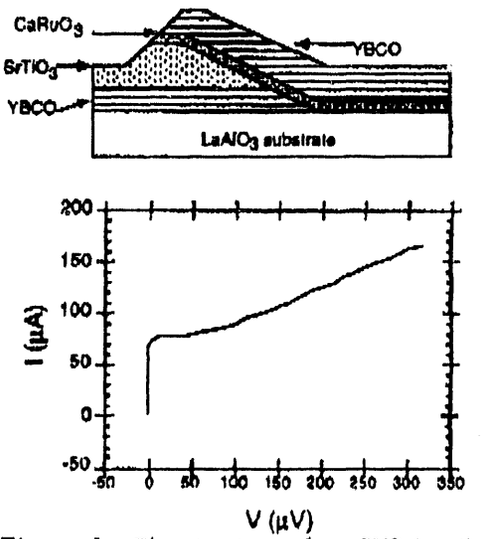


*Figure 1. The structure of an SNS junction and a corresponding IV curve*

The second Josephson technology is based on electron-beam defined nanobridges[3] shown in Fig. 2. In these junctions, a narrow bridge (20-90 nm wide and long) is defined by e-beam lithography and the surrounding material removed by wet etching. A junction barrier is apparently formed by natural out-diffusion of oxygen from the bridge region. Although the parameters are not as useful as those of the SNS junctions, these junctions are extremely uniform. Typically, a single bridge has critical current of 15-20 μA and a normal state resistance

of 15-30 Ω at 77K. Based on DC tests, the expected spreads on $I_c$ are ± 10% and on $R_n$ are ± 4%.

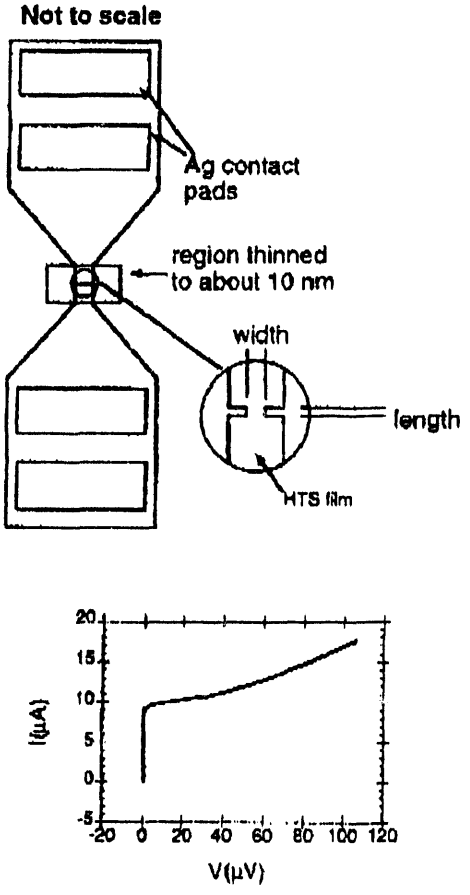


*Figure 2. The structure of a nanobridge junction and a corresponding IV curve.*

The third type of device is a three terminal superconducting transistor based on the magnetic control of flux flow called a superconducting flux flow transistor (SFFT)[4] or magnetic effect transistor (MET). It is based on the magnetic control of flux flow through one or more links arranged in parallel as shown in Fig. 3. When the material is sufficiently crystalline and the links are thinned relative to the surrounding banks, magnetic flux quanta can nucleate and flow rather easily through the bridges driven by a Lorentz-type force. From a bias current alone, sufficiently high to exceed a lower critical field, vortex-antivortex pairs are generated. When a control line current is applied, the local critical field is suppressed and additional flux quanta are able to enter the system. This creates the deviation of the upper quasi-linear slope shown in Fig. 3. This flux flow state is characterized by an output resistance of several ohms and an inductance of a few pH depending on the exact link design. A local magnetic field, as can be generated by a local control line, can cause additional flux to nucleate in the bridges and hence alter the characteristics as shown in Fig. 3. This response can be characterized by a transresistance $r_m$ which is nominally 4 Ω/μm for a limited range of bridge lengths (accompanied by an output resistance of about 0.5-1 Ω/μm).

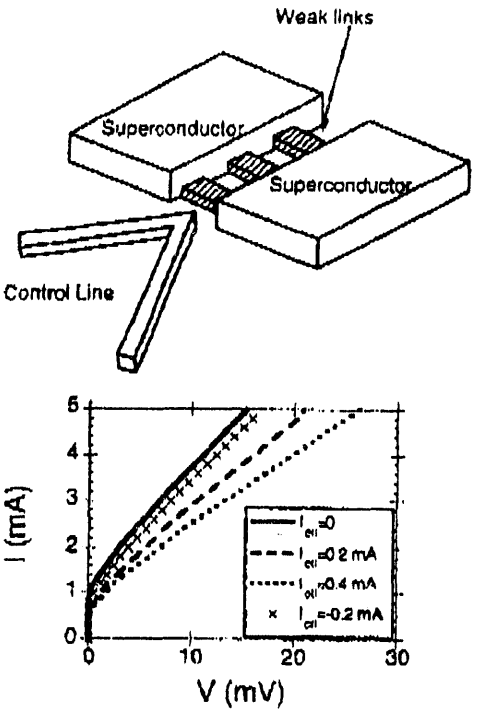


*Figure 3. The structure of a flux flow transistor and a corresponding IV curve set.*

Each of these device structures plays a key role in the digital technology to be presented. The junctions are basically two terminal devices (that can be equipped with control lines for three terminal action in some cases) and are useful for extremely efficient and fast logic, serial memory counting structures, comparators, etc. The SNS junctions have an advantage in absolute circuit parameters (making designs more realizable) while the nanobridges have better uniformity enabling more complicated and interdependent circuits. The choice of junction will vary with the circuit. Flux flow devices are true three (or four) terminal devices with gain which make them invaluable for SRAMs, buffer and driver logic and amplifier structures. More than one of the devices may be used in a hybrid circuit or block depending on the circuit needs.

## CIRCUITS AND SUBSYSTEMS

Various logic gates have been demonstrated in a variety of configurations. Fed back flux flow gates are one family based on an ECL-like architecture. While the IV characteristics shown in Fig. 3 are somewhat soft, a pair of devices in a fed back arrangement makes a convenient gate family. A full family of AND, OR, NOR, NAND and XOR gates have been demonstrated with gate delays as low as 10 ps. These are discussed more fully elsewhere[5]. A family of Josephson gates based on the long standing LTS family of RSFQ have also been demonstrated in HTS using the junction technologies discussed above. Gate delays in this pulse-based logic family have been as low as 5 ps and work continues on developing higher density random logic.

Shift registers represent one of the more elaborate components and they are surprisingly easy to implement in superconducting technology. One structure, based on pulse manipulation[6], is shown in Fig. 4. The information is stored in the lower data register as the presence or absence of a circulating loop of current in each cell. Such data is relatively easy to readout with an individual superconducting quantum interference device (SQUID, 2 junctions in an inductive loop) or with a flux flow-based amplifier[4]. A clock pulse propagates along the arbitration register, whose purpose is to ensure that the clock pulse gets to the right segment at the right time, causing the circulating current bits to move to the adjacent cell. Since only a single junction must switch to perform the move, the minimum clock period can theoretically be less than 5 ps. Clock periods as low as 8-9 ps have been demonstrated with limited data sets.

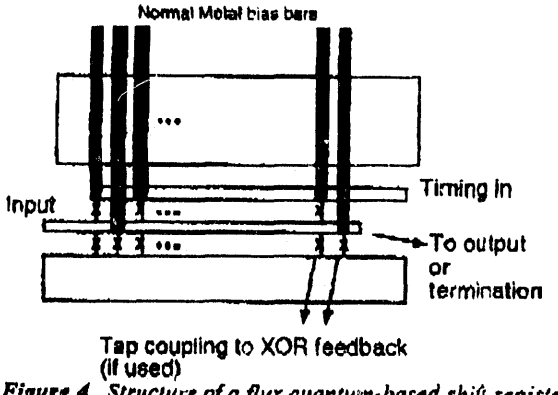


*Figure 4. Structure of a flux quantum-based shift register in which the x's represent junctions. Data is contained in the lower 'data' register in the form of the presence or absence of a circulating current in the loops between pairs of junctions.*

Of great use in military and commercial electronics applications are pseudo-random bit sequencers (PRBS) which also provide one of the best ways to test these shift registers at speed[7]. The concept of the PRBS is shown in Fig. 5 and it consists, in its simplest form, of a shift register with feedback in the form of an exclusive-OR of two of the last few bits. For a given starting register state (not all 0s), the register will produce a stream of seemingly random bits. This stream will be completely reproducible with the same starting data. Such a structure is obviously useful for encoding but is also ideal for testing a variety of digital and communications devices since it avoids some pattern dependent results. To test shift registers, two PRBS blocks can be used. Each is loaded with the same starting data (which can be done at low speed with a large clock period). The outputs are coupled to another exclusive-OR gate and the high speed clocks to the PRBS units are started. Every time there is a difference between the two register outputs, the XOR output will go high, triggering an error latch. These circuits were run for times of up to 15 minutes (a cooling limit) at various clock periods with different starting data sets to try to gain an understanding of the error profiles. These results are summarized in table I and indicate a relatively low error rate.

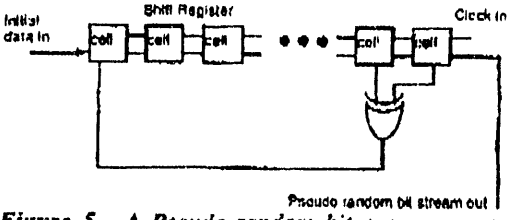


*Figure 5. A Pseudo-random bit sequencer structure based on a shift register and exclusive-OR feedback.*

| Start Patt. | Clock | log(err rate) |
|---|---|---|
| 111111110... | 10 GHz | < -12 |
| 111111110... | 60 GHz | < -12 |
| 101010100... | 10 GHz | < -11 |
| 100100100000.. | 10 GHz | < -10 |
| 100010000000.. | 60 GHz | < -12 |

*Table I. Table showing the maximum error rate in the shift register for different clock frequencies and starting patterns.*

Another block of considerable value is the analog to digital converter (ADC) in which enormous resources have been expended in many technologies. Many superconducting architectures have been demonstrated in LTS and several in HTS. One such architecture is based on the unique voltage to frequency conversion present in the Josephson element. If an unknown analog signal is coupled into a biased SQUID, a train of pulses will be produced whose period is directly related to the signal amplitude in a well known way. By counting these pulses over a stable time period, an accurate conversion can be obtained. The structure of this ADC suitable for HTS fabrication is shown in Fig. 6. The counter is a structure known as the theta cell and it also belongs to the family of pulse manipulation logic. An initial incident pulse produces a circulating current in the upper half of the cell. The second pulse induces this current into the rest of the cell and produces a pulse which is sent to the adjoining cell. Thus it is a true binary counter. The counter cells can operate, in principle, at speeds of several hundred GHz and the 8th bit has been observed counting at nearly 1 GHz (suggesting the LSB is counting at near 250 GHz). A plot of count in a 2 ns interval for a variety of inputs is shown in Fig. 7 and illustrates at least basic functionality.

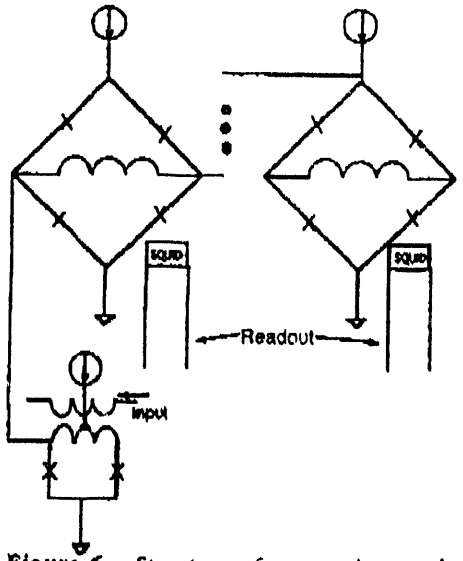


*Figure 6. Structure of a counting analog-to-digital converter (the x's represent junctions). The input current causes generation of a pulse stream by the 2 junction SQUID (to which it is coupled) whose period is directly related to the input amplitude. The rest of the circuit counts these pulses to do the conversion.*

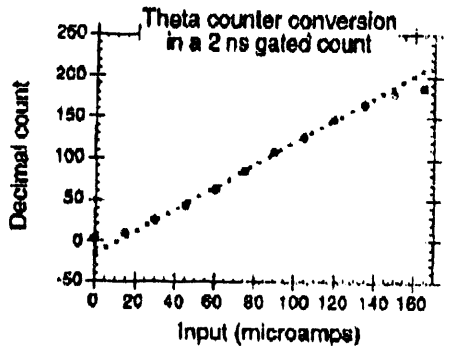


*Figure 7. Decimal count vs. input amplitude for the counting ADC. The range can be changed by using different input coupling.*

The counter output was coupled to a simple resistive digital to analog converter (DAC) to reconstruct rf waveforms. The result of a sinusoidal input is shown in Fig. 8 with 8 bits of resolution. Twelve bit and larger units are in design at present as are other HTS architectures.

## IMPACT AND CONCLUSIONS

A variety of superconducting digital circuits have been demonstrated at 77K with potentially very interesting performance levels. The densities and complexity of these circuits promise to expand due to the increasing yields and uniformity of the device processes. Circuits of gate complexities over several thousand are now in fabrication and designed to operate at speeds, and more importantly power levels, significantly better than other technologies. Should the manufacturability be realized, this technology could have a significant impact on high speed digital electronics

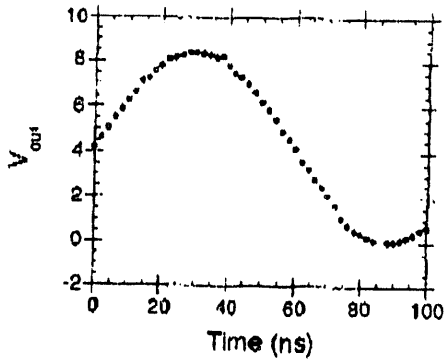


*Figure 8. Reconstruction of a sinusoid by the ADC coupled to a resistive DAC.*

## ACKNOWLEDGEMENTS

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