A General Purpose I_{DDQ} Measurement Circuit

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ABSTRACT

A relatively high-speed I_{DDQ} measurement circuit called QuiC-Mon is described. Depending upon IC settling times, upper measurement rates range from 50 kHz to 250 kHz at 100 nA resolution. It provides an inexpensive solution for fast, sensitive I_{DDQ} measurements in CMOS IC wafer probe or packaged part production testing.

INTRODUCTION

Static CMOS IC defect detection can often be accomplished efficiently by monitoring quiescent power-supply current (I_{DDQ}). Since CMOS ICs are designed to operate with low power consumption, abnormal currents often indicate an internal defect, design error, or fabrication error. I_{DDQ} testing has been used for many years by a number of companies and measurement techniques have taken several forms [1]. Off-chip I_{DDQ} sensors and associated circuitry are mounted either in the tester itself [2] or on the load board [3]. A Precision Measurement Unit (PMU) can make absolute value I_{DDQ} readings down to the nA level but at measurement rates from 10-50 Hz [4,5]. Commercial I_{DDQ} monitors make pass/fail limit readings at the 1 μ A level at test speeds near 15 kHz [6].

This paper describes a printed wiring board circuit called QuiC-Mon (for *Qui*escent *C*urrent *M*onitor) that provides a reliable, absolute, off-chip I_{DDQ} measurement at a test rate over an order of magnitude faster than previously reported at the 1 μ A level. This circuit is intended for companies entering the I_{DDQ} test practice who want higher speeds and lower sensitivities than typically available, at an affordable cost.

QuiC-Mon reports an eight-bit value that may be converted into an absolute current measurement. It uses the Keating-Meyer method of I_{DDQ} measurement, which floats the CMOS device under test (DUT) power supply

(V_{DD}) pin and monitors the rate of voltage decay [7]. This technique requires knowledge of the DUT V_{DD} pin capacitance (C_{DD}); QuiC-Mon makes independent C_{DD} measurements up to 4 nF in the same vector as the I_{DDQ} measurement. The I_{DDQ} range is programmable, but typically up to 25 μ A may be measured with the onboard analog-to-digital converter (ADC) for a target I_{DDQ} resolution of 100 nA. I_{DDQ} values that fall outside the measurement range are signaled by a overrange output from the ADC. Range can be doubled through ADC cascading.

Maximum test frequencies depend upon several factors, a primary one being the DUT power supply current (i_{DD}) transient settling time. Measurement rate also depends heavily on capacitance contributed by the DUT and load board. QuiC-Mon switches out most of the loadboard capacitance; however, C_{DD} may be designed into the IC to reduce transient noise. C_{DD} of the ICs evaluated here was between 1 and 4 nF. Higher capacitance environments in the μ F range slow I_{DDQ} measurement considerably, primarily because of RC time constants on the V_{DD} node introduced by QuiC-Mon. Despite these degradations, vector rates of over 250 kHz have been achieved on smaller VLSI devices with QuiC-Mon. Data on this is given later in the paper.

A brief review of I_{DDQ} concepts and currently available monitors is given with emphasis on the Keating-Meyer method used by QuiC-Mon. Then, details and design issues are discussed. QuiC-Mon's test results from two Sandia CMOS ICs are also shown. A circuit schematic of QuiC-Mon is included in the Appendix with operating characteristics and timing diagrams.

THEORY: I_{DDQ} Measurement Concepts

Normal, static CMOS ICs generate a large current transient during each change in logic state that can approach several amps. This is caused by the charging of internal and external node capacitance and the current

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through complementary n - and p -channel transistors during the transition phase. This current transient decays quickly and within a microsecond power supply current has usually settled to its quiescent level (I_{DDQ}). This "standby" current depends largely on the IC's transistor size and count, but is typically in the 1 to 100 nA range [1]. Most static CMOS defects, such as gate oxide shorts, interconnect bridges, and certain open-circuit defects, cause high I_{DDQ} states [3-5, 8-11], usually orders of magnitude higher than normal.

Measurement Techniques. Different instrumentation designs have been used to measure I_{DDQ} . Current viewing resistors are often limited in measurement accuracy and testing frequency. A diode-resistor method initially used at Sandia National Laboratories in 1976 had a low current limit of 50 μ A at a 10 kHz vector rate [3]. An op-amp circuit designed at Sandia used a virtual ground at the V_{SS} line and had a low current limit of around 15 μ A at a 100 kHz vector rate. The Bit-Current Option on the Advantest T3342 tester has a sensitivity of 1 μ A at about

15 kHz [6]. A good discussion of design issues with off-chip measurements is given by Crapuchettes [2].

The Keating-Meyer Method. Figure 1 contains a block diagram of the I_{DDQ} measurement technique first proposed by Keating and Meyer in 1987 [7]. During normal operation, the switch is closed, and the DUT draws current from the tester power supply (V_{TPS}). For an I_{DDQ} measurement, the switch is opened and the DUT is forced to draw its supply current from C_{DD} . If C_{DD} of the device is known, measuring the voltage drop ΔV after time Δt reveals I_{DDQ} as

$$I_{DDQ} = C_{DD} \frac{\Delta V}{\Delta t} \quad (1)$$

The power supply and load board capacitance, C_{LARGE} , are isolated from the floating V_{DD} node. Figure 2 illustrates typical waveforms of this circuit. Higher currents discharge the floating V_{DD} node more rapidly than low currents. C_{DD} must be measured or be known within acceptable tolerances to obtain an accurate I_{DDQ} measurement.

Figure 1. The Keating-Meyer I_{DDQ} Circuit [7].

IMPLEMENTATION: QuiC-Mon v3.2

QuiC-Mon v3.2 is the result of over two years of work at UNM in conjunction with Sandia National Laboratories. It is an order of magnitude faster and more accurate than QuiC-Mon v2.0 [12] and additionally performs measurements of I_{DDQ} and C_{DD} in the same vector period. The circuit block diagram is shown in Figure 3 with expanded elements and nomenclature required for the description. The Appendix gives a detailed circuit schematic.

Figure 2. Typical Keating-Meyer Waveforms.

Figure 3. Block diagram of QuiC-Mon.

Switch: Two parallel ADG221KN transmission gates (TGs) perform the function of the Keating-Meyer switch. The ADG221KN was selected for its low on-resistance (R_{TG} , $\sim 57 \Omega$), high off-state impedance, switching speed, and TTL logic interface. A 10Ω resistor (R_X) connects QuiC-Mon's internal V_{DD} node (V_{DDI}) and that of the DUT (V_{DD}) for amplifier stability. This makes the V_{TPS} to V_{DD} resistance about $10 + 57 \parallel 57 = 38.5 \Omega$. The TG switch remains closed during DUT input changes to prevent i_{DD} spikes from draining a floating V_{DD} node. To prevent potentially damaging resistive drops R_{TG} and R_X , two parallel 1N914B signal diodes (not shown) always connect V_{TPS} and V_{DD} .

DUT Capacitance: The lumped capacitance of the DUT (C_{DD}) consists of both internal (C_{DDI}) and external (C_{DDX}) components. Internal capacitance is the result of IC reverse-biased pn junctions and other factors discussed later. External capacitances include interconnect routing, tester channel electronics, and other parasitics that appear between QuiC-Mon and the DUT. This includes discrete capacitors placed on this node; these should be minimized as they slow down measurements. Discrete capacitors should be placed in parallel with C_{LARGE} so they will be isolated when the TG is opened.

Internal Capacitance: An additional capacitor (C_X , $\sim 0.0015 \mu F$) is added to QuiC-Mon's V_{DDI} node. This augments C_{DD} to prevent low-capacitance DUTs from causing large voltage drops on the floating node (1). Tester input V_{IMB} and capacitor C_{IMB} (30 pF) neutralize charge injection caused by transmission gate switching. Input V_{INJ} and capacitor C_{INJ} (22 pF) are used to measure C_{DD} (see next section). For calculations, all V_{DDI}

capacitances (C_X , C_{IMB} , C_{INJ} , and other parasitics) are combined into C_{INT} . The prototype board's C_{INT} was determined empirically to be 1.92 nF by monitoring voltage decay with a calibrated current load.

Amplifier network: A high-speed amplifier was constructed from fast-settling OP64GP op amps. It amplifies the difference between V_{TPS} and V_{DDI} and references it to ground for digital conversion. The precision amplifier gain (A) of 110 is controlled through components with 1% tolerance or better. A final stage OP260GP configured as a voltage follower clamps the voltage output (V_A) between $-0.7 V$ and $+1.9 V$. This is required to prevent damage to the ADC.

Flash ADC: V_A is quantized by an MC10319P eight-bit flash ADC within 4 ns of the sampling pulsc. An adjustable voltage regulator sets the ADC reference voltage to $+1.28 V$. ADC resolution (ρ) for 2^8 states is $\frac{1.28}{256} = 5 mV/bit$, or an effective V_{DDI} resolution of $\frac{\rho}{A} = 45.5 \mu V/bit$. The ADC's converted output D is

$$D = \frac{V_A}{\rho} = \frac{A}{\rho}(V_{TPS} - V_{DDI}) \quad (2)$$

TAKING MEASUREMENTS

Voltage Offset. Any current drawn from V_{DDI} generates an additive voltage drop across R_{TG} that affects all measurements. This amplified offset V_{AO} is

$$V_{AO} = A(I_{DDQ} + I_{AMP})R_{TG} \quad (3)$$

where I_{AMP} is the amplifier bias current, which is typically 300 nA for an OP64GP. This offset causes a dc shift in the measurement waveforms but does not alter their characteristics.

Measuring C_{DD} Per Vector. The physical basis for C_{DD} is the IC surface area of reverse biased pn junctions seen from the V_{DD} pin to the diffusion, well, and substrate regions. Capacitance across gate oxides and between IC metal and poly lines also contributes to C_{DD} . SSI ICs have a small number of internal nodes with a small C_{DD} . Changes in input state can create large relative variations in C_{DD} as p -channel transistors connect or disconnect junctions from the power rail. This was shown in [12], where an LCR bridge was used to measure SSI and MSI IC C_{DD} values during different logic states. ICs had as much as a 25% variation in C_{DD} from an all-high input state to an all-low input state.

Larger ICs have more complementary circuitry, so that while some nodes switch high, a roughly equivalent number are switching low. The small variations become swamped by the larger C_{DD} , so that capacitance can in some cases be assumed constant over the vector set. This was confirmed with C_{DD} measurements on larger ICs taken with QuiC-Mon (see Results section). However, other factors become more prevalent, such as the switching in or out of tester channel capacitance over a large number of output pins. Thus, a fast, simple way to measure C_{DD} in the same cycle as I_{DDQ} was sought in case of significant C_{DD} variations.

C_{DD} Measurement Technique. We initially considered using (1) as a means for measuring C_{DD} . If the tester provides an additional known current source to V_{DD} , C_{DD} can be calculated from the additional voltage drop. However, this technique degrades for high I_{DDQ} , particularly currents drawn by IC defects. Another problem is the magnitude of the additional current source required to achieve a satisfactory measurement resolution. We therefore used a charge-injection method based on a transient analysis of the V_{DD} node components. This allows C_{DD} to be measured in the same vector period as I_{DDQ} without severe penalty and solves both the resolution and I_{DDQ} dependence pitfalls. The Appendix illustrates timing waveforms associated with these measurements.

Figure 4 shows a simplified model of this technique. While the TG switch is closed, the tester applies a 5 V step to V_{INJ} . This injects about -110 pC of charge through C_{INJ} (22 pF) onto V_{DDI} . The V_{DDI} node voltage drops instantaneously. The initial amplified voltage excess

Figure 4. Simplified diagram of QuiC-Mon during C_{INJ} measurement.

$V_{A(INJ)}$ was estimated by using a capacitor voltage divider relation between C_{INJ} and other V_{DDI} node capacitances

$$V_{A(INJ)} = \alpha A \frac{V_{INJ} C_{INJ}}{C_{DD} + C_{INT}} \quad (4)$$

where C_{INT} encompasses the total V_{DDI} capacitance, including C_{INJ} . The effects of the R_{TG} and R_X pathway were accounted for by α , an empirically determined correction factor. Its value was 0.92 for the prototype board.

The V_{DDI} node returns exponentially to its equilibrium condition (the voltage offset described previously). The transient response depends on resistances R_{TG} and R_X as well as C_{DD} and C_{INT} . The node time constant is

$$\tau = \beta [R_{TG} C_{INT} + (R_{TG} + R_X) C_{DD}] \quad (5)$$

where β is an empirical constant required to compensate for slight changes in the time constant introduced by R_X . Its value was calculated through computer simulations to be 0.91.

After the capacitance time delay (t_{cdd}) to allow for amplifier settling and signal delays, the ADC samples the remaining excess voltage:

$$v_A(t_{MC}) = V_{AO} + V_{A(INJ)} e^{-\frac{t_{cdd} - t_{pda}}{\tau}} \quad (6)$$

where t_{pda} is the analog signal delay through the amplifier (about 135 ns). It is important to note that the only effect

that I_{DDQ} has on this measurement is in the voltage offset term, which represents only a dc shift in the response and does not affect its transient shape or characteristics. This was confirmed through numerous computer simulations and empirical data taken with several calibrated resistor current loads.

A typical measurement has $t_{cdd} = 300$ ns, a balance between resolution and amplifier settling. To ensure a monotonically increasing relationship between $v_A(t)$ and C_{DD} , $t_{cdd} - t_{pda}$ must be less than τ for the range of C_{DD} expected. In this region, the effects of α and β in (6) tend to nullify. Since (6) is transcendental in C_{DD} , a lookup table was used to translate ADC values into capacitance.

Measuring I_{DDQ} . I_{DDQ} is measured by opening the TG switch. As the DUT draws charge at a constant rate from V_{DD} (and V_{DDI}), V_A increases linearly. For typical I_{DDQ} measurements, the voltage drop in (1) is on the order of 10 mV; in this range, it is assumed that even resistive defect loads will be linear. After the discharge time (t_{iddq}) has elapsed, the amplifier output is

$$V_A = V_{AO} + A \frac{I_{DDQ} + I_{AMP}}{C_{DD} + C_{INT}} (t_{iddq} - t_{pd}) \quad (7)$$

where t_{pd} is the total propagation delay, encompassing the switch-off time of the transmission gate and the amplifier analog signal delay. Eqn. (7) can be converted to an I_{DDQ} calculation with (3)

$$I_{DDQ} = \frac{V_A}{A} \frac{(C_{DD} + C_{INT})}{t_{iddq} - t_{pd} + R_{TG}(C_{DD} + C_{INT})} - I_{AMP} \quad (8)$$

The discharge time t_{iddq} controls not only the speed of the measurement but its resolution. Longer time intervals allow for finer I_{DDQ} measurements at the expense of reduced range (see Results).

Current transient considerations. The IC i_{DD} transient following a change logic state must decay to I_{DDQ} before measurements start. Otherwise, measured I_{DDQ} will also include the remaining excess current, causing output values higher than the true value. Adequate time must be allotted so that excess current is less than the I_{DDQ} resolution desired. For smaller VLSI circuits ($C_{DD} < 2$ nF), a liberal settling time of 3 μ s guarantees this.

While most DUTs normally settle within 1 μ s, the V_{DD} time constant τ in (5) can extend settling time. For larger

VLSI DUTs, τ is larger, and more settling time must be allotted. While a large τ improves C_{DD} measurement by relaxing time constraints, it is the limiting factor in maximum vector frequency.

Parameter Variations: Amplifier offset voltage and R_{TG} vary with V_{TFS} . R_{TG} variations have significant impact on circuit measurements. These variations were characterized and are illustrated in the first page of the Appendix.

Charge injection: TG charge injection caused by switching must be monitored with an oscilloscope. The amplitude of the voltage step at V_{IMH} must correct charge imbalance.

Lead lengths: Lead lengths from QuiC-Mon to the DUT must be as short as possible. This became more important during wafer probing, where space constraints were more pronounced. It is crucial that QuiC-Mon be located as close to the DUT as possible so that incident noise is minimized.

Additional C_{DD} discreties: External discrete capacitances on V_{DD} should be kept to a minimum. Adding capacitance helps to control high-frequency switching problems, but QuiC-Mon runs proportionately slower (see Results).

CIRCUIT VERIFICATION

QuiC-Mon was initially characterized with a series of discrete capacitor and resistor loads. The timing specifications listed in the Appendix were derived from such loads. This also established the constants α and β in (4) and (5).

Parts from two Sandia CMOS IC designs were then evaluated. Both designs used the static CMOS design rule philosophy for I_{DDQ} testability. The Sandia SA3304 is an emulation of the National Semiconductor Timing and Control Unit (TCU) which is part of the 32C016 family of devices. It contains about 2,500 transistors. The Sandia SA3865 is an emulation of the Intel 80C51 microcontroller and contains about 78,700 transistors. I_{DDQ} results from each device tested with QuiC-Mon were evaluated against PMU-measured I_{DDQ} .

QuiC-Mon was interfaced to an Advantest T3342 tester with timing diagrams given in the Appendix. A sample of a functional vector set was measured at 200 kHz for the SA3304 and 100 kHz for the SA3865. The lower frequency for the SA3865 was required because of a

higher C_{DD} and to allow ample time for I/O settling. Both C_{DD} and I_{DDQ} were measured on the same cycle using double clocking, since the sampling clock on the ADC must be triggered twice in the same vector period. A comparison of the calculated I_{DDQ} against the PMU value allowed an estimate of C_{DD} measurement accuracy. I_{DDQ} discharge time (t_{iddq}) was 1350 ns and C_{DD} measurement delay (t_{cdd}) was 300 ns for all tests.

RESULTS

The circuit was reliable and accurate at high frequencies. Results also proved repeatable within expected noise tolerances. Samples over several parts showed Gaussian noise characteristics on both C_{DD} and I_{DDQ} measurements, indicating that amplified white noise was a significant factor in sampling error at 100 nA resolution.

C_{DD} Measurement. Figure shows the results of C_{DD} measurement on the SA3304. QuiC-Mon was able to detect a variation in C_{DD} due to 35 pF per tester channel connected to V_{DD} through output buffers when they were driven high. The columns show the number of outputs high during a vector state (left axis) while the line graph denotes average measured C_{DD} of nine parts. This variation could be eliminated if DUT outputs were open-circuited during I_{DDQ} measurements. When tester channel capacitance was subtracted out, C_{DD} variations between vectors were less than 50 pF, near the measurement noise margin.

Figure 5. SA3304 C_{DD} measurement results. Columns are number of outputs high; line is measured C_{DD} .

The SA3865 C_{DD} data displayed in Figure 6 show the average C_{DD} measured over 21 vectors for various values of V_{TPS} . Note the significant variation in part-to-part C_{DD} which is enough to warrant at least one C_{DD} measurement

Figure 6. Average C_{DD} of 9 SA3865 Packaged ICs over 21 I_{DDQ} vectors.

per IC. The expected inverse dependence on V_{TPS} of reverse biased pn junctions is evident. At higher values of C_{DD} , the resolution of the C_{DD} measurement increases, and noise variations become more significant. This was true on the SA3865, which showed larger percentage variations in measured C_{DD} than the SA3304. Wafer probe results at $V_{TPS} = 5$ V were similar to the packaged part with slightly more load board capacitance, as shown in Figure 7. The variations per vector of the SA3865 were about 3% of the average.

Figure 7. C_{DD} data on SA3865 wafer probe ICs. Points represent average over 20 die sites.

I_{DDQ} Measurement. For I_{DDQ} measurements, accuracy was defined by the difference between QuiC-Mon's results and those of the Advantest's PMU. Since QuiC-Mon I_{DDQ} results came from both a C_{DD} sample and an I_{DDQ} sample, results showed slightly more noise variation than individual samples. The SA3304 parts had a wide range of I_{DDQ} values from under 1 μ A to over 30 μ A; the SA3865 parts were well behaved with currents around 6.5

μA . Table 1 shows the results of I_{DDQ} measurements for packaged (P) and wafer (W) parts.

Table 1. I_{DDQ} results.

Part	V_{TFS}	Vectors	Error μ (nA)	Error σ (nA)
SA3304 (P)	4.5	300	21	215
SA3865 (P)	4.5	189	30	330
SA3865 (P)	5	189	-20	314
SA3865 (P)	5.5	189	1.7	324
SA3865 (W)	5	520	5	181

Figure 8 is the distribution of errors between QuiC-Mon and the PMU at the wafer probe level. Errors in I_{DDQ} measurements remained consistent over the measurable I_{DDQ} range. Table 2 shows vector-by-vector I_{DDQ} data taken from an SA3304 with a wide I_{DDQ} spread.

Figure 8. SA3865 Wafer I_{DDQ} Error Distribution.

Table 2. Sample SA3304 I_{DDQ} Data.

Vector	PMU (μA)	QuiC-Mon (μA)	Δ (μA)	Rel. Error
1	13.76	13.26	0.5	3.62%
2	8.26	8.2	0.06	0.68%
3	14.12	13.48	0.64	4.52%
4	8.16	8.16	0	0.06%
5	13.72	13.4	0.32	2.36%
6	6.79	7.05	-0.26	-3.81%
7	13.38	12.98	0.4	2.95%
8	10.12	10.28	-0.16	-1.56%
9	13.84	13.36	0.48	3.45%
10	8.36	8.44	-0.08	0.97%

Measurement Speeds. Figure 9 shows the I_{DDQ} measurement resolution in nA/bit for various values of

Figure 9. I_{DDQ} Measurement Resolution at $V_{TFS} = 5\text{ V}$.

C_{DD} and discharge times. Lower C_{DD} values allow better I_{DDQ} resolution in a shorter period of time.

Figure 10 shows the effect of total V_{DD} node capacitance for a 100 nA/bit current resolution. This shows that a discrete capacitor in parallel with C_{DD} to reduce $L\frac{di}{dt}$ switching transients requires that extra time be allotted for I_{DDQ} measurements. The frequency includes liberal transient settling time.

Figure 10. Maximum Vector Frequency vs. C_{DD} .

Cost. Most of the cost for the QuiC-Mon printed wiring board circuit occurred in development. Five copies of the low-volume prototype board were designed and manufactured for approximately \$1000 per board. Parts for each board totaled under \$100.

The additional cost for engineering labor to integrate QuiC-Mon into a test system must also be considered. This cost would be amortized over the volume of product tested. Development of a specialized load board would be more costly for a low-volume ASIC than for a high-volume production IC. Implementation of QuiC-Mon on an Advantest T3342 tester took about 20

man-hours. This included fixturing and checkout of the circuit with an oscilloscope.

FUTURE ENHANCEMENTS

QuiC-Mon v4.0 has recently been returned from PWB fabrication and will begin characterization in August. It has several improvements which should make it more user-friendly and more robust. These include:

- ☐ A derivative amplifier to eliminate timing sensitivity
- ☐ Removal of effects of offset voltage and TG charge injection
- ☐ Reduction in R_{π}
- ☐ ADC output internally converted to current
- ☐ C_{DD} measured by QuiC-Mon or user-entered
- ☐ User-selectable C_{DD} and I_{DDQ} ranges

CONCLUSION

This paper describes QuiC-Mon, a printed wiring board circuit capable of I_{DDQ} measurements to 100 nA resolution in the 50-250 kHz range. This circuit can perform an absolute value measurement of I_{DDQ} and C_{DD} in the same vector at both wafer probe and packaged part levels. This unique and inexpensive technique for I_{DDQ} measurement should appeal to companies desiring to incorporate I_{DDQ} testing to improve product reliability of CMOS ICs.

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Appendix

QuiC-Mon v3.2 Circuit Specifications

Parameter [†]	Symbol	Min	Typ [‡]	Max	Units
Analog Circuitry					
PWB power supply voltage	V_{PWB}	± 9	± 12	± 15	V
PWB power supply current	I_{PWB}	—	200	—	mA
Tester supply voltage	V_{TPS}	4	5	$V_{PWB} - 2.7$	V
External node resistance	R_X	—	10	—	W
TG charge injection	Q_{IMB}	-105	-90	-85	pC
ADC reference voltage	V_{REF}	1.26	1.28	1.3	V
ADC resolution	ρ	4.92	5	5.08	mV/bit
Amp. gain	A	109.5	110	110.5	V/V
Amp. input current	I_{AMP}	—	300	—	nA
Amp. power supply rejection	$PSRR$	—	95	—	dB
V_{DD} node capacitance	C_{INT}	—	1.92	—	nF
Digital I/O					
Input high-level voltage	V_{IH}	4.9	5	5.1	V
Input low-level voltage	V_{IL}	-0.1	0	0.1	V
Output high-level voltage	V_{OH}	2.4	3	—	V
Output low-level voltage	V_{OL}	—	0.35	0.4	V
VIMB step voltage	V_{IMB}	2.9	3.06	3.2	V
Timing Specifications					
Vector period	T	4000	5000	—	ns
Transient settling time	t_s	1000	2500	—	ns
C_{DD} measurement time	t_{cap}	300	900	—	ns
I_{DD} measurement time	t_{cur}	550	1350	—	ns
Pre-measurement recharge time	t_{rch}	100	100	—	ns
Amplifier analog signal delay	t_{pda}	—	135	—	ns
I_{DD} measurement prop delay	t_{pd}	—	210	—	ns
TG switch-on time	t_{on}	—	80	—	ns
C_{DD} measurement delay	t_{cdd}	250	300	400	ns
Sample clock to data valid	t_{dv}	—	19	—	ns
Minimum sample pulse width	t_{sw}	15	200	—	ns
I_{DD} measurement delay	t_{iddq}	500	1350	—	ns

[†] Parameters are measured at $V_{PWB} = \pm 12.0$ V for the prototype board unless otherwise specified.

[‡] Typical parameters are given for $V_{PWB} = \pm 12.0$ V and $V_{TPS} = +5.0$ V on the prototype board.

Figure A1. R_{TG} as a function of V_{TPS} and V_{PWB} .

Figure A2. Amplifier offset voltage as a function of V_{TPS} and V_{PWB} .

Figure A3. Typical QuiC-Mon timing waveforms.

QuiC-Mon v3.2 Circuit Schematic

Parts Listing

Designation	Nominal	Function
ICs		
U1	ADG221KN	TG Switch
U2, U3	OP64GP	Amplifier
U4	OP260GP	Clamping
U5	MC10319P	Flash ADC
U6	LM317T	Adjustable Regulator
U7	LM7805CT	+5 V Regulator
U8	LM7905CT	-5 V Regulator
Capacitors		
C1	0.0015 μ	C_s
C2	22 p	C_{sw}
C3	30 p	C_{cm}
C4	4.7 μ	Bypass
C5	22 μ	Bypass
C10-C20	10 μ	Bypass
C21	.1 μ	Bypass

Designation	Nominal	Function
Resistors		
R1	100, 1%	Amplifier Gain
R2, R3, R5	1.00K, 1%	Amplifier Gain
R4, R6	10.0K, 1%	Amplifier Gain
R7	2.0 K	Clamping Current Limiter
R8	2.7 K	Clamping Feedback
R10	10	R_s
R20	10 K	Amplifier Offset Null
R30	240	Voltage Adjust
R31	500	Voltage Adjust
Diodes		
D1-D6	1N914B	Clamping
Jumper		
JP1	—	Shorting of TG

A General Purpose /DDQ Measurement Circuit

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Presentation Outline

- **Introduction**
- **Implementation**
- **Quic-Mon Verification**
- **Future Enhancements**
- **Conclusions**

Purpose

- High-speed /DDR monitor
- Off-chip for flexibility
- Absolute measurements for data analysis
- Low-cost alternative

Introduction to Quic-Mon

- High speed off-chip monitor (100kHz typical)
- Absolute and pass/fail measurement
- Measures C_{DD} to 4 nF at 50 pF resolution
- Measures I_{DDQ} to 25 μ A at 100 nA resolution
- Measures C_{DD} and I_{DDQ} in 2 μ s

Keating-Meyer Method

Typical Waveforms

I_{DDQ}
CLOSED
SWITCH
OPEN

V_{DD}

V_O

NORMAL I_{DDQ} CYCLE

HIGH I_{DDQ} CYCLE

Quic-Mon v3.2

Measurement Procedure

- Switch DUT inputs
- Transient settling (1 to 5 μ s)
- Measure C_{DD} (800 ns)
- Measure I_{DDQ} (1400 ns)

What Contributes to C_{PD} ?

- pn junction capacitance
- Built-in V_{DD} capacitance
- External discrete capacitance
- Loadboard, routing capacitance

CG Measurement Techniques

100 Measurement Techniques

Putting it All Together

[illegible]

Verification on Advantest T3342

- Checked against Precision Measurement Unit (PMU)
- SA3304 Timing Control Unit (Packaged)
- SA3865 Microcontroller (Packaged & Wafer Probe)

C_{DD} Data: SA3304 Package

CDD Data: SA3865 Wafer Per Vector

C_{DD} Data: SA3865 Wafer Per Die Site

I_{DDQ} Error Spread: SA3865 Package

I_{DDQ} Error Spread: SA3865 Wafer

READINGS IN BIN

1000 Measurement Resolution ($V_{TPS} = 5\text{ V}$)

Maximum Vector Frequency

1000

100

10

1

1000

0.01

0.1

TOTAL V_{DS} CAPACITANCE (pF)

Future Enhancements: Quic-Mon v4.0

- Derivative amplifier
- Reduction in R_{TG}
- ADC output internally converted to current
- C_{DD} either board-measured or user-entered
- Selectable I_{DDQ} and C_{DD} ranges

Conclusions

- Inexpensive / DDC monitor
- Demonstrated speed, sensitivity
- Absolute measurements at pass/fail speeds
- Generic interface
- More robust, intelligent design in V4.0

DATE

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END