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Non-H_2Se, Ultra-Thin $CuInSe_2$ Devices

Annual Subcontract Report
10 November 1992 – 9 November 1993

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Section 1.0

SUMMARY

This report describes advances made during Phase II (Nov. 10, 1992 - Nov. 9, 1993) of a three-phase, cost-shared subcontract whose ultimate goal is the demonstration of thin film $CuInSe_2$ photovoltaic modules prepared by methods adaptable to safe, high yield, high volume manufacturing.

At the end of Phase I, EPV became one of the first groups to clear the 10% efficiency barrier for CIS cells prepared by non-H_2Se selenization. During Phase II a total area efficiency of 12.5% was achieved for a 1 cm^2 cell.

The key achievement of Phase II was the production of square foot CIS modules without the use of H_2Se. This is seen as a crucial step towards the commercialization of CIS. Using a novel interconnect technology, EPV delivered an 8.0% aperture area efficiency mini-module and a 6.2% aperture area efficiency 720 cm^2 module to NREL.

On the processing side, advances were made in precursor formation and the selenization profile, both of which contributed to higher quality CIS. The higher band gap quaternary chalcopyrite material $CuIn(S_x, Se_{1-x})_2$ was prepared and 8% cells were fabricated using this material.

Device analysis revealed a correlation between long wavelength quantum efficiency and the CIS Cu/In ratio. Temperature dependent studies highlighted the need for high V_{oc} devices to minimize the impact of the voltage drop at operating temperature. Numerical modeling of module performance was performed in order to identify the correct ZnO sheet resistance for modules.

Efforts in Phase III will focus on increase of module efficiency to 9-10%, initiation of an outdoor testing program, preparation of completely uniform CIS plates using second generation selenization equipment, and exploration of alternative precursors for CIS formation.

Note added in proof. Prior to the final preparation of this manuscript an EPV CIS module (163.4 cm^2) was measured by NREL at 9.1% aperture area efficiency.

Section 2.0

INTRODUCTION

This report describes advances made during Phase II (November 10, 1992 - November 9, 1993) of a three-phase, cost-shared subcontract entitled "Non-H_2Se, Ultra-Thin CIS Devices". The overall objective of this subcontract is the demonstration of large area, thin film $CuInSe_2$ photovoltaic modules using methods applicable to safe, high yield, high throughput manufacturing. Results obtained during Phase I of this project are described in an earlier publication and report [1,2].

Major developments have occurred during the last year or two in the area of thin film photovoltaics. Of note are the achievement of 15-16% conversion efficiency for both copper indium diselenide and cadmium telluride solar cells [3-6]. The largest modules based on these materials have achieved power densities of 102 W/m^2 (for 0.4 m^2 CIS) and 74 W/m^2 (for 0.72 m^2 CdTe) [7-9]. These advances are consistent with DOE projections for US photovoltaics in the year 1995 (as set forth in the Photovoltaic Program Plan, FY 1991 - FY 1995 [10]), namely for flat plate thin films, 15 - 18% laboratory cells and 8 - 10% commercial modules.

EPV is engaged in developing manufacturing technology for photovoltaic modules using CIS and other I - III - VI_2 absorbers. Under the NREL Polycrystalline Thin Films Task, EPV has conducted a research program on CIS to demonstrate the viability of a selenization approach to CIS module formation, but without the use of the toxic gas H_2Se. A further aim has been to develop novel interconnect technology in order to overcome some of the manufacturing hurdles that have hindered commercialization of CIS.

At the end of Phase I of this program (duration 8 months) EPV delivered to NREL a 1.47 cm^2 CIS cell with an active area efficiency of 10.5%, and a 5.6% 30 cm^2 module [2]. At the end of Phase II (duration 12 months) EPV delivered a 12.5% total area efficiency 1 cm^2 cell, an 8.0% aperture area efficiency 38 cm^2 module ($80W/m^2$), and a 6.2% aperture area efficiency 720 cm^2 module generating 4.5 W ($62 W/m^2$) [11,12].

The above cell results have comfortably cleared the 10% efficiency barrier for non-H_2Se selenization. EPV believes that efficiencies approaching 14% can be achieved using unalloyed CIS by further refinement of its existing process.

The new module technology embodied in the 8.0% module described above has yet to be fully exploited. More uniform CIS and reduced area loss will enable square foot plates generating 7W to be produced, scaling to 50W for 0.5 m x 1.25 m manufactured modules.

EPV's approach to material deposition relies on vacuum processing in order to control thickness, composition, and microstructure to the degree required for uniform, repeatable, high performance CIS. The bulk of our CIS has been produced by the selenization of appropriately formed Cu-In precursor layers using a process developed and refined by EPV [1,2,11]. Alternative vacuum-based approaches are also under investigation.

In common with several other leading CIS groups, EPV clearly recognizes the potential benefits of having the flexibility to incorporate into modules high quality alloys with bandgaps greater than that of $CuInSe_2$. Resulting from our efforts on $CuIn(Se,S)_2$ alloys, an 8% $1cm^2$ cell was delivered to NREL during Phase II.

Another line of research is directed towards sidestepping the Cd issue through the development of Cd-free junctions.

Single junction solar cells based on I-III-VI_2 materials have the potential to reach 18 - 20% efficiency, with individual PV parameters being V_{oc} 660mV, J_{sc} 36 mA/cm^2, FF 80%. This should allow manufactured modules to reach 14 - 15% aperture area efficiency.

Under this program EPV will continue to develop CIS technology and to understand the factors controlling module performance in order to define a commercially viable process capable of manufacturing power modules at 8 - 10% efficiency. In the future, drawing on both in-house research and that of other groups, EPV will strive to more closely approach the realistic limits of performance for I-III-VI_2 materials in both single and tandem junction configurations.

Section 3.0

ABSORBER DEVELOPMENT

Copper indium diselenide was prepared by selenization of Cu-In precursor layers. The substrates used are 1 ft^2 (929 cm^2) soda lime glass with a sputtered Mo back contact layer. The selenization is effected by evaporation of an elemental selenium source onto an appropriately prepared and annealed stack of sputtered Cu and In layers. The evaporation is conducted according to a specific Se flux versus time profile which in turn is a function of the chosen substrate temperature versus time profile. This process, the details of which must remain proprietary, was developed by EPV and has been steadily refined over time. It has been described in general terms in previous reports and publications [1,2,11].

3.1 Metals Deposition and Precursor Formation

The Mo, Cu and In layers are deposited under clean and reproducible conditions by magnetron sputtering in a load-locked, three target sputtering system. Without a load lock, lengthy presputtering of the In target would be required to remove the surface oxide that forms upon atmospheric exposure. The 1 ft^2 substrates are held vertically on a pallet and are transferred from the load lock chamber to the main chamber. Here the pallet carrier translates the substrate past the cathodes for metal deposition under chosen conditions of scan speed, discharge power, gas pressure and number of scans. Both RF and DC deposition modes are employed. The system is pumped by a closed-cycle helium cryogenic pump.

Cognizant of the relationship between film stress and sputtering gas pressure, we have adopted sputtering conditions for the Mo layer that lead to extremely adherent Mo films. As reported by Hoffman and Thornton, the average internal stress changes from compressive to tensile upon increase of argon sputtering pressure [13]. We have found that a gas pressure of 15 mTorr, for example, leads to adherent Mo films having a resistivity of 3.5×10^{-5} ohm cm (about 6x the resistivity of bulk Mo). More conductive films can be obtained at lower sputtering pressures owing to film densification.

The Cu and In layers are deposited in a stack and annealed prior to selenization in order to form the correct precursor layer. As we have previously reported, the Cu/In ratio must be held within a certain range in order to obtain the highest efficiency devices [2,11]. We have also found that device performance is influenced by the number, sequence, and thickness of the Cu and In layers and continue to update our standard recipe in this respect.

3.2 Refinement of Selenization Process

During the course of our research in Phase II it became clear that device performance and run repeatability are sensitive to the details of the selenization process. We will first analyze a particular selenization study because of the several conclusions drawn from it and consequently because of its pedagogic value. This study concerned very rapid ramping of the substrate temperature in order to simulate a high throughput manufacturing process. It should be said here that the selenization conditions employed in this rapid ramp study turned out to be inferior to EPV's standard process employed at that time. However, as will be described in Section 3.2.2, insights gained from this study subsequently allowed notable improvements to be made to the standard process.

3.2.1 Rapid Ramping of Substrate Temperature

In the rapid ramp study, extensive analysis (J-V, SR, microprobe, XRD, SEM) was performed on materials and devices resulting from a single 1 ft^2 precursor plate which was cut into 2" strips for different selenizations. Figure 1 shows the orientation of these strips relative to the direction of scan for sputtering. The precursor Cu/In ratio is reasonably constant across the scan direction of the plate, but is known to vary in the perpendicular direction. In the selenization experiments the substrate temperature was ramped at three times the usual rate. Under these conditions a dark band usually appeared near the middle of the CIS strips, which we believed to be indicative of a two phase region (CIS plus $Cu_{2-x}Se$). The dark band does not normally appear in our standard process.

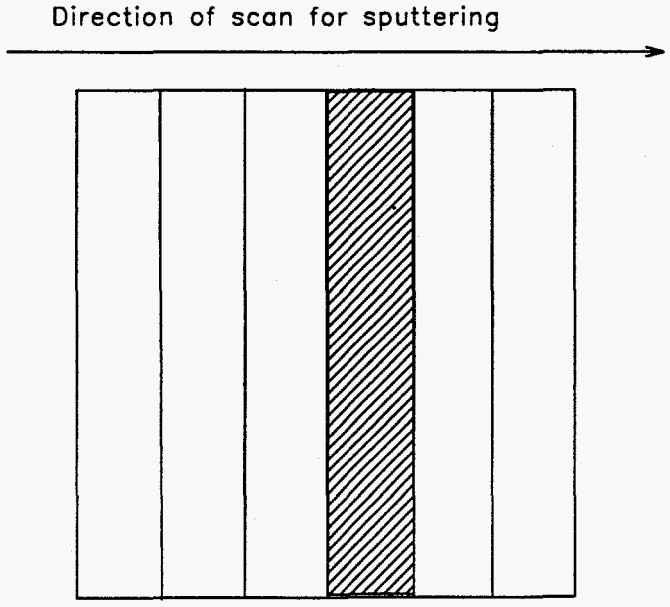

Fig. 1. Orientation of sections cut from a 1 ft^2 precursor plate for selenization experiments

From one of the selenized strips samples were cut at measured positions for microprobe analysis at NREL. One sample was also cut at a fixed distance from the top of the plate for all strips subjected to different selenizations. The microprobe data is shown in Table I. The Cu/In ratio as a function of position for one of the selenized strips is shown in Figure 2. These data correspond to the first 9 entries of Table I. The shaded region of Figure 1 represents the position of the darker band of CIS. In this region the Cu/In ratio is 1.00 - 1.01. Near the top and bottom edges of the strip, the Cu/In ratio fell as low as 0.73 - 0.75.

The second group of entries in Table I corresponds to the five selenizations of the remaining precursor strips. In particular, the last entry of this group corresponds to a selenization in which considerably more Se was evaporated prior to initiation of the temperature ramp. This led to a lower indium content and a significantly increased Se/In ratio, implying increased indium loss and a more favorable Cu/In ratio.

Table I. Composition as determined by microprobe analysis of CIS prepared with a high substrate temperature ramp rate (plate 3-11-2)

Distance from top (cm)	Cu (%)	In (%)	Se (%)	Cu/In	Se/Cu	Se/In	Thickness (um)
1.6	20.7	28.3	51.0	0.733	2.46	1.81	2.33
4	20.9	28.2	50.9	0.741	2.43	1.80	
7.6 (9)*	22.2	27.4	50.4	0.808	2.27	1.84	1.95
10.8	23.8	26.3	49.9	0.902	2.10	1.90	1.75
12.7 (8)*	25.7	25.6	48.7	1.000	1.89	1.90	1.77
17.8	25.8	25.6	48.6	1.010	1.88	1.90	
21	23.4	26.5	50.1	0.877	2.14	1.89	1.76
22.9	22.2	27.4	50.4	0.810	2.27	1.84	
27.9	21.1	28.2	50.7	0.750	2.40	1.80	
7.6	21.6	27.8	50.6	0.778	2.34	1.82	
7.6 (12)*	22.2	27.6	50.2	0.806	2.26	1.82	2.05
7.6	22.0	27.7	50.3	0.793	2.29	1.81	2.07
7.6	21.9	27.7	50.4	0.792	2.30	1.82	
7.6 (16)*	22.2	27.0	50.8	0.824	2.29	1.88	1.95

*numbers in parentheses refer to the XRD traces

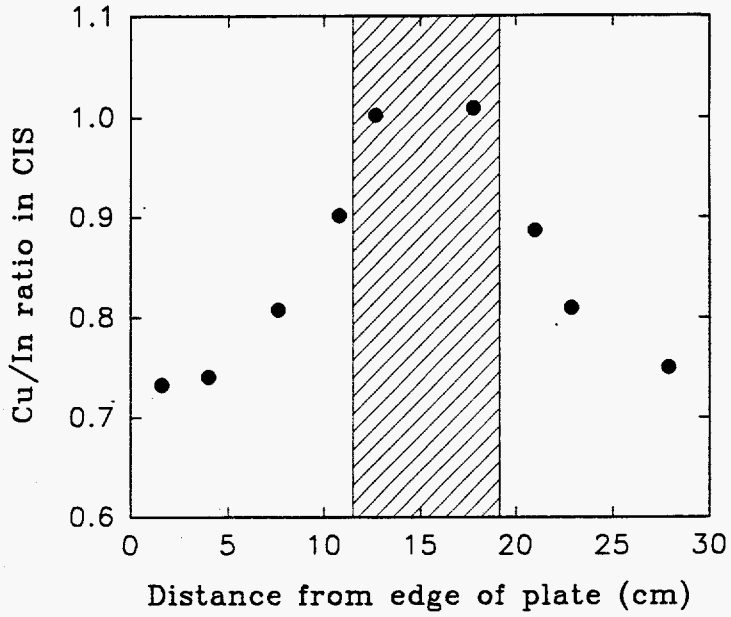

Fig. 2. Cu/In ratio for CIS on a 2" x 12" strip as a function of distance from the top edge of the strip (data for rapid ramp selenization).

Four samples in Table I were examined by X-ray diffraction at NREL. Very little difference was seen in the X-ray patterns (see Figure 3), except for the clear presence (as expected) of $Cu_{2-x}Se$ in sample 8 and its absence in sample 16.

The intensity of the (112) peak for sample 16 was half that of the other samples, possibly because of the absence of the $Cu_{2-x}Se$ phase which has a strong line at the same d-spacing.

The photovoltaic parameters of 1 cm^2 cells fabricated on the CIS adjacent to the areas analyzed by electron microprobe are shown in Figure 4. The data are plotted versus the Cu/In ratio, solid circles representing the first group of films in Table I (same selenization, different positions), and open circles the second group (same position, different selenizations). As reported in the Phase I Annual Report, the efficiency falls strongly for Cu/In values smaller than a certain value (see behavior of solid circles). Cells fabricated in the two phase region (Cu/In $\approx$ 1.0) also performed well below average, despite the KCN etch that was employed. Different selenizations also resulted in a spread in the Cu/In ratio, and considerable spread in device fill factor (see open circles).

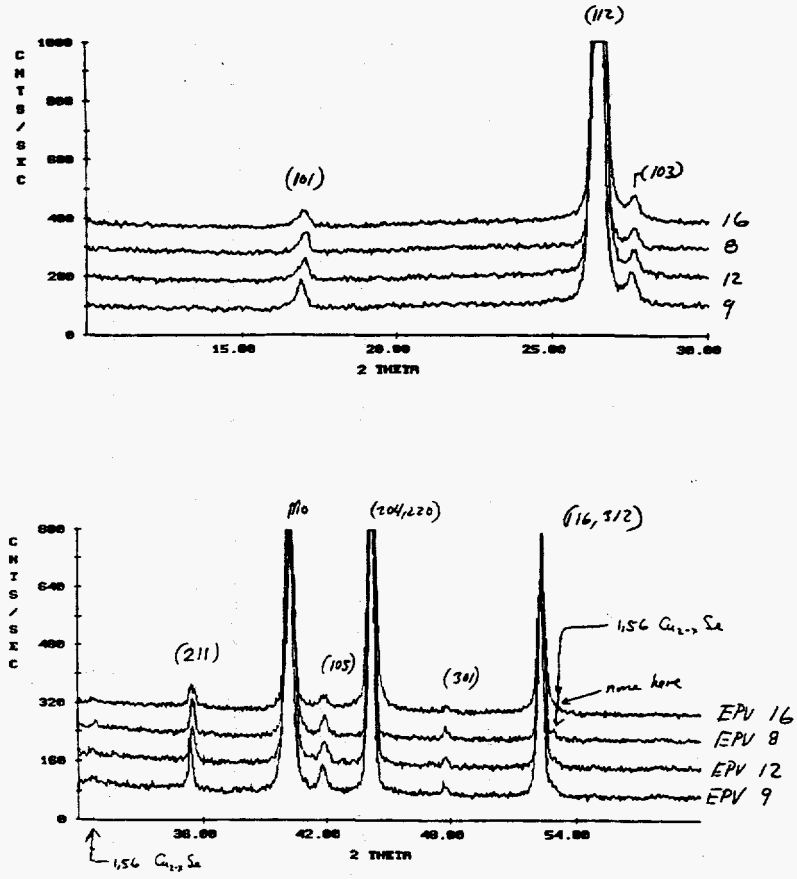

Fig. 3. X-ray diffraction spectra for 4 of the CIS samples listed in Table I.

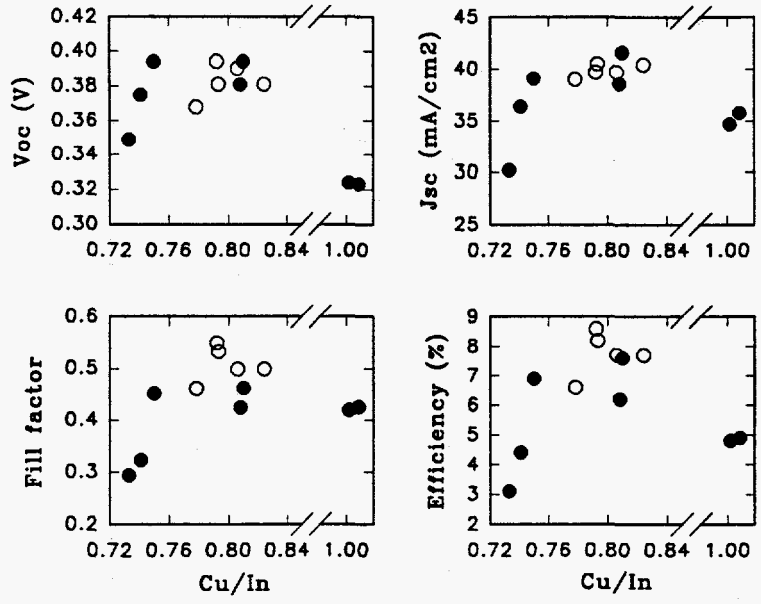

Fig. 4. Photovoltaic parameters of 1 cm^2 CIS cells fabricated adjacent to the areas analyzed by electron microprobe, and plotted versus Cu/In ratio.

Scanning electron micrographs of these films reveal considerable variation in both surface topography and fracture cross section. As the Cu/In ratio increases the film surface becomes rougher. For the film with Cu/In = 1.0 (5th entry in Table 1) deep holes could be seen at the surface together with faceted crystallites. For the 5th film in the second group in Table 1 (Cu/In = 0.824) an unusually smooth surface was apparent, as was a strong indication of columnar growth. This film was exposed to the most selenium early in the selenization.

These data indicate, in general, that the Cu/In ratio is not a unique determinant of cell performance (nor of CIS morphology), and that the particulars of the selenization must also be considered.

3.2.2 Improvement of the Standard Process

It was concluded from the rapid ramp study that the strong spatial variation of the CIS Cu/In ratio resulted from the spatial dependence of In loss on Se delivery rate and substrate temperature ramp rate. These and other experiments suggest that the Se flux must be properly adjusted to match the chosen temperature-time profile. In particular, a sufficient Se flux must be provided to effect the conversion of volatile In_2Se to nonvolatile InSe; see for example [14]. The required flux therefore depends on the substrate temperature ramp rate.

Re-optimization of the selenization process was facilitated by changes made to both hardware and software. Longer heating lamps were installed in the selenization chamber, leading to a more uniform substrate temperature distribution and improved CIS uniformity. More importantly, variations in device performance from run to run were traced to irreproducibility in the selenization step. This realization led us to introduce a new method of process control. As a result, precise adherence of actual substrate and selenium source temperature profiles to those programmed can be obtained. This degree of control allowed us to empirically optimize the Se flux profile based on reliable device performance data. The updated selenization process has resulted in notably improved CIS quality and uniformity.

Compositional data for a 10% efficient CIS cell as determined by EPMA after removal of the ZnO and CdS layers is shown in Table II. The composition is much closer to stoichiometry than the In-rich nature reported for most earlier films [1]. The uniformity of the CIS has been studies using V_{oc} maps for 1 cm^2 devices fabricated across the full width of 1 ft^2 plates. Such maps lie wholly above 410 mV, indicating a reasonable degree of uniformity.

Table II. Compositional analysis of CIS and CISS devices (in atomic %)

Cell material	Cu	In	Se	S
$CuInSe_2$	24.6	25.4	50	-
$CuIn(Se_{1-x}S_x)_2$	25.6	25.2	24.3	24.9

3.3 Higher Bandgap Alloys Using Sulfur

It may be possible to realize several commercial advantages through the development of I-III-VI_2 materials having a band gap larger than that of $CuInSe_2$. For example, although CIS cells are efficient and stable, their high current density means that a large number of cells per unit length must be employed in modules in order to limit resistive losses in the zinc oxide. Thus, it would be desirable to utilize wider bandgap I-III-VI_2 alloys in modules so that the cells generate a higher voltage and lower current. The resulting increase in optimum cell width then leads to smaller area losses and shorter patterning times. The use of such alloys would also bring the bandgap of the absorber closer to the optimum value for solar cells, which is calculated to be in the range 1.4 - 1.5 eV for homogeneous absorbers (see Figure 5). The use of graded bandgap [15] or notch structures [16] may also be beneficial.

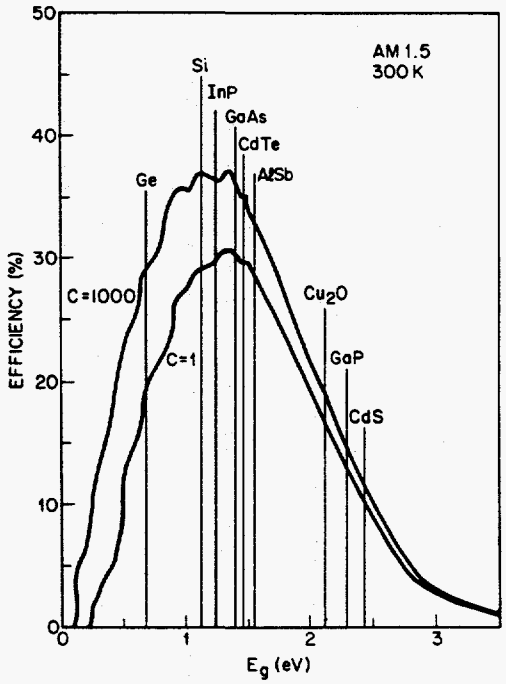

Fig. 5. Ideal solar cell efficiency versus band gap (after Sze)

Some of the chalcopyrite structure compounds are listed in Figure 6. The most commonly employed substitutions are gallium for indium and sulfur for selenium. Thus $CuGaSe_2$ has a bandgap in the range 1.67 - 1.70 eV, and $CuInS_2$ a bandgap in the range of 1.5 - 1.55 eV. Historically, most alloying has been conducted using Ga, and it is significant that Stolt et al. deliberately codeposit a low concentration of Ga (~ 0.1 %) even in unalloyed $CuInSe_2$ [17]. Promising solar cell results were reported by Walter et al. for CuIn $(S, Se)_2$, namely V_{oc} 613 mV, J_{sc} 33.5 mA/cm^2, FF 74%, active area efficiency 15.2% [18]. A transition from defect chalcopyrite to the presence of a spinel structure was observed at S/(S + Se) = 0.55 [19]. Later work demonstrated a 10.2% efficient $CuInS_2$ cell by employing a cyanide treatment of Cu-rich $CuInS_2$ to remove a CuS (covellite) secondary phase, the cell parameters being 697 mV, 21.5 mA/cm^2, 69% FF [20]. In $Cu(In, Ga)Se_2$ films the presence of a copper selenide secondary phase was found to increase the interdiffusion of indium and gallium by between one and two orders of magnitude [21].

At EPV we have produced chalcopyrite $CuIn(Se, S)_2$ alloys by co-evaporation of sulfur and selenium onto Cu/In precursor layers. As described later in section 4.4, CISS cells were fabricated using this material. The composition of the best cell had roughly equal atomic concentrations of all four elements (Cu/In/Se/S = 25.6%/25.2%/24.3%/24.9%) as indicated in Table II above.

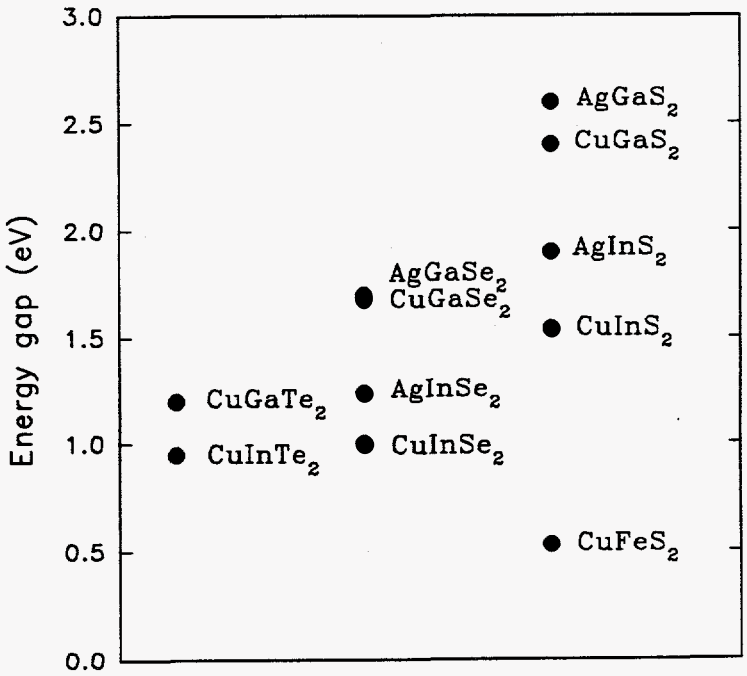

Fig. 6. Energy gap of various chalcopyrite semiconductors

Section 4.0

DEVICE RESULTS

The standard device structure employed by EPV is soda lime glass / Mo / $CuInSe_2$ / CdS/ZnO. Both evaporation and chemical bath deposition have been employed for the CdS layer [2]. Most of the devices reported here used CBD CdS at a deposition rate of 80 A/min. The ZnO was prepared by magnetron sputtering in a high resistivity/low resistivity bilayer configuration. The low resistance layer consists of ZnO:Al.

4.1 Effect of Cu/In Ratio

A series of devices was prepared using precursors spanning a range of Cu/In ratios. This was accomplished by using identical Cu sublayers and varying the thickness of the In sublayers. Following device measurements, the films were analyzed by electron microprobe. As shown in Figure 7, an approximate plateau in conversion efficiency was found for Cu/In ratios lying between 0.89 and 0.83, with a strong decline in efficiency for ratios in the range 0.83 to 0.74. A steep fall in fill factor (most probably due to rising CIS resistivity) is clearly a major factor in the decline of efficiency. From this study we learned that a ± 6% variation in precursor Cu/In ratio results in a ± 3% variation in cell efficiency in the plateau region. In other words, the EPV process is tolerant of small changes in precursor Cu/In ratio.

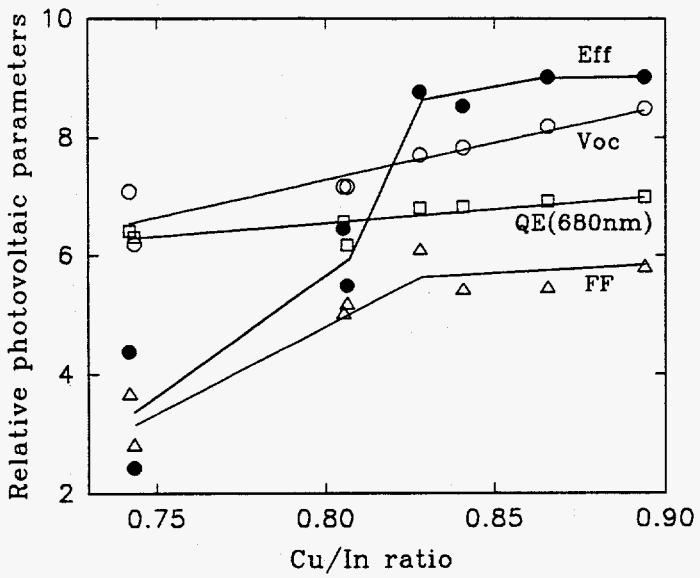

Fig. 7. Photovoltaic parameters versus Cu/In ratio of the CIS

The dependence of J_{sc} on Cu/In ratio was not investigated directly because of the usual uncertainty in estimating active areas. Rather, a fixed monochromatic beam of light

that fell wholly within the active area was used for all cells to determine QE (680 nm). This showed a slight decline for decreasing Cu/In (see Figure 7).

Following this result, we explored the range of spectral response curves that can be obtained from cells with different CIS quality. As a general observation we found that variations in the infrared response account for most of the differences in J_{sc} from cell to cell. For example, at 1150 nm we found that quantum efficiencies can range from 0.45 to 0.80. A plot of J_{sc} versus QE (1150 nm) was found to be roughly linear (see Figure 8), the relation being:

$$\text{active area } J_{sc}\ (\text{mA/cm}^2) = 20.0 + 0.25 \times \text{QE (1150 nm)\%} \qquad [1]$$

The variation in blue response (400-500nm) due to differences in CdS thickness was found to be a much smaller effect as far as accounting for differences in J_{sc}.

We also found that the long wavelength quantum efficiency declines as the measured Cu/In ratio of the CIS declines. Some of this data is shown in Figure 9. A few exceptions to this ranking indicate that another factor is relevant. We now have evidence that this factor is controlled by the selenization conditions. The reduced quantum efficiency in the range 550 - 850nm for the grossly indium rich device of Figure 9 may be indicative of hole transport limitation in the surface region of an n-type ordered vacancy compound/p-type CIS heterojunction (see, for example [22]), or may indicate the presence of indium selenide.

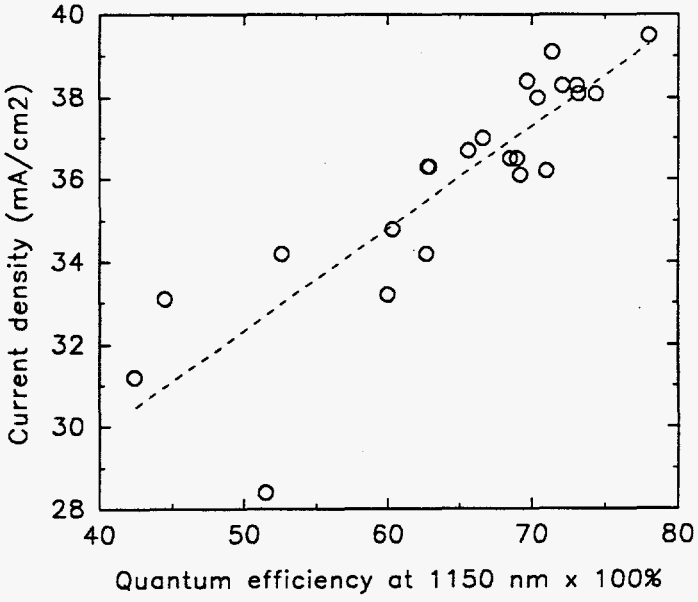

Fig. 8. Correlation of cell short-circuit current density and red response (characterized by QE at 1150 nm)

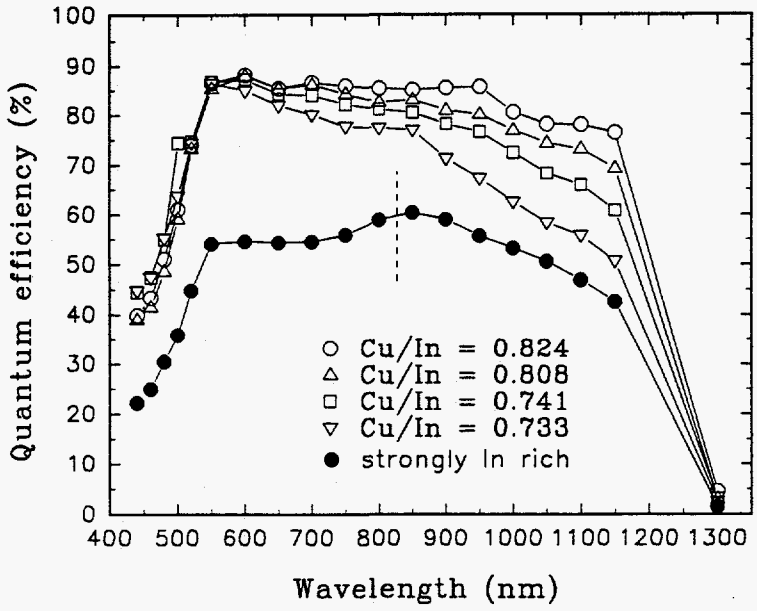

Fig. 9. Spectral response of CIS cells with various Cu/In ratios

4.2 Light Soaking Effects

We have noticed that some CIS cells, especially those with low initial fill factors (and probably In-rich), improve upon light soaking. The main effect is an increase in fill factor. Table III quantifies some of our observations on one of the cells that most strongly exhibited this effect. We find that the rate of improvement is dependent on bias condition. The experiments were mostly conducted in order of increasing light soak dose, with room temperature relaxation of the FF before each experiment. In the relaxed state a series resistance of 4.2 ohm cm^2 was deduced from I-V data, while after a 2 minute, 1 sun, o.c. soak the Rs was 3.1 ohm cm^2. It was also discovered that the low light intensity (0.1 sun) fill factor remained roughly constant at 62% and improved only slightly upon light soaking even though the 1 sun fill factor could be substantially improved by light soaking. This suggests that the light soaking does not affect the junction but rather decreases the series resistance of the cell, perhaps by shifting the bulk Fermi [11].

Table III. Influence of intensity, time, and bias on light soaking of certain CIS devices (I-V measurements at 1 sun)

Soak conditions: 30s, open circuit, variable intensity

Intensity (suns):	0.0	0.1	0.5	1.0	2.0
Fill factor (%):	42.9	43.1	43.9	47.7	51.6

Soak conditions: 1 sun, open circuit, variable time

Time (mins):	0.0	0.5	1.0	1.5	2.0
Fill factor (%):	42.9	47.7	51.5	53.1	54.4

Soak conditions: 1 sun, 1.5 mins, variable cell bias

Bias voltage (V):	-1.00	-0.60	0.00	0.41	0.70
Fill factor (%):	50.4	51.1	52.1	53.1	55.3

4.3 Device Analysis and Temperature - Dependent Studies

The basic device parameters V_b, n, J_o, J_{oo}, R and G may be determined from illuminated J-V measurements and $V_{oc}(T)$ measurements as follows. The J-V characteristic is assumed to be of the form $J=J_o \exp [(V-JR)/V_o] - J_L + GV$ where $V_o = nkT/q$, $J_o = J_{oo} \exp (-qV_b / nkT)$, from which it follows

$$V_{oc} = V_b + nkT/q \ln (J_L/J_{oo}) \qquad [2]$$

and, for G = 0

$$dV/dJ = R + V_o/(J + J_L) \qquad [3]$$

We define the light forward current as $J + J_L$, where $J_L > 0$, $J < 0$ for $V < V_{oc}$. The influence of series resistance means that correct n values cannot be deduced from a simple log plot of $J + J_L$ versus V, but must be obtained by computing dV/dJ and plotting it versus $1/(J + J_L)$. Typical R and n values for EPV cells deduced in this way generally lie between 0.5 - 1.0 ohm cm^2 and 1.40 - 1.75, respectively. Figure 10, for example, shows a plot of dV/dJ versus $1/(J + J_L)$ for an 11% efficient cell. For this cell R = 0.73 ohm cm^2, G = $1 \cdot 10^{-3}$ mho/cm^2, and n = 1.67.

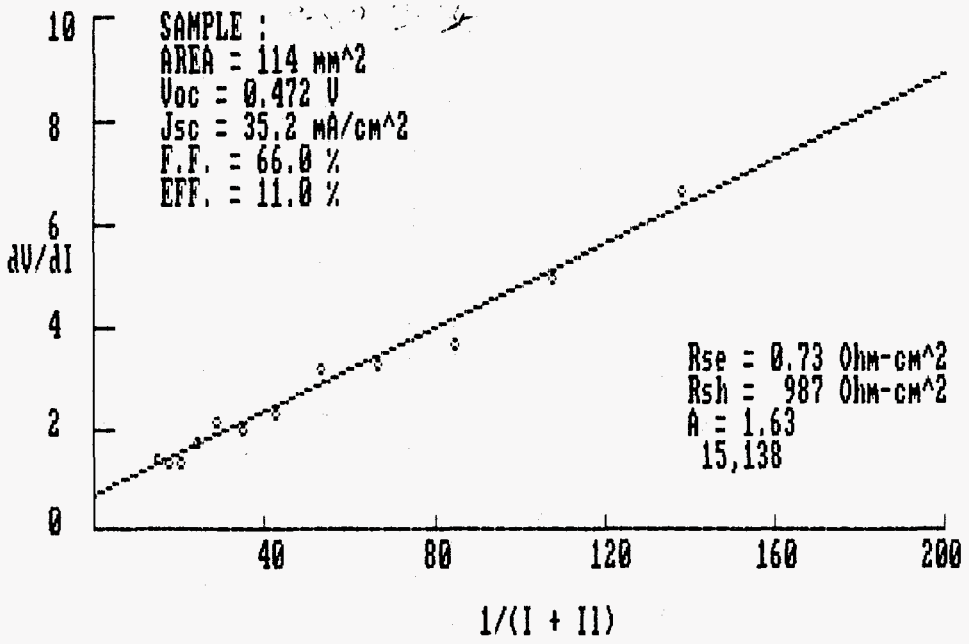

Fig. 10 Plot of dV/dJ versus $1/(J + J_L)$ to determine cell series resistance and diode factor.

Figure 11 shows the statistical dependence of measured PV conversion efficiency on diode quality factor n. The data base contains results on 725 cells. Quality factors outside the range 1.4 to 1.8 appear to depress the cell efficiency. Inspection of plots of individual PV parameters versus n revealed that V_{oc} and J_{sc} were anti-correlated, with V_{oc} increasing for smaller n values. The anti-correlation could result from variation of the space charge width with doping, i.e. higher doping resulting in higher V_{oc}, but also in a narrower depletion region and lower J_{sc}.

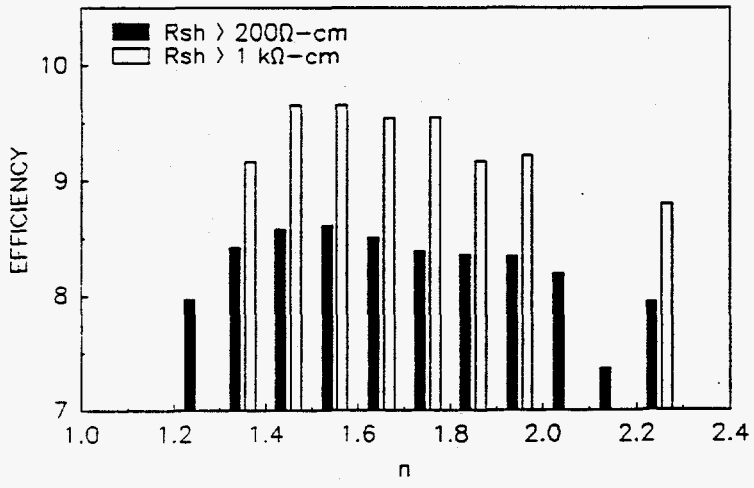

Fig. 11. Average cell efficiency versus diode factor n

Figure 12 shows a plot of V_{oc} (0.26 sun) versus T for a low leakage CIS device using chemical bath deposited CdS. For temperatures between 60°C and -93°C this plot is exactly linear, as predicted by the equation above, and extrapolates to a T = 0 intercept (built-in voltage V_b) of 1.07 V. This is slightly larger than the bandgap of CIS. Other CdS/CIS cells have yielded a V_b closer to 1.00 eV, and further work is necessary to determine the origin of this difference and whether slight cell leakage depresses the measured value of V_b. It is of interest that a Cd - free CIS cell also exhibited a barrier height of 1.0 eV (Figure 13).

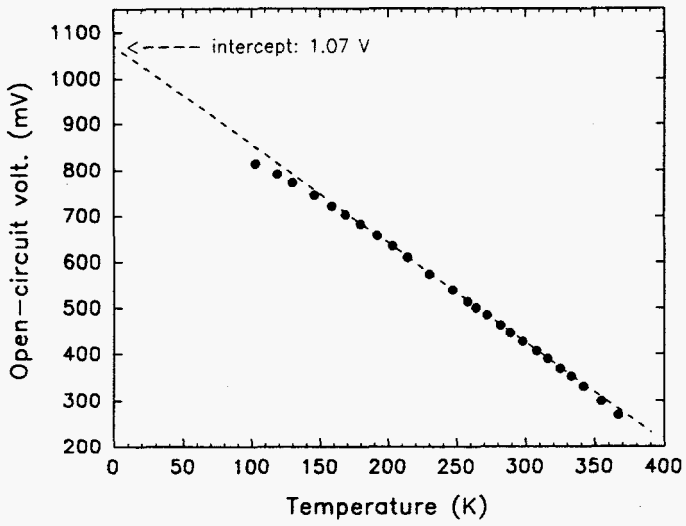

Fig. 12. Open-circuit voltage versus temperature (at a light intensity of 0.26 sun) for a CIS cell with CBD CdS

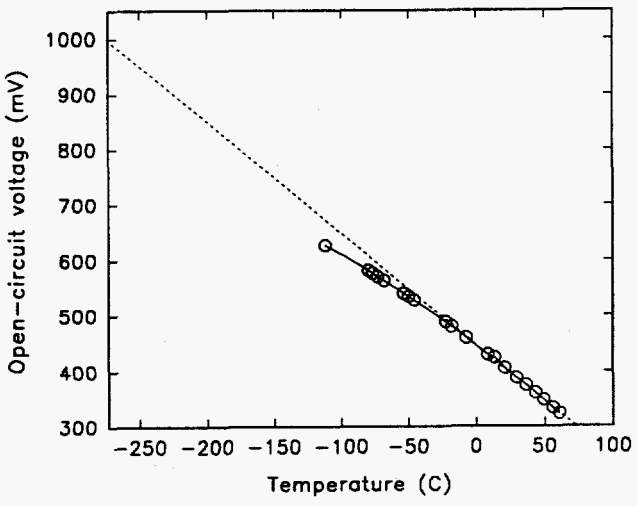

Fig. 13. Open-circuit voltage versus temperature for a Cd-free CIS cell

By measuring V_{oc} versus T at two different intensities, corresponding to light generated currents J_{L1} and J_{L2}, the measured slopes m_1 and m_2 can be used to determine the

diode quality factor n from the equation $m_1 - m_2 = n(k/q) \ln (J_{L1}/J_{L2})$. Using a different cell, the following slopes (mV/°K) were determined from V_{oc} versus T plots: -1.924 at 1 sun, -2.125 at 0.229 sun, and -2.320 at 0.0557 sun. These yield an n value of 1.59, and from the equations above J_{oo} = 33,700 A/cm^2. Thus, measurement of V_{oc} (T) at different intensities permits the determination of the basic diode parameters V_b, n, and J_{oo}.

We have also studied the temperature dependence of the 1 sun photovoltaic parameters for CIS cells. Figure 14 shows the behavior of V_{oc}, FF, and J_{sc}, and Figure 15 the temperature dependence of the conversion efficiency. In many cells a linear increase in FF is observed as the temperature is lowered from 115°C to 60°C. Below this temperature the FF falls below the extrapolated linear increase, saturates, and eventually declines. The deviation from linear behavior is mainly attributed to a nonlinear current limiting element in series with the main CIS junction. This current limitation is manifested in the low temperature I-V curve as a roll over in the first quadrant. Possible candidates for this oppositely-oriented barrier include the CdS/CIS and CIS/Mo junctions, or even potential barriers at CIS grain boundaries.

As shown in Figure 15, the cell of Figure 14 operated with conversion efficiencies ranging from 3% at 125°C to 16.2% at -150°C. The strongest factor contributing to this behavior is the high percentage change in V_{oc} with temperature. This is another argument in favor of higher V_{oc} devices, for which a given temperature coefficient dV_{oc}/dT will result in smaller percentage changes at elevated operating temperatures.

For the Cd-free device of Figure 13, a conversion efficiency of 18.4% was obtained at 157°K, the V_{oc} being 639 mV at this temperature. The I-V curve is shown in Figure 16. Figure 17 shows the dependence of fill factor on temperature for this cell.

A preliminary study of the temperature dependence of the bulk CIS conductivity (conducted on a Au/CIS/Mo sandwich structure) revealed an activation energy of 0.23 eV [11].

4.4 CISS Cells

The spectral response of $CuIn(Se,S)_2$ cells with 25% sulfur concentration is shown in Figure 18 (dashed curve). The bandgap is widened by about 0.15 eV relative to CIS (solid curve). We have also measured the temperature dependence of V_{oc} (in a manner analogous to Figure 12, but at 1 sun intensity) for CISS cells. We find dV_{oc}/dT = -2.26 mV/°C and an intercept at absolute zero of 1.20 eV (diode barrier height). Table IV summarizes our findings for CIS and CISS cells. As well as being advantageous in terms of wider cells and reduced area loss, the higher gap material possesses a further small advantage in terms of a reduced $(1/V_{oc})\, dV_{oc}/dT$.

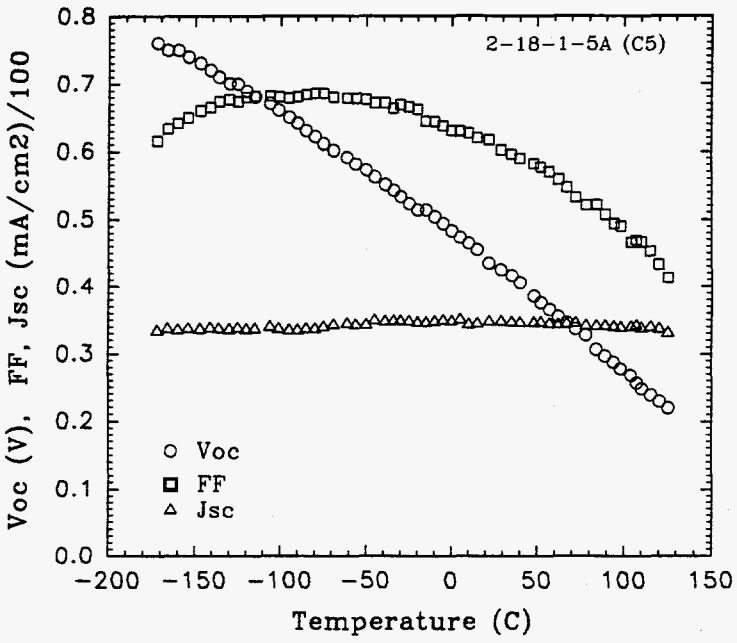

Fig. 14. Open-circuit voltage, fill factor, and short-circuit current density of a CIS cell versus operating temperature.

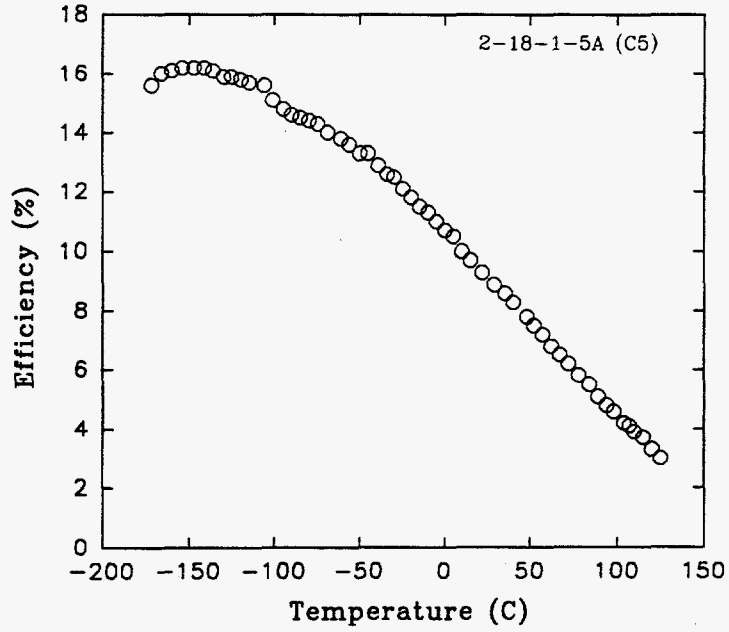

Fig. 15. Conversion efficiency of a CIS cell versus operating temperature

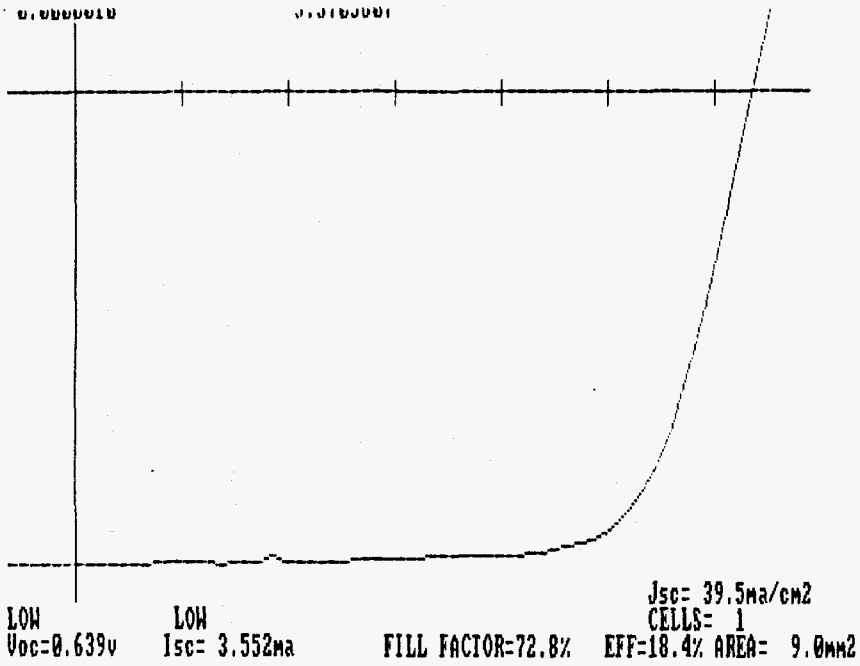

Fig. 16. J-V curve for a Cd-free CIS cell operated at -116°C (conversion efficiency 18.4%)

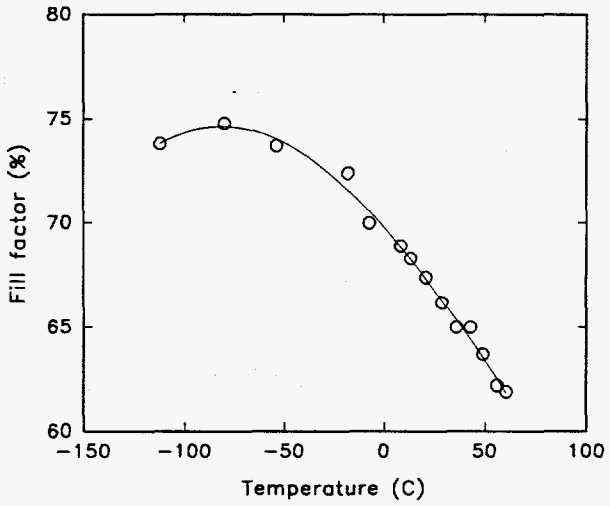

Fig. 17. Fill factor versus temperature for the Cd-free cell of Fig. 16.

Table IV. Temperature dependence of V_{oc} for $CuInSe_2$ and $CuIn(Se,S)_2$.

	$CuInSe_2$	$CuIn(Se, S)_2$
V_{oc}(RT) (mV)	430	550
dV_{oc}/dT (mV/°C)	-1.97	-2.26
$(1/V_{oc})dV_{oc}/dT$ (/°C)	-0.0046	-0.0040
% loss V_{oc} (% / 10°C)	4.6	4.0

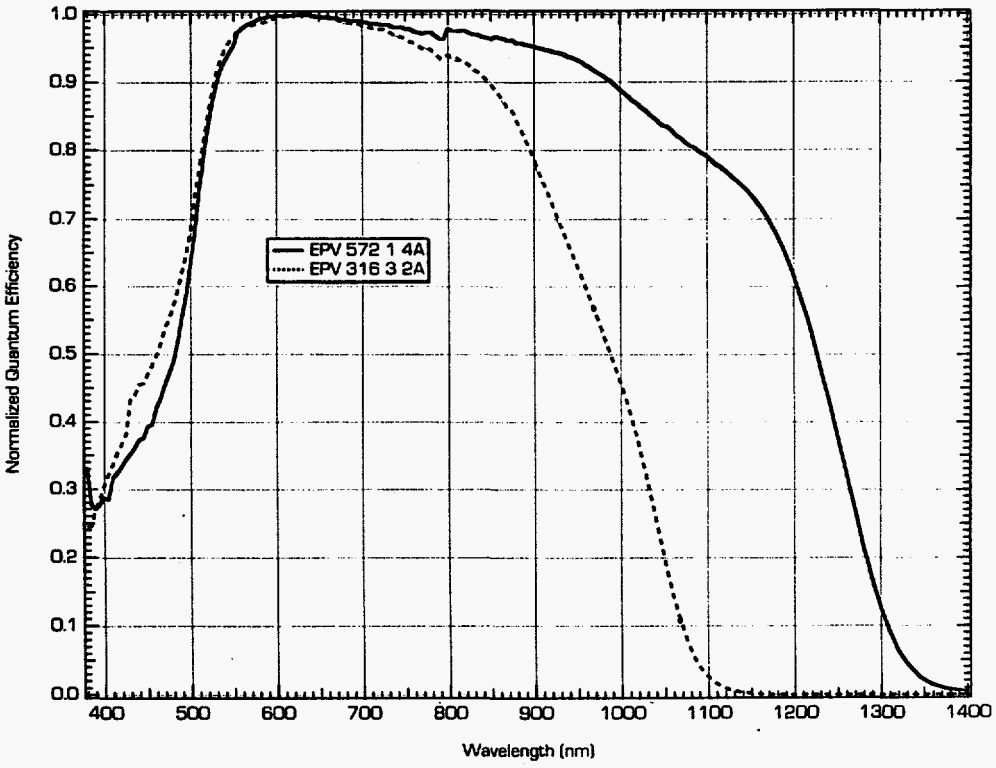

Fig. 18. Normalized quantum efficiency versus wavelength for CIS and CISS cells

4.5 Summary of Cell Results

Table V summarizes some of the cell results obtained by EPV. The parameters of the first three entries in this table (CISS, CIS, and Cd-free CIS cells) were measured under standard reporting conditions, while the last entry represents the performance of the Cd-free cell at 157°K. At this temperature the parameters of the cell were V_{oc} = 639mV, J_{sc} = 39.5 mA/cm^2, FF = 72.8%, efficiency 18.4%. A much greater effort has so far been expended in developing unalloyed CIS than the wider gap material CISS. Figure 19 shows the I-V curve for a gridless CIS cell prepared by application of suitable contacts to one cell of a completed mini-module. Evaporated AlF_3 was applied as an anti-reflection coating. A total area efficiency of 11.8 % was measured by NREL, with a V_{oc} of 485 mV, J_{sc} of 37.2 mA/cm^2 and fill factor of 65.6%.

Table V. PV parameters for CISS, CIS and Cd-free CIS cells

Material	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Area cm^2	Efficiency (%)	Comments
CISS	555	25.6	56.1	1.16	8.0	grid, no A/R
CIS	490	37.7	67.6	1.00	12.5	gridless, A/R
CIS, Cd-free	413	37.0	67.2	0.11	10.3	no A/R

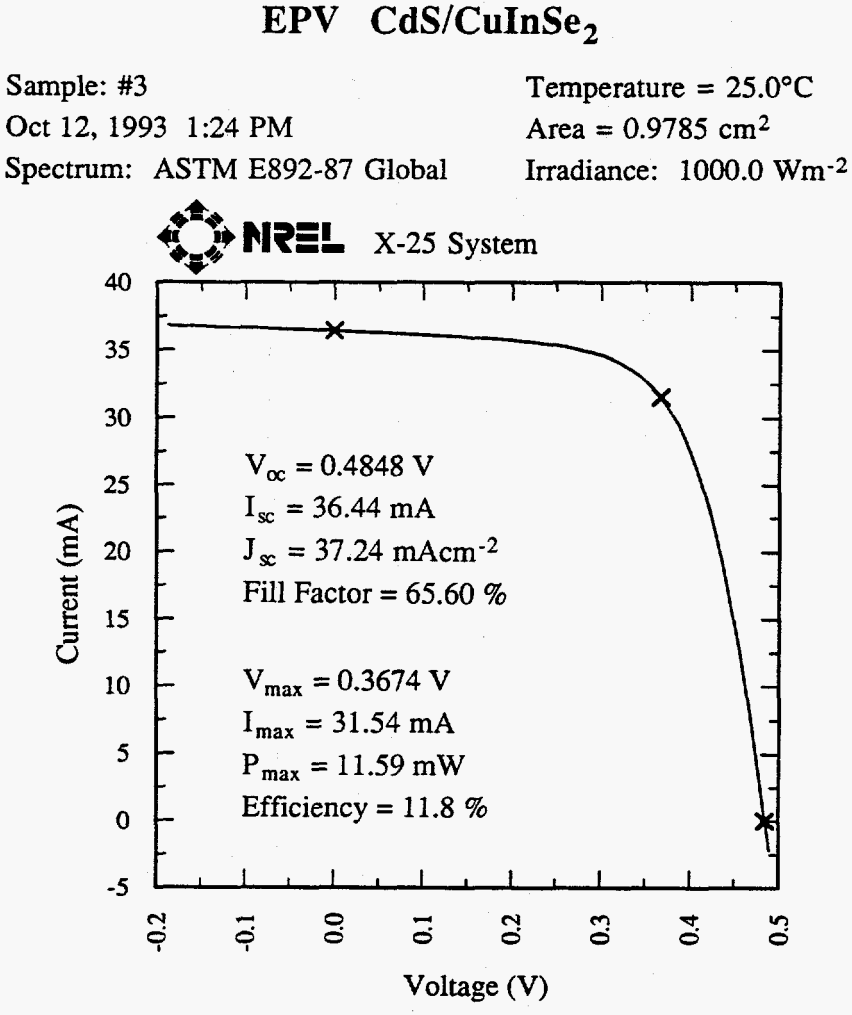

Fig. 19. I-V curve for a gridless 11.8% CIS cell

4.6 Available Current Density and Cd-free Cells

It is of interest to estimate the contributions to the short - circuit current originating from various regions of the solar spectrum. Using the ASTM E892 global reference spectrum (normalized to 100 mW/cm^2 and shown in Figure 20) we have calculated the available current density (assuming 1 electron per photon) in the wavelength ranges indicated in Table VI. Multiplying by an average quantum efficiency for CIS cells yields the current contributions as indicated.

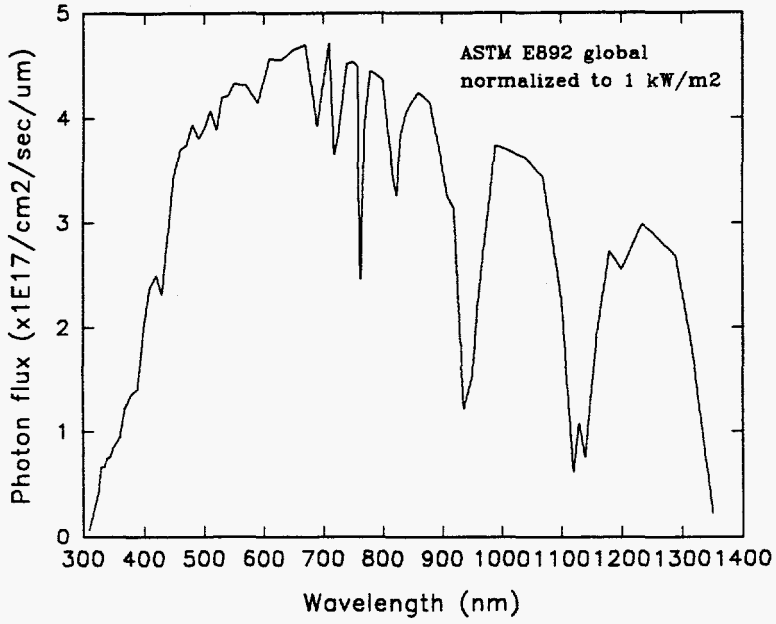

Fig. 20. ASTM E892 global solar photon flux versus wavelength

Table VI. Available current density and typical current contribution from a CIS cell (no A/R coating) in various wavelength ranges.

Wavelength Range(nm)	Available current density (mA/cm^2)	Typical CIS QE (av.)	Current contribution (mA/cm^2)
360 - 400	0.88	0.46	0.40
400 - 500	5.07	0.56	2.84
500 - 600	6.69	0.77	5.15
600 - 700	7.17	0.81	5.81
700 - 800	6.70	0.81	5.43
800 - 900	6.33	0.81	5.13
900 - 1000	4.25	0.81	3.44
1000 - 1100	5.41	0.75	4.06
1100 - 1200	2.78	0.64	1.78
1200 - 1300	4.45	0.33	1.47
	49.73		35.51

The standard device structure employed by EPV is soda lime glass/Mo/$CuInSe_2$/CdS/ZnO. Although the amount of Cd in a module employing this device structure is very small (about 0.001% by weight) and is fully contained within the lamination, EPV nevertheless considers it highly desirable to eliminate Cd entirely. The substitution of a wide gap, transparent heterojunction partner in place of the CdS could also improve J_{SC} by an amount whose upper limit can be estimated as follows. By setting QE = 0.81 in Table VI for all wavelengths less than 600 nm we eliminate absorption in the CdS and thereby gain an incremental current density of about 1.8 mA/cm^2.

We have prepared CIS cells with an alternative heterojunction layer and no CdS with efficiencies up to 10.3% (see Table V). We are therefore confident that Cd-free CIS modules can be manufactured with reasonable efficiencies, nevertheless, the efficiency gap between these cells and CdS/CIS cells has yet to be closed.

Based on the ASTM E892 global spectrum normalized to 1 kW/m^2 (Figure 20) we have calculated J_{SC} (max) assuming an external quantum efficiency of unity for wavelengths less than 1300 nm, and zero for longer wavelengths (bandgap 0.954 eV). This we find to be 50 mA/cm^2. For absorption in a finite thickness of CIS (with zero back reflection) we find the percentage of J_{SC} (max) that can be obtained as a function of CIS thickness (again assuming no other optical or transport losses) to be as shown in Figure 21. This information will be used in Phase III when we hope to study the trade-offs involved in conversion efficiency and deposition time as a function of CIS thickness.

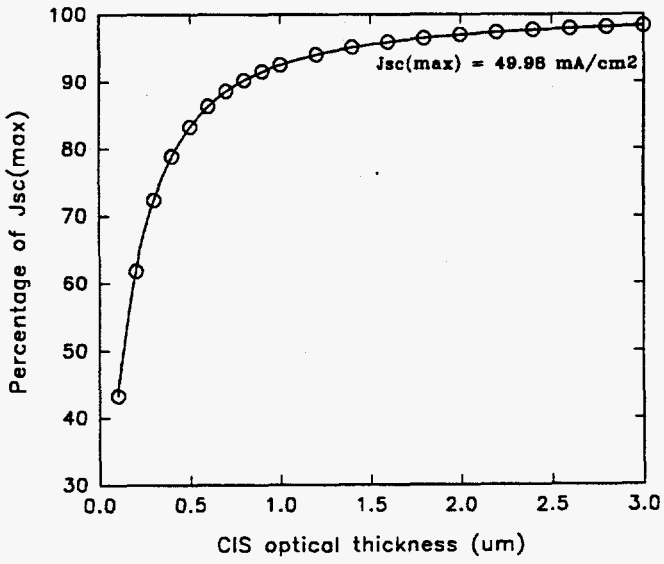

Fig. 21. Percentage of J_{SC} (max) obtainable as a function of CIS thickness

4.7 Modeling of Internal Quantum Efficiency

We have started to model the quantum efficiency of CIS cells to see if it might be possible to extract device and material parameters such as depletion width W and minority carrier diffusion length L. A program was written to calculate the internal quantum efficiency as the sum of contributions from the depletion region and the field-free region. Tuttle's optical absorption data was employed, although near the band edge alpha values were chosen to approximately reproduce the observed QE fall off. Figure 22 shows the influence of W and L, while Figure 23 shows the decomposition into depletion and field-free region contributions for a particular combination of W and L. The dominance of collection from the depletion region is evident. A similar conclusion was reached by Sites [23].

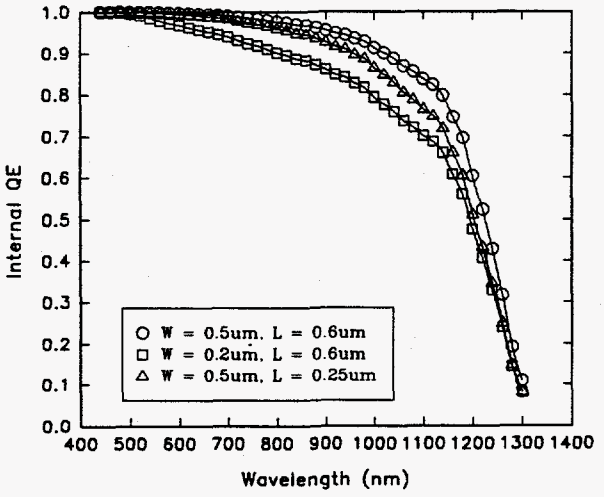

Fig. 22. Internal quantum efficiency versus wavelength for different combinations of space charge width and diffusion length.

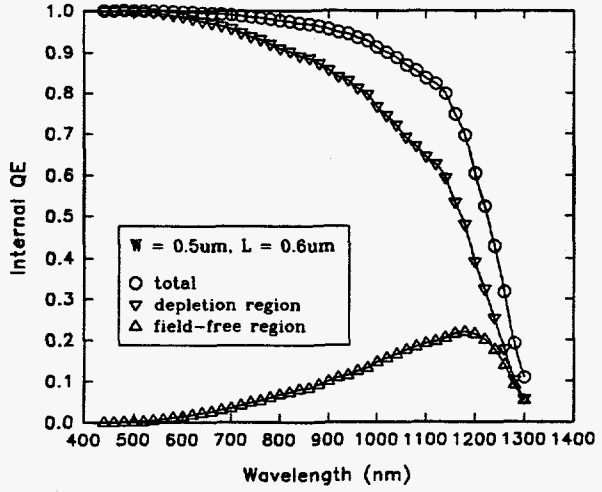

Fig. 23. Decomposition of internal QE into depletion region and field-free region contributions

Section 5.0

MODULE AND INTERCONNECT TECHNOLOGY

5.1 Module-related Problems and their Control

The processing of complete 1 ft^2 plates into modules, as opposed to the handling of smaller glass pieces for cell fabrication, usually presents a fresh set of problems to be dealt with (see for example [7,8]). The most dramatic of these can be occasional peeling of large areas of the CIS from the Mo. This is exacerbated by the presence of scribe lines and stress resulting from the deposition of thicker ZnO. In the course of advancing our module technology we have encountered these and many other problems, for example, berms at the edge of Mo scribes, spatial variation of CIS properties, ZnO/Mo contact resistance and other scribe-related potential drops [2], high series resistance within the cell structure, shunting, and excessive ZnO sheet resistance. The detection and quantification of these problems required bringing to bear a variety of techniques for the local evaluation of cell and material properties at selected areas of experimental modules.

All of the above module-related problems were brought under control during Phase II, with the exception of cell fill factor uniformity. The latter, while reasonable, was limited by the point source nature of our first generation selenization equipment. It is expected that our second generation selenization system will result in completely uniform CIS during Phase III.

5.2 Interconnect Technology

A major push on the module front was rewarded with the successful development of new patterning and interconnect technology for module formation. The underlying idea resulted from careful analysis of the problems encountered in an earlier technology. The new technology has consistently outperformed earlier interconnect schemes, and has been dramatically validated through the achievement of a close to 10% active area efficiency 20 cell mini-module. Several aspects of the new interconnect technology are believed to be entirely EPV distinctive. The process has proven itself to be reliable and capable of reflecting the intrinsic quality of the CIS.

5.3 Module Calculations

For the optimal design of modules, and for the purpose of accurately predicting their performance under variable conditions of temperature and intensity, we have written a computer program to calculate the power generated by a unit cell of the module as a function of the cell parameters. Numerical integration along a coordinate perpendicular to the interconnects is used to exactly calculate the terminal I-V characteristics of the cell. The input parameters are J_{ph}, T, n, J_{oo}, diode series resistance, zinc oxide sheet

resistance, and relevant cell and interconnect widths. Figure 24 shows a three dimensional plot of aperture area efficiency for a laminated module at 300° K as a function of total cell width (3, 4, 5, 6, 7 mm) and ZnO resistance (5, 7, 10, 12, 15, 20, 30 ohms/sq.). Experimental data linking ZnO transmission and sheet resistance and current loss upon lamination were employed to calculate J_{ph}. The exhibited case assumes R_s = 0.3 ohm cm^2, n = 1.55, 0.5 mm dead width, and 0.25 mm ZnO collection width. The aperture efficiency peaks at 8.8% for 12 ohm/sq. ZnO and 4 mm wide cells. At 322° K the peak aperture efficiency is 7.6% (occurring at the same values of ZnO resistance and cell width) and a similarly shaped surface is obtained. Fig. 25 shows the calculated aperture efficiency and fill factor as a function of temperature for a cell width of 0.5 cm. Calculations such as these have been employed in generating realistic values of the temperature coefficients for CIS modules.

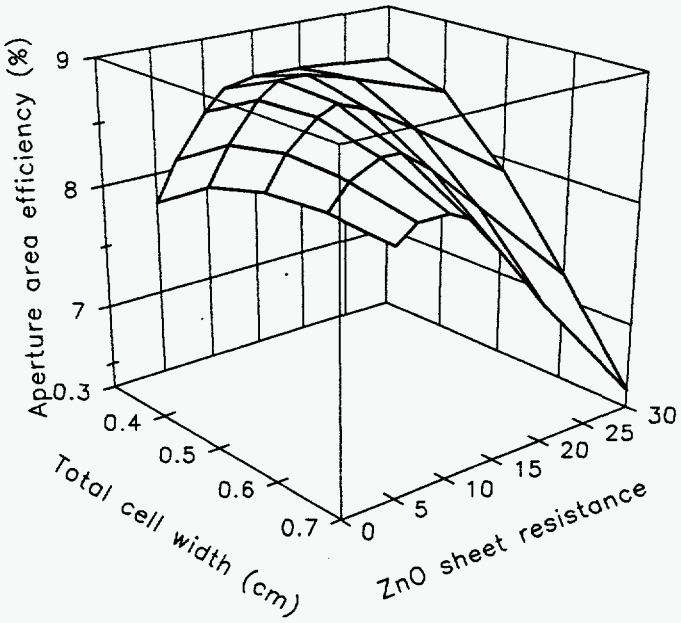

Fig. 24. Calculated aperture area efficiency for glass-glass laminated CIS modules at 300°K versus ZnO sheet resistance and total cell width

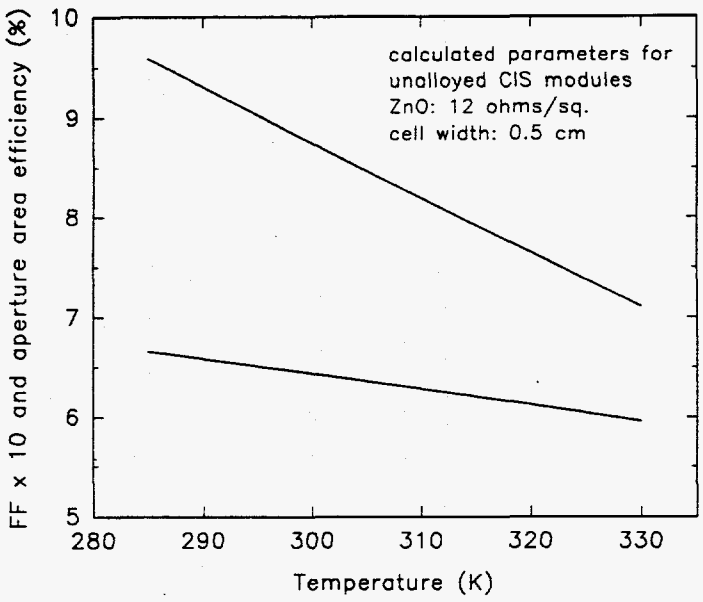

Fig. 25. Calculated temperature dependence of module aperture area efficiency and module fill factor

5.4 Module Results

In order to validate the new interconnect technology described above we sent a CIS mini-module to NREL for efficiency verification. The module consisted of 20 monolithically interconnected cells having an aperture area of 38.3 cm^2. The I-V curve for this module is shown in Figure 26. An aperture area efficiency of 8.04% was measured, with a fill factor of 61.2%, and an average voltage per cell of 455 mV. Subsequent to this demonstration, improvements were made in CIS uniformity, interconnect processing conditions, tip geometry for mechanical scribing of the CIS, and control of ZnO sheet resistance to approximately 10 ohms/square. Application of these improvements allowed larger area CIS modules to be fabricated with reasonable efficiencies. These results are summarized in Table VII. The two larger modules were

Table VII. CIS module PV parameters for a range of module sizes

Aperture Area (cm^2)	# of cells	V_{oc} (V)	I_{sc} (mA)	FF (%)	Power (W)	Aperture Area Efficiency (%)
38.3	20	9.10	55.2	61.2	0.31	8.0*
464.0	43	17.62	297.0	59.0	3.10	6.6
720.0	52	21.50	395.0	52.6	4.50	6.2

*NREL measurements

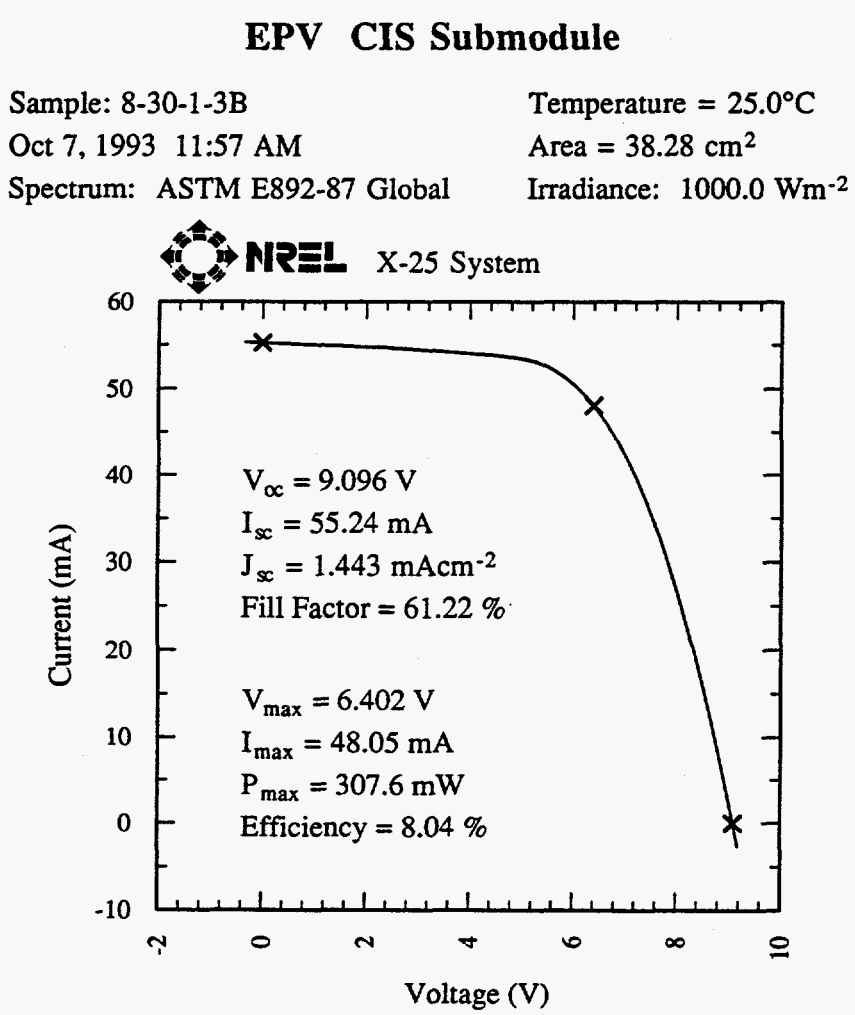

Fig. 26. I-V curve for a 20-cell CIS submodule embodying new interconnect technology (8% aperture area efficiency, 455 mV per cell V_{oc})

measured in sunlight and the current normalized to 100 mW/cm^2. The I-V curve for the 720 cm^2 (4.5 watt) module is shown in Figure 27. It is clear that significant improvements can be made in shunt conductance, fill factor, and area utilization in the larger modules, and this will be a focus of work in the next phase.

The low light performance of modules is more sensitive to the presence of slightly shunted cells than is the 1 sun performance. This is illustrated in Figure 28 which shows the open-circuit voltage for all cells in a 19 cell module under both 100 mW/cm^2 and 0.5 mW/cm^2 illumination. Diagnostics such as these are being used to further improve module performance.

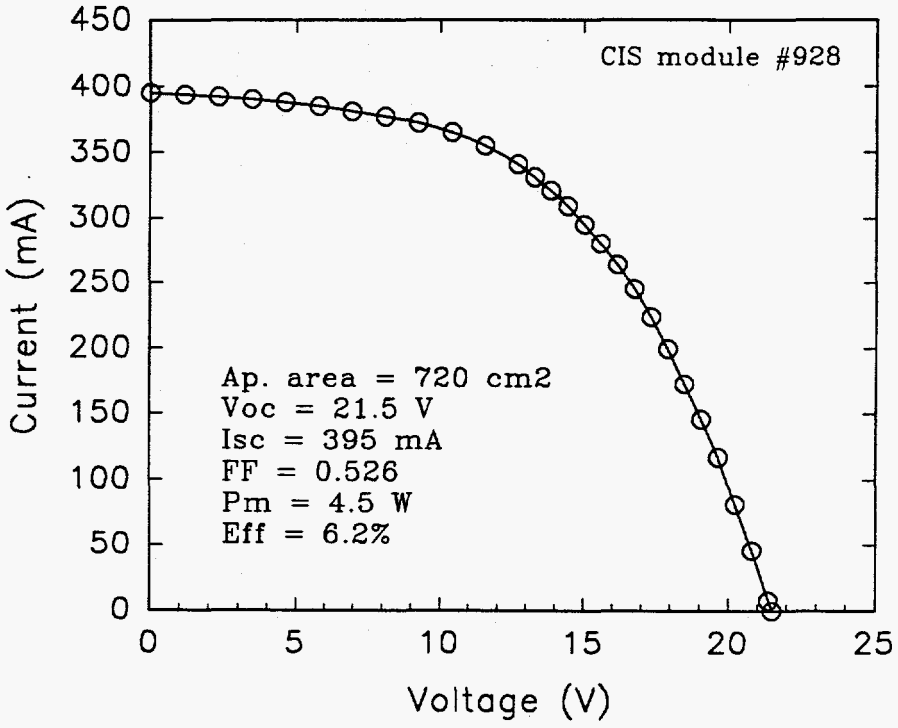

Fig. 27. I-V curve for a 52-cell CIS submodule (aperture area 720cm^2, efficiency 6.2%)

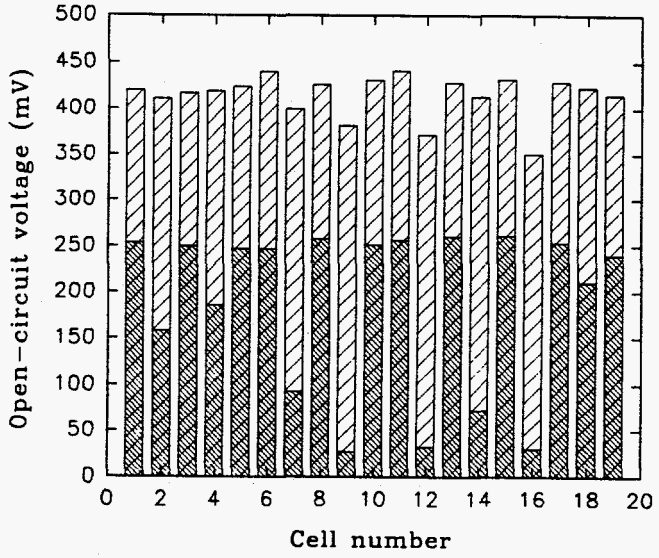

Fig. 28. Open-circuit voltage of all cells in a submodule for 100mW/cm^2 and 0.5 mW/cm^2 illumination

5.5 Module Finishing and Encapsulation

The fabrication of modules from patterned CIS plates involves cutting to size (if necessary), bonding of metal foil bus bars, lamination of a cover glass and attachment of wires or connector. Both UV-cured acrylic and EVA have been used for lamination.

Section 6.0

CONCLUSIONS

A key achievement has been the production of square foot CIS modules without the use of hydrogen selenide. This is seen as a crucial step towards the commercialization of CIS. A novel CIS interconnect technology has allowed the fabrication of smaller modules with aperture area efficiencies of 8% and active area efficiencies approaching 10%. Cell efficiencies of 12.5% have been achieved. Full square foot modules can be produced with powers of about 5 watts.

Section 7.0

FUTURE PLANS

The major programs planned for Phase III are:

1. Increase of module aperture area efficiency to 9-10% through further improvement of CIS uniformity, reduction of shunting effects, and increased area utilization,

2. Increased emphasis on module finishing, encapsulation, and outdoor testing,

3. Preparation of completely uniform CIS on 1 ft^2 substrates using second generation selenization equipment, and

4. Exploration of alternative precursors to CIS formation.

Section 8.0

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Section 9.0

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13. ABSTRACT *(Maximum 200 words)*

This report describes advances made during Phase II of a three-phase, cost-shared subcontract whose ultimate goal is the demonstration of thin-film $CuInSe_2$ (CIS) photovoltaic modules prepared by methods adaptable to safe, high-yield, high-volume manufacturing. The key achievement during this phase was the production of square-foot CIS modules made without the use of H_2Se. This is a crucial step towards the commercialization of CIS. Using a novel interconnect technology, EPV delivered a minimodule with an 8.0% aperture-area efficiency and a 720 cm^2 module with a 6.2% aperture-area efficiency On the processing side, advances were made in precursor formation and the selenization profile, both of which contributed to higher quality CIS. Device analyses revealed a correlation between long-wavelength quantum efficiency and the CIS Cu/In ratio. Temperature-dependent studies highlighted the need for devices with high open-circuit voltages to minimize the impact of the voltage drop at operating temperature. Numerical modeling of module performance was performed to identify the correct ZnO sheet resistance for modules.

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