1 of 1

Computer-Aided Test Equipment Graphics System (CATEGS)

Kansas City Division

W. Fuller

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AlliedSignal Inc.
Kansas City Division
P.O. Box 419159
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COMPUTER-AIDED TEST EQUIPMENT GRAPHICS SYSTEM (CATEGS)

W. Fuller

Published September 1993

Final Report
W. Fuller, Project Leader

Project Team:
J. K. Neuenschwander
J. E. White

Technical Communications
Kansas City Division

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A E R O S P A C E

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A 2-to-1 productivity improvement was achieved by developing designs in an electronic media and electronically moving those designs for drawing preparation and release. Value-added benefits of faster development of design and improved quality of the definitions produced were also achieved.

Of the original five topics to be investigated, only one topic and part of another were completed using the funds allocated for this project.

Discussion

Scope and Purpose

Existing CAD and emerging CAE technologies were evaluated for implementing automated processes applicable to the design, documentation, fabrication, and maintenance of electrical test equipment. Application of this technology was expected to improve the quality, productivity, schedule, and cost performance of AlliedSignal Inc., Kansas City Division, test equipment responsibilities. First benefits of this technology were demonstrated with the initial computer-aided test equipment graphics system (CATEGS).

Activity

Five topics were identified in this investigation. Each topic and its results are listed below.

- Evaluate existing purchased software for auto-routing of printed circuit and wire wrap boards with representative prototype projects.

In the beginning Mylar film and tape were used. This process was inexact and provided no way, other than a visual examination of the artwork, to verify that the artwork was correct. With the implementation of DES software, the advantages of using the VAX-based IEDS PCB software became obvious. Training classes were scheduled and taken. The VAX software was customized to fit our needs and our Gerber photo plotter. The VAX-based software provided many

advantages over manual PCB creation, but it was complicated. Three lab technicians were trained, and they were able to create PCBs using the VAX-based software. Minimal documentation had been produced at this time.

Then PCB Engineer became available. Upon evaluating this product, it was determined that PCB Engineer was a vast improvement over VAX-based IEDS. Therefore, it was decided that before training large numbers of people to do PCBs, we would customize and document this new system and abandon the IEDS product. PCB Engineer was more user friendly and easier to understand. As of December 1990 the PCB Engineer product has been fully customized, at least 12 people have been trained, and a user's guide has been published.

A copy of the user's guide, Version 5.0 (02-07-91), is included as the Appendix to this report. The original of this guide is being updated.

By developing designs in an electronic media and electronically moving those designs, a 2-to-1 productivity improvement was achieved over previous methods. Users and customers also identified value-added benefits of faster development of designs and improved quality of the definitions produced.

- Evaluate existing purchased software for the simulation of digital and analog circuits with representative prototype projects.

Although some work had begun in evaluating Intergraph's HILO digital circuit simulation software, Intergraph has discontinued full support of HILO and is now recommending the AdvanSIM digital circuit simulator. Therefore, the HILO Digital Simulator evaluation was discontinued.

- Evaluate purchased software for the preparation of procedures with combined text and graphics entry using representative prototype projects.

The project to evaluate the preparation of procedures with combined text and graphics entry was not completed. A package called DP/Publisher was investigated and found to be in excess of the requirements of this endeavor. Therefore, the evaluation was discontinued.

- Evaluate the capabilities of the Interpro 32C workstation to determine its application as a multi-tasking general engineering workstation for PC operation, stand-alone designing, and accessing the Kansas City Division mainframes.

The project to evaluate the capabilities of the Interpro 32C workstation was not undertaken with funds allocated for this endeavor.

- Develop and evaluate automated processes for tester fabrication and maintenance. This includes work order and material order preparation, redlining of drawings, simulation during hardware prove-in and tester troubleshooting, and change order preparation. As these automated processes are developed, other applications may be identified which could provide additional benefits. Limited feasibility will be explored and

reported and, if applicable, will be added by revision to this endeavor.

The project to develop automated processes for tester fabrication and maintenance was not undertaken with funds allocated for this endeavor. However, software for redlining of drawings is available on the system.

Accomplishments

All accomplishments have been identified in the above discussion. New features of the CATEGS system are constantly being evaluated and updated. With the availability of designs and component libraries in electronic data bases, further benefits can be achieved by automating other test equipment processes, including integration with the fabrication and maintenance shops.

Appendix

**PCB Engineer User's Guide,
Version 5.0**

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SECTION I
TYPICAL PC BOARD JOB FLOW

1.1 Create The New Schematic:

Design Engineer	CREATE
-----------------	--------

Create an INTELLIGENT flat schematic and then generate a netlist. Refer to the D/131 DES User's Guide, section VII, titled Intelligent Schematic Requirements. Also verify that all of the required Component Dictionary, Component Supply File and Layout Cell Library entries have been made.

NOTE: The cathode of diodes and the positive side of polarized capacitors must be pin number 2.

1.2 Create The New PCB Engineer Job (Same job-name as flat schematic) :

PCB Engineer	Create
--------------	--------

Create from network job "00_pcb_40_seed" found on node "is3".

1.3 Receive The Schematic Netlist:

File	Receive	Job/Lib
------	---------	---------

Select "LOCAL" for the "Node" and then select "job-name S" for the "Job/Lib". When the "Files" menu appears, select "job name.cae" and then select the green check-mark to receive the netlist file.

1.4 Create The Libraries:

A. Component Dictionary

Application Utilities	Library Services	Type Extraction	Component
--------------------------	---------------------	--------------------	-----------

1.4 continued

B. Cell Library

NOTE: The libraries are located on node "isj" in job "00_library_____". There is also an old set of libraries, one or two days old, located on node "dia14" or "ed_pn" in job "old_library".

1.5 Compile The Netlist:

1.6 Define The Job Parameters:

Refer to paragraph 3.1.2 and 3.1.3 for requirements.

1.7 Enter Component Design File:

A. Place Board Area

NOTE: For ENGINEERING, IP32 users, new mouse functions:

1. Press and hold the DATA button to activate PAN feature.
2. Press and hold the COMMAND button to activate ZOOM IN feature.
3. Press and hold the RESET button to activate ZOOM OUT feature.

B. Place Contour

NOTE: Select PIN CODE 199 (0.093 TH drill), LEFT Compensation and check Board Cut. The board contour must be placed in a CLOCKWISE direction. For COUNTERCLOCKWISE placement, select RIGHT Compensation. To use "Tentative" data points on the Board outline, turn "Snap Lock - Keypoint" on. After placing the contour, turn off level 39, the contour level.

C. Place Route Border

D. Place Mounting Holes

NOTE: Key-in pin code for desired mounting hole and key-in a weight of 1, refer to Pin Table, paragraph 3.2.1. You must have two mounting holes for registration, which may be placed off the board if necessary.

E. Place Origins

Carefully select this tooling hole, as it will establish the grid locations. The board origin and the NC origin must be at the same point.

F. Place Route Obstructs

1.8 Netload The Board:

- OR - From the 8-Button menu

Use the File Manager to "Type" the "Netload Log" file and examine it for errors and warnings. This can be done from within the design file by selecting the following: Eng / Design Utilities / Utilities / File Mgr.

1.9 Place The Components:

Note: Remember to allow space for I.C. and transistor sockets as well as card connectors and other hardware.

1.10 Schematic Component Difference:

Check the Net and Type Comparisons. Use the File Manager to "Type" the "Sch Comp Differences" file and examine for errors and warnings.

- 1.11 **Back Annotate** (This is to assure that the design is good prior to executing potentially destructive steps):

Use the File Manager to "Type" the "Back Annotation Log" file and examine for errors and warnings.

- 1.12 **PCBPUT the job to the VAX** (Makes a backup copy of the job, in case of a catastrophe):

Select the CLIX window pick from the top of the 8-Button menu. When prompted, entry your VAX username and password. At the unix prompt, type pcbput. This will copy the entire job to your VAX account as one file named "job_name.pcb".

- 1.13 **Do Any Necessary Placement Improvement** (Including Move Component, Pin Swap, Gate Swap or Renumber Reference Designator):

NOTE: If you wish to generate SLIs, to aid in component placement improvement, refer to step 15.

- 1.14 **Back Annotate If Necessary** (Must be done if Pin Swap, Gate Swap or Renumber Reference Designator were done):
Path: ENG, placement, back annotate

- A. Using the "File" Manager, "Send" the "WasIs List" file to Design Engineer job, "job_name S".
- B. Exit the Component Design File and PCB Engineer.
- C. Enter Design Engineer and select the same "job_name".
- D. Enter a "CLIX" window:
At the UNIX prompt, type -> back_annotate
When prompted for a file name, type the job_name.
When prompted for another file name, type the letter "q".
- E. Delete the CLIX window.
- F. Netlist the schematic; Select Input/Output and then Netlisters.
- G. Exit Design Engineer.
- H. Enter PCB Engineer and select the same "job_name".
- I. Using the "File" manager, "Delete" the "WasIs List" file.
- J. Perform steps 1.3, 1.5 and 1.8 of this procedure.

1.15 Verify Pad Sizes and Drill Sizes for All Parts Placed on the Board.

Be sure to pick drill sizes which exist, refer to ANSI Standard Staight Shank Twist Drill chart. Pad sizes should be at least 0.020 larger in diameter than the applicable drill size.

1.16 Generate SLIs:

-OR- From the 8-Button Menu

Note: Select "minimum spanning tree" for PCBs and "chaining" for WW Bds.

1.17 Route the Board:

-OR- From the 8-Button Menu

NOTE: The Tiger Router is on "is3" and the pop up Tiger window will contain no information. To check the Tiger router log, use the file manager.

1.18 Design Rules Checking (Without planes):

-OR- From the 8-Button Menu

Pop-up the DRC window and examine its contents for errors and warnings. Then enter the design file and place the markers. Review all violations and correct them.

NOTE: Remember to delete DRC Markers when you are done.

1.19 Make Planes:

A. Place Plane Shape

B. Generate Plane Data

Pop-up the Planes Processor window and examine the contents for errors and warnings.

1.20 Design Rules Checking (With planes):

-OR- From the 8-Button Menu

Pop-up the DRC window and examine its contents for errors and warnings. Then enter the design file and place the markers. Review all violations and correct them.

NOTE: Remember to delete DRC Markers when you are done.

1.21 Silk Screen and Layer Information:

- A. Move the reference designators to appropriate locations for silk screening.

- B. Place any additional silk screen requirements on level 36. Suggested line weight = 3 and text height = 0.075.
- C. Place the board number, suffix and top-layer suffix (i.e. 356924-000 A00) on the top layer of the board (level 11). Also place the bottom-layer suffix (i.e. D00) on the bottom layer of the board (level 18).
- D. Place the layer titles as appropriate. Recommended weight = 10 and text size = 0.2. Do not place layer titles on levels 11-18, place them on levels 1-8.

Example: 4 layer board with silkscreen and top and bottom solder mask.

Level 1	DD382756-A00	Level 2	DD382756-B00	Level 3	DD382756-C00
(Layer 1)	JEB 10-19-90	(Layer 2)	JEB 10-19-90	(Layer 3)	JEB 10-19-90
	UNCLASSIFIED		UNCLASSIFIED		UNCLASSIFIED
Level 8	DD382756-D00	Level 36	DD382756-E00		
(Layer 4)	JEB 10-19-90	(Silk Screen)	JEB 10-19-90		
	UNCLASSIFIED		UNCLASSIFIED		
Level 21	SM382756-A00	Level 22	SM382756-D00		
(Solder Mask Top)	JEB 10-19-90	(Solder Mask Bottom)	JEB 10-19-90		
	UNCLASSIFIED		UNCLASSIFIED		

1.22 Plot Setup:

Generate Gerber data and Plot Design files for all layers.

1.23 Review Gerber Data:

1.24 Make Mag Tape:

Select "1200 reel" for the tape device and "stream data" for the write method. Then from the "files" list on the left-hand side of the screen, select each of the Gerber data files to be written to the tape, in the order desired.

Next, mount the tape and select 1600 baud. Then select the green check in the "Send To Tape" window.

If this tape is to be submitted to the Fire 9000, in-plant, then attach the appropriate printout to the tape and take it to the Fire 9000 room. If this tape is to be sent out-of-plant, attach an aperture printout to it.

1.25 Generate Drill and Contour Data Files:

Select "excel_mkiii" for the Machine Name, "Mils" for the Bandwidth and "English" for the Summary Units. Then select the green check.

1.26 Punch Drill and Contour Tapes:

Turn on the punch machine and its interface and load the paper tape onto the take-up spool.

Drill Tape: Select "Prim drill lyr thru" for the Files To Punch, "Paper Tape Punch" for the Punch Machine and "Drill" for the Punch Format.

Contour Tape: Select "Primary contour" for the Files To Punch, "Paper Tape Punch" for the Punch Machine and "Drill" for the Punch Format.

Using the File Manager, print the "Drill summary-1", "Contour summary-1" and the "X-Y Hole Summary" files on the "Eng_laser" or "draft_laser". These files are needed by the manufacturer.

1.27 Top Drawing Creation:

Using the File Manager, receive a file named "Top E Size", "Top D Size" or "Top C Size", as appropriate, from the job named "00 top drawing" found on is3. Then select Graphics from the 8-button menu and select the top drawing from the menu.

Note: You may use the micro-station function key menustrip. You must type drft_ref in the clix window to attach a the drafting format (see Section VIII).

Generic notes for top drawing: (Hdw.cel lib)
ac=NOPC1 - (generic notes)
ac=LMPC1 - (starter field)
ac=rev1 - (revision block)

To plot Top Drawing:

Path: PCB, plot setup
toggle middle window to desired plotter.
Input file - (top E dwg) - plot.

1.28 Assemble Packet To Send To PCB Manufacturer:

Include the following:

1. NC Drill Tape
2. Contour Tape
3. Drill summary-1
4. X-Y Hole summary
5. Contour summary-1
6. Phototools from In-Plant Fira 9000 or mag tape and aperture printout. If you are sending a mag tape out of the plant, call your planner and request that a KD be prepared for it. If this is a rush job, hand-carry the KD to Computer Security for a signature.
7. Top Drawing with the following information on it:
 - a. Part number and suffix
 - b. Material type and thickness.
 - c. Any plating requirements.
 - d. Layer sequence description, in list of materials.
 - e. Fabrication specification, i.e. IPC-ML-910A.
 - f. Dimensions from tooling hole to board corners.

SECTION II
SYSTEM ADMINISTRATOR FUNCTIONS

2.1 Libraries

There are no libraries defined at this time. With the implementation of NFS, we will be able to define libraries across the network.

2.2 Devices

Devices are plotters, printers, paper tape machines, backup and archive storage areas and mag tape definitions. Each of the devices, which have been setup, are described below.

2.2.1 Archive

At this time, we do not see a useful application of the archive function. Therefore, no archive devices are configured.

2.2.2 Backup

At this time, we do not see a useful application of the backup function. Therefore, no backup devices are configured.

2.2.3 Gerber Plot

2.2.3.1 Gerber Disk

This device is used to generate Gerber data files. The data files will be written into the current job with the filenames specified in the PCB, Post Proc, Plotting menus. Currently, the only way to get Gerber data files onto mag tape is to first create them on the disk and later to send them to a mag tape device.

These data files can also be used for verifying designs, before they are sent to the Fire 9000, by accessing them through the Gerber Data Reader utility.

2.2.3.1 Gerber Disk (continued)

The following default Gerber parameters have been setup by the system administrator:

Unit	IN	
Arc Style	None	(Needs to be changed to <u>Quadrant</u> in PCB Engineer version 4.0.2)
Format	2.3	
X-Offset	0.0	
Y-Offset	0.0	
Scale	1.0	
Fill Method	Simple	
Step Mode	Absolute	
Zero Trunc	Leading	
Delimiter	*	
Character Set	ASCII	

2.2.4 IPLOT

This is the new Network Queuing Software (NQS), which controls unix-based plotting on the network. IPLOT will enlarge or reduce your drawing to fit the selected plot size. For this reason, multiple plotter setups are required for the same plotter in order to be able to select the plot size. PCB Engineer does not use this plot method, but Design Engineer does.

Device Name	Physical Device	Location	Queue Name
Drafting Laser A	ilp811	Drafting	d1_laser
Drafting V8836 C	v8836	Drafting (C-size Laser)	d2_v8836
Drafting V8836 D	v8836	Drafting (D-size Laser)	d2_v8836
Drafting V8836 E	v8836	Drafting (E-size Laser)	d2_v8836
Eng Color	Shinko Paper	Engineering	e1_color
Eng Color Transp	Shinko Transp	Engineering	e1_colort
Eng Laser	ilp811 Paper	Engineering	e1_laser
Eng Laser Trans	ilp811 Transp	Engineering	e1_lasert
Eng V8524 C	v8524	Engineering	e2_v8524
Eng V8524 D	v8524	Engineering	e2_v8524

Command line qualifiers for plotting devices:

Drafting Laser	-ysize=8.0	Limits plot size.
Drafting V8836 C	-ysize=17	Limits plot size.
Drafting V8836 D	-ysize=22	Limits plot size.
Drafting V8836 E	-ysize=34	Limits plot size.
Eng Color	-ysize=11	Limits plot size.
Eng Color Transp	-ysize=11	Limits plot size.
Eng Laser	-ysize=8	Limits plot size.
Eng Laser Transp	-ysize=8	Limits plot size.
Eng V8524 C	-ysize=17	Limits plot size.
Eng V8524 D	-ysize=22	Limits plot size.

2.2.5 IPS

This is VAX based plotting which is only used by Drafting for release quality plots.

Device Name	Physical Device	Location	Node Name
Release C-Size	v8836	Drafting	i780
Release D-Size	v8836	Drafting	i780
Release E-Size	v8836	Drafting	i780

Command line qualifiers for plotting devices:

Release C-Size	/size=(22.0,17.0)	/tbl=desengr.tbl
Release D-Size	/size=(34.0,24.0)	/tbl=desengr.tbl
Release E-Size	/size=(44.0,34.0)	/tbl=desengr.tbl

2.2.6 Paper Tape

Device Name	Physical Device	Node Name
Paper Tape	tty00	is3

NOTE: For the paper tape punch software to function, "paper_tape" must reside on is3 in the /usr/ip32/ldes directory.

2.2.7 Printer

The following are the print devices which are configured:

Device Name	Node	Queue
i200	i200	VMS sys\$print
i780	i780	VMS sys\$print
Eng_Laser	N/A	e1_laser (Engineering ILP811)

2.2.8 Store

At this time, we do not see a useful application of the store function. Therefore, no store devices are configured.

2.2.9 Tape

The following are the mag tape devices which are configured:

Device Name	Physical Device	Node Name	System Type
1200 cart	mu:	1200	VMS
1200 reel	ms:	1200	VMS
1780	mta0:	1780_2	VMS
isj 8mm cart	mt6	isj	UNIX
unix tape	mt6	a2_pn	UNIX

SECTION III
PCB SEED FILE

3.1 Job Parameters

The job parameters are accessed from the 8-button menu. The path is: PCB, Application Utilities, Parameters.

3.1.1 Design Options

The following design options are setup in the seed job:

NOTE: Edge connectors have pads on the top and bottom layers only. Therefore, we have standardized on layers 1 and 8 for the top and bottom layers, respectively, for all circuit boards.

Option	Default set by seed job
-----	-----
Top Layer	1
Bottom Layer	8
Active Via Cell	050VIA
Active Jumper Code	1
Active Test Pad Code	1
Via Penalty	Low
Top Class	Pattern
Bottom Class	Dimension
Blind/Buried Vias Used	No
Augment Schematic Netlist	Yes
Allow Display Class Mod.	Yes
Online DRC	Yes
Online DRC Audio Response	Yes

3.1.2 Tables

The following default table assignments are made in the seed job:

Default Set By pcb_seed	Description
Pin Table	Pin Table
Pad Table	Pad Table
Component Dictionary	Component Dictionary
Cell Library	Cell Library
not defined	Bill of Material Library
not defined	Pin Correspondence File
fontlib	Font Library
Color Table	Color Table
Plot Description 1	Plot Setup Descr. File
not defined	3D Cell Library
not defined	Clearance Matrix
not defined	Testpad Table
not defined	Jumper Table

3.1.3 CAM

The following default CAM definitions are included in the seed job:

Default Set By pcb_seed	Default File Name
Logical Tool Table	Logical Tool Table
not defined	Automatic Test Equipment Dictictionary
not defined	Auto Insertion Dictionary
not defined	Auto Insertion Preassigned SMDs
not defined	Auto Insertion Preassigned DIPs
not defined	Auto Insertion Preassigned Axias
not defined	Auto Insertion Preassigned Radials
not defined	Wire Wrap Logical Bin
not defined	Wire Wrap Logical Color
Formatter Table	Aperture Table
not defined	Logical Pen Table
not defined	Optronics ID file

3.1.4 Design Rules

The following default design rules are included in the seed job:

Option	Default Set By pcb_seed
Active Trace Width	15.0
Clearance Trace to Trace	15.0
Clearance Trace to Pad	10.0
Clearance Trace to Mounting Hole	100.0
Clearance Pad to Pad	35.0
Clearance Component to Component	0.0
Clearance Component to Obstruct	0.0
Clearance Component to Board Edge	0.0
Clearance Mounting Hole to Mounting Hole	0.0

3.1.5 Planes

The following default plane definitions are included in the seed job:

Plane Name	Net Name	Plane Layer	Clearance	Type	Pins Processor File
GND	GND	2	15	Regular	Undefined
VCC	VCC	3	15	Regular	Undefined

3.1.6 Special Widths

There are no special widths defined in the seed job.

3.1.7 Levels

The following default level assignments are included in the seed job:

Level	Definition	Level	Definition
9	Pins	23	Registration Marks
29	Type Designator	0	Autoplace Links Front
28	Reference Designator Side 1	0	Autoplace Links Back
0	Reference Designator Side 2	0	Auto Links Via
10	Route Border	21	Solder Mask Side 1
31	SLI	22	Solder Mask Side 2
25	Tooling/Mounting Hole	58	Slots/Contours
27	Board Outline	63	DRC Markers
30	Board Origin	0	Storage
26	Component Outline	34	Placement Checkoff
0	No Place Area	32	Placement Evaluation
0	Panels	0	Placement Outline

3.1.7 continued

----- Level Definition -----		----- Level Definition -----	
1	Top Side Text (etch)	8	Bottom Side Text (etch)
36	Top Side Text (silkscreen)	40	Bottom Side Text (silk- screen)

3.1.8 Etch/Pad Levels

The following etch/pad levels are setup in the seed job:

Layer	Primary	Secondary

1	11	1
2	12	2
3	13	3
4	14	4
5	15	5
6	16	6
7	17	7
8	18	8

3.2 PIN, PAD and LEVEL CORRESPONDENCE TABLES

These tables are accessed from the 8-button menu. The path is: PCB, Application Utilities, Tables.

The Font 126 and Pad Definitions tables are included here as reference material for interpreting the Pin and Pad tables.

NOTE: Fast Font turns letters on rather than pad shapes.

Font 126

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
□	◻	○	◇	◊	⊠	⊞	⊡	⊢	⊣	⊤	⊥	⊦	⊧	⊨	⊩	⊪	⊫	⊬	⊭	⊮	⊯	⊰	⊱	⊲	⊳
a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x	y	=
○	○	○	○	⊗	○	○	○	○	○	○	□	▤	▥	▦	▧	▨	▩	▪	▫	▬	▭	▮	▯	▰	▱

Pad Definitions

Pad Type	Physical Geometry	Offset Axis	Pad Type	Physical Geometry	Offset Axis
0	○	-	8	⊙	Y
1	◻	X	9	◻	X
2	◻	X	10	◻	Y
3	◻	X	11	◻	X
4	◻	X	13	△	Y
5	◻	Y	14	◻	X
6	◻	Y	15	▽	Y
7	◻	Y	16	◻	X

3.2.1 Pin Table Definition

The following default pin table is included in the seed job:

NOTE: The pins have been defined such that the hole/drill size is equal to the pad diameter. This will cause the DRC (Design Rules Checking) software to correctly check the trace to pad clearances even though we do not place pads in our designs. DRC will actually be checking the trace to pin clearance, where the pin/drill size matches the pad size.

PIN CODE	FONT	CHAR	HEIGHT	WIDTH	APER- TURE	DIAMETER (LAYER)	PAD CODE	
1	126	A	62	62	24	62	3	NORMAL -LANDS
2	126	B	75	75	3	75	4	
3	126	C	75	75	3	75	5	
4	126	D	86	86	4	86	6	
5	126	E	100	100	5	100	7	
6	126	F	100	100	5	100	8	
7	126	H	125	125	13	125	9	
8	126	I	125	125	13	125	10	
9	126	G	125	125	13	125	10	
10	126	A	62	62	24	62	3	-VCC & GND LANDS
11	126	J	62	62	24	62	3	
12	126	K	62	62	24	62	3	
13	126	L	75	75	3	75	4	
14	126	M	75	75	3	75	4	
15	126	N	75	75	3	75	5	
16	126	O	75	75	3	75	5	
17	126	Q	86	86	4	86	6	
18	126	R	86	86	4	86	6	
19	126	S	100	100	5	100	7	
20	126	T	100	100	5	100	7	
21	126	U	100	100	5	100	8	
22	126	V	100	100	5	100	8	
23	126	W	125	125	13	125	9	
24	126	P	125	125	13	125	9	
25	126	Y	125	125	13	125	10	
26	126	Z	125	125	13	125	10	
27	126		40	40	1	40	40	

3.2.1 Pin Table Definition (continued)

PIN CODE	FONT	CHAR	HEIGHT	WIDTH	APER- TURE	DIAMETER (LAYER)	PAD CODE	
28	0		63	63	1	63	0	MOUNTING HOLES
29	0		78	78	1	78	0	
30	0		94	94	1	94	0	
31	0		109	109	1	109	0	
32	0		125	125	1	125	0	
33	0		140	140	1	140	0	
34	0		156	156	1	156	0	
35	0		172	172	1	172	0	
36	0		188	188	1	188	0	
37	0		203	203	1	203	0	
38	0		219	219	1	219	0	
39	0		234	234	1	234	0	
40	0		250	250	1	250	3	VIAS
41	126	3	50	50	2	50	41	
42	126	3	62	62	24	62	42	
43	0	0	0	0	0	0	0	
51	126	a	20	20	1	20	51	
52	126	b	25	25	1	25	52	
53	126	c	30	30	1	30	53	
54	126	d	35	35	1	35	54	
55	126	f	40	40	1	40	55	
56	126	g	45	45	2	45	56	
57	126	h	50	50	2	50	57	
58	126	i	55	55	24	55	58	
59	126	j	62	62	24	62	59	
60	126	k	65	65	24	65	60	
61	126	l	0	0	0	0	0	
62	126	m	0	0	0	0	0	
63	126	n	0	0	0	0	0	
64	126	o	0	0	0	0	0	
65	126	p	25	25	0	26	165	
66	126	q	25	25	0	26	166	
67	126	r	0	0	0	0	0	
68	126		0	0	0	0	0	
70	126		0	0	0	0	6	

3.2.1 Pin Table Definition (continued)

PIN CODE	FONT	CHAR	HEIGHT	WIDTH	APER- TURE	DIAMETER (LAYER)	PAD CODE	
78	0		63	63	1	63	0	-MOUNTING HOLES
79	0		78	78	1	78	0	
80	0		94	94	1	94	0	
81	0		109	109	1	109	0	
82	0		125	125	1	125	0	
83	0		140	140	1	140	0	
84	0		156	156	1	156	0	
85	0		172	172	1	172	0	
86	0		188	188	1	188	0	
87	0		203	203	1	203	0	
88	0		219	219	1	219	0	
89	0		234	234	1	234	0	
90	0		250	250	1	250	0	
91	0		120	120	1	120	0	
92	0		89	89	1	89	0	-SPECIAL
100	126	A	62	62	24	62	3	
101	126	E	100	100	5	100	101	
199	126	a	93	93	0	93	0	-CONTOUR PIN CODE
201	126	f	40	40	1	layer 1	21	-EDGE CONNECTORS
202	126	f	40	40	1	layer 2	21	
203	126	B	75	75	3	layer 1	22	
204	126	B	75	75	3	layer 4	22	
205	126	B	75	75	3	layer 1	23	
206	126	B	75	75	3	layer 8	33	
207	126	G	24	24	0	layer 1	66	
208	126	B	26	26	0	layer 1	208	
209	126	A	26	26	0	layer 8	209	
210	126	A	44	44	0	layer 2	20	
211	126	A	25	25	0	layer 1	22	
212	126	A	25	25	0	layer 2	22	
221	126	A	44	44	0	layer 1	221	
222	126	A	44	44	0	layer 2	222	
231	126	A	40	40	0	layer 1	68	-SURFACE MOUNTED DEVICES
232	126	B	40	40	0	layer 2	68	
247	126	h	50	50	2	layer 1	247	
248	126	A	62	62	24	layer 1	248	
249	126	B	75	75	3	layer 1	249	
250	126	D	86	86	4	layer 1	250	
251	126	E	100	100	5	layer 1	251	
252	126	H	125	125	13	layer 1	252	
253	126	a	20	50	17	layer 1	253	
254	126	a	50	20	17	layer 1	254	

3.2.2 Pad Table Definition

The following default pad table is included in the seed job:

NOTE: We have decided not to use the pads processor, and not to place pads in our designs. This decision was made to conserve design file space and to simplify the design process. Due to this decision, the pad table is only used to establish the default pad sizes used during DRC (Design Rules Checking).

PAD CODE	FONT	CHAR	HEIGHT	WIDTH	APER- TURE	DIAMETER	TYPE	X	Y	OFFSET
1	126	C	30	30	8	21	0	30	30	-
2	126	C	55	55	9	29	0	55	55	-
3	126	A	62	62	24	62	0	62	62	-
4	126	B	75	75	3	75	0	75	75	-
5	126	C	75	75	3	75	0	75	75	-
6	126	D	86	86	4	86	0	86	86	-
7	126	E	100	100	5	100	0	100	100	-
8	126	F	100	100	5	100	0	100	100	-
9	126	H	125	125	13	125	0	125	125	-
10	126	I	125	125	13	125	0	125	125	-
11	126	A	75	60	18	0	1	75	60	0
12	126	A	60	75	19	0	1	60	75	0
13	126	A	60	60	20	0	1	60	60	0
14	126	A	75	75	21	0	1	75	75	0
15	126	G	101	81	22	37	0	101	81	-
16	126	P	101	81	22	37	0	101	81	-
17	126		150	120	23	0	0	150	120	-
18	126		187	187	24	0	0	187	187	-
19	126	C	62	500	0	0	2	500	62	200
20	126	C	62	500	0	0	2	500	62	150
21	126	A	500	62	24	62	6	62	500	-219
22	126	A	425	75	3	75	6	75	425	-175
23	126	A	975	75	3	75	5	75	975	-450
24	126	G	150	150	1	125	0	150	150	-
25	126		1	1	20	0	12	75	60	0
26	126		1	1	20	0	11	60	75	0
27	126	A	52	32	0	0	5	32	52	0
28	126	A	32	52	0	0	1	52	32	0

3.2.2 Pad Table Definition (Continued)

PAD CODE	FONT	CHAR	HEIGHT	WIDTH	APER- TURE	DIAMETER	TYPE	X	Y	OFFSET
29	126		0	0	1	0	0	0	0	-
30	126	B	11	11	0	0	0	11	11	-
33	126	A	975	74	3	75	5	75	975	350
40	126		40	40	1	40	0	40	40	-
41	126	3	50	50	2	50	0	50	50	-
42	126	3	62	62	24	62	0	62	62	-
51	126	a	20	20	1	20	0	20	20	-
52	126	b	25	25	1	25	0	25	25	-
53	126	c	30	30	1	30	0	30	30	-
54	126	d	35	35	1	35	0	35	35	-
55	126	f	40	40	1	40	0	40	40	-
56	126	g	45	45	2	45	0	45	45	-
57	126	h	50	50	2	50	0	50	50	-
58	126	i	55	55	24	55	0	55	55	-
59	126	j	62	62	24	62	0	62	62	-
60	126	k	65	65	24	65	0	65	65	-
61	126	0	0	0	0	0	0	0	0	-
62	126	1	0	0	0	0	0	0	0	-
63	126	4	0	0	0	0	0	0	0	-
64	126	5	0	0	0	0	0	0	0	-
65	126	7	25	150	0	0	0	150	25	-
66	126	8	150	25	0	0	0	25	150	-
67	126	9	65	100	0	0	0	100	65	-
68	126	s	100	50	0	0	0	50	100	-
69	126	t	60	65	0	0	0	65	60	-
70	126	u	65	60	0	0	0	60	65	-
71	126	v	150	15	0	0	0	15	150	-
72	126	w	15	150	0	0	0	150	15	-
73	126	x	25	75	0	0	0	75	25	-
74	126	y	75	25	0	0	0	25	75	-
75	126	z	15	75	0	0	0	75	15	-
76	126	!	75	15	0	0	0	15	75	-
80	126	A	40	40	9	20	0	40	40	-
101	126	A	1100	100	5	100	6	100	1100	-500
165	126	%	40	40	0	32	0	40	40	-
166	126	?	40	40	0	32	0	40	40	-
208	126	@	40	40	0	0	0	40	40	-
209	126	#	40	40	0	0	0	40	40	-
221	126	A	60	60	0	30	0	60	60	-
222	126	A	20	20	10	0	0	20	20	-
247	126	h	50	50	2	50	1	50	50	-

3.2.2 Pad Table Definition (Continued)

PAD CODE	FONT	CHAR	HEIGHT	WIDTH	APER- TURE	DIAMETER	TYPE	X	Y	OFFSET
248	126	A	62	62	24	62	1	62	62	-
249	126	B	75	75	3	75	1	75	75	0
250	126	D	86	86	4	86	1	86	86	0
251	126	E	100	100	5	100	1	100	100	0
252	126	H	125	125	13	125	1	125	125	0
253	126	a	20	50	17	20	1	50	20	0
254	126	a	50	20	17	20	1	20	50	0

3.2.3 Level/Level Correspondence

The level correspondence file has not been modified.

1 to 1
.
.
.
63 to 63

3.2.4 Jumper Table Definition

The jumper table is used for surface mounted devices only.
No jumper tables have been defined.

3.2.5 Test Pad Table Definition

The test pad table is for surface mounted devices only.
No test pad tables have been defined.

3.3 Plotting

The plotting parameters are accessed from the 8-button menu.
The path is: PCB, Post Proc, Plotting.

3.3.1 Plot Setup

The following defaults are set up by the seed job:

NOTE: Edge connectors only have pads on the top and bottom layers. These layer numbers are built into the call. Therefore, in order to support edge connectors and to standardize our PCB designs, the seed job sets the top and bottom layers to 1 and 8 respectively.

Logical file name*	Level/Layer	Elements to be plotted
G: layer one	layer 1	Traces Layer 1, Mounting Holes, Component Pins_THR, Via Pins, Graphic Elements_ U_ALL Level 1 Graphic Elements_U _ALL Level 11 Component Pads_TOP Layer 1
G: GND plane	layer 2	Traces Layer 2, Mounting Holes, Component Pins_THR, Via Pins, Plane Data Layer 2, Graphic Elements_U_ALL Level 2
G: VCC plane	layer 3	Traces Layer 3, Mounting Holes, Component Pins_THR, Via Pins, Plane Data Layer 3, Graphic Elements_U_ALL Level 3
G: layer eight	layer 8	Traces Layer 8, Mounting Holes, Component Pins_THR, Via Pins, Graphic Elements_U_ALL Level 8 Graphic Elements_U_ALL Level 18 Component Pads_BOT Layer 8

3.3.1 (continued)

Logical file name*	Level/Layer	Elements to be plotted
G: solder mask top		Solder Mask Side 1_U All, Mounting Holes, Via Pins, Component Pins_THR, Component Pads_TOP Layer 1
G: solder mask bot		Solder Mask Side 2_U All, Mounting Holes, Via Pins, Component Pins_THR, Component Pads_BOT Layer 8
G: silk screen top	level 36	Graphic Elements_0_U_ PRM Level 36, Mounting Holes, Ref designator ALL, Component Outline_U_ ALL

NOTE: Modify screen to change fill ellipses to draw ellipses.

* Name specified in PCB, Post Proc, Plotting menus.

3.3.2 Gerber - D-Code/Aperture Correlation

The correlation table was not modified.

Apertures	D-Code
1 -- 10	10 -- 19
11 -- 12	70 -- 71
13 -- 22	20 -- 29
23 -- 24	72 -- 73
25 -- 29	5 -- 9
30 -- 69	30 -- 69
70 -- 70	4 -- 4

3.3.3 Gerber - Aperture Wheel

The following aperture wheel is included in the seed job:

NOTE: The aperture assignments were made to match our Gerber Photoplotter, of which the aperture wheel had already been defined by previous users; the Applicon system. Some new apertures have been added to support surface mount devices.

Aperture number	Definition	Function
1	Round .040	Flash
2	Round .050	Flash
3	Round .075	Flash
4	Round .086	Flash
5	Round .100	Flash
6	Round .005	Flash
7	Round .010	Draw
8	Round .015	Draw
9	Round .020	Draw
10	Round .025	Draw
11	not defined	
12	not defined	
13	Round .125	Flash
14	Round .150	Flash
15	Round .175	Flash
16	Round .040	Draw
17	not defined	
18	Round .050	Draw
19	Round .075	Draw
20	Round .100	Draw
21	Round .125	Draw
22	Round .150	Draw
23	not defined	
24	Round .062	Flash
97	Square .050	Flash
98	Square .062	Flash
99	Square .075	Flash
100	Square .086	Flash
101	Square .100	Flash
102	Square .125	Flash
103	Rectangle .020 x .050	Flash
104	Rectangle .050 x .020	Flash

3.3.4 Gerber - Formatter Table

The following formatter table is included with the seed job:

Type	Qualifier	Value	Pos	Size	Shape	Angle	Description
PIN	PIN_CODE	27	1	40 x 40	ROUND	0	Mounting Hole, 0.040
PIN	PIN_CODE	51	1	40 x 40	ROUND	0	Via, 0.040
PIN	PIN_CODE	52	1	40 x 40	ROUND	0	Via, 0.040
PIN	PIN_CODE	53	1	40 x 40	ROUND	0	Via, 0.040
PIN	PIN_CODE	54	1	40 x 40	ROUND	0	Via, 0.040
PIN	PIN_CODE	55	1	40 x 40	ROUND	0	Via, 0.040
PIN	PIN_CODE	91	1	40 x 40	ROUND	0	Mounting Hole, 0.120
PIN	PIN_CODE	92	1	40 x 40	ROUND	0	Mounting Hole, 0.089
PIN	PIN_CODE	56	1	50 x 50	ROUND	0	Via, 0.050
PIN	PIN_CODE	57	1	50 x 50	ROUND	0	Via, 0.050
PIN	PIN_CODE	34	1	50 x 50	ROUND	0	Mounting Hole, 0.156
PIN	PIN_CODE	35	1	50 x 50	ROUND	0	Mounting Hole, 0.172
PIN	PIN_CODE	36	1	50 x 50	ROUND	0	Mounting Hole, 0.188
PIN	PIN_CODE	37	1	50 x 50	ROUND	0	Mounting Hole, 0.203
PIN	PIN_CODE	84	1	50 x 50	ROUND	0	Mounting Hole, 0.156
PIN	PIN_CODE	85	1	50 x 50	ROUND	0	Mounting Hole, 0.172
PIN	PIN_CODE	86	1	50 x 50	ROUND	0	Mounting Hole, 0.188
PIN	PIN_CODE	87	1	50 x 50	ROUND	0	Mounting Hole, 0.203
PIN	PIN_CODE	2	1	75 x 75	ROUND	0	Norm. Land, 0.075
PIN	PIN_CODE	3	1	75 x 75	ROUND	0	Norm. Land, 0.075
PIN	PIN_CODE	13	1	75 x 75	ROUND	0	GND Land, 0.075
PIN	PIN_CODE	14	1	75 x 75	ROUND	0	VCC Land, 0.075
PIN	PIN_CODE	15	1	75 x 75	ROUND	0	GND Land, 0.075
PIN	PIN_CODE	16	1	75 x 75	ROUND	0	VCC Land, 0.075
PIN	PIN_CODE	79	1	75 x 75	ROUND	0	Mounting Hole, 0.078
PIN	PIN_CODE	29	1	75 x 75	ROUND	0	Mounting Hole, 0.078
PIN	PIN_CODE	101	1	75 x 75	ROUND	0	Mounting Hole, 0.100
PIN	PIN_CODE	4	1	86 x 86	ROUND	0	Norm. Land, 0.086
PIN	PIN_CODE	17	1	86 x 86	ROUND	0	GND Land, 0.086
PIN	PIN_CODE	18	1	86 x 86	ROUND	0	VCC Land, 0.086
PIN	PIN_CODE	30	1	86 x 86	ROUND	0	Mounting Hole, 0.094
PIN	PIN_CODE	38	1	86 x 86	ROUND	0	Mounting Hole, 0.219
PIN	PIN_CODE	39	1	86 x 86	ROUND	0	Mounting Hole, 0.234
PIN	PIN_CODE	40	1	86 x 86	ROUND	0	Mounting Hole, 0.250
PIN	PIN_CODE	80	1	86 x 86	ROUND	0	Mounting Hole, 0.094
PIN	PIN_CODE	88	1	86 x 86	ROUND	0	Mounting Hole, 0.219
PIN	PIN_CODE	89	1	86 x 86	ROUND	0	Mounting Hole, 0.234
PIN	PIN_CODE	90	1	86 x 86	ROUND	0	Mounting Hole, 0.250
PIN	PIN_CODE	5	1	100 x 100	ROUND	0	Norm. Land, 0.100
PIN	PIN_CODE	6	1	100 x 100	ROUND	0	Norm. Land, 0.100
PIN	PIN_CODE	19	1	100 x 100	ROUND	0	GND Land, 0.100
PIN	PIN_CODE	20	1	100 x 100	ROUND	0	VCC Land, 0.100
PIN	PIN_CODE	21	1	100 x 100	ROUND	0	GND Land, 0.100
PIN	PIN_CODE	22	1	100 x 100	ROUND	0	VCC Land, 0.100
PIN	PIN_CODE	31	1	100 x 100	ROUND	0	Mounting Hole, 0.109
PIN	PIN_CODE	81	1	100 x 100	ROUND	0	Mounting Hole, 0.109

3.3.4 Gerber - Formatter Table (continued)

Type	Qualifier	Value	Pos	Size	Shape	Angle	Description
TRACE	WIDTH	5	6	5 x 5	ROUND	0	Trace, 0.005
TRACE	WIDTH	10	7	10 x 10	ROUND	0	Trace, 0.010
LINE	WEIGHT	2	7	10 x 10	ROUND	0	Line Weight 2, 0.010
PIN	PIN_CODE	5	1	100 x 100	ROUND	0	Norm. Land, 0.100
PIN	PIN_CODE	6	1	100 x 100	ROUND	0	Norm. Land, 0.100
PIN	PIN_CODE	19	1	100 x 100	ROUND	0	GND Land, 0.100
PIN	PIN_CODE	20	1	100 x 100	ROUND	0	VCC Land, 0.100
PIN	PIN_CODE	21	1	100 x 100	ROUND	0	GND Land, 0.100
PIN	PIN_CODE	22	1	100 x 100	ROUND	0	VCC Land, 0.100
PIN	PIN_CODE	31	1	100 x 100	ROUND	0	Mounting Hole, 0.109
PIN	PIN_CODE	81	1	100 x 100	ROUND	0	Mounting Hole, 0.109
TRACE	WIDTH	5	6	5 x 5	ROUND	0	Trace, 0.005
TRACE	WIDTH	10	7	10 x 10	ROUND	0	Trace, 0.010
LINE	WEIGHT	2	7	10 x 10	ROUND	0	Line Weight 2, 0.010
TRACE	WIDTH	15	8	15 x 15	ROUND	0	Trace, 0.015
LINE	WEIGHT	0	8	15 x 15	ROUND	0	Line Weight 0, 0.015
LINE	WEIGHT	3	8	15 x 15	ROUND	0	Line Weight 3, 0.015
TRACE	WIDTH	20	9	20 x 20	ROUND	0	Trace, 0.020
LINE	WEIGHT	4	9	20 x 20	ROUND	0	Line Weight 4, 0.020
TRACE	WIDTH	25	10	25 x 25	ROUND	0	Trace, 0.025
LINE	WEIGHT	5	10	25 x 25	ROUND	0	Line Weight 5, 0.025
PIN	PIN_CODE	7	13	125 x 125	ROUND	0	Norm. Land, 0.125
PIN	PIN_CODE	8	13	125 x 125	ROUND	0	Norm. Land, 0.125
PIN	PIN_CODE	9	13	125 x 125	ROUND	0	Norm. Land, 0.125
PIN	PIN_CODE	23	13	125 x 125	ROUND	0	GND Land, 0.125
PIN	PIN_CODE	24	13	125 x 125	ROUND	0	VCC Land, 0.125
PIN	PIN_CODE	25	13	125 x 125	ROUND	0	GND Land, 0.125
PIN	PIN_CODE	26	13	125 x 125	ROUND	0	VCC Land, 0.125
PIN	PIN_CODE	32	13	125 x 125	ROUND	0	Mounting Hole, 0.125
PIN	PIN_CODE	33	13	125 x 125	ROUND	0	Mounting Hole, 0.140
PIN	PIN_CODE	82	13	125 x 125	ROUND	0	Mounting Hole, 0.125
PIN	PIN_CODE	83	13	125 x 125	ROUND	0	Mounting Hole, 0.140
TRACE	WIDTH	40	16	40 x 40	ROUND	0	Trace, 0.040
LINE	WEIGHT	1	16	40 x 40	ROUND	0	Line Weight 1, 0.040
TRACE	WIDTH	50	18	50 x 50	ROUND	0	Trace, 0.050
LINE	WEIGHT	6	18	50 x 50	ROUND	0	Line Weight 6, 0.050
LINE	WEIGHT	10	18	50 x 50	ROUND	0	Line Weight 10, 0.050
LINE	WEIGHT	12	18	50 x 50	ROUND	0	Line Weight 12, 0.050
TRACE	WIDTH	75	19	75 x 75	ROUND	0	Trace, 0.075
LINE	WEIGHT	9	19	75 x 75	ROUND	0	Line Weight 9, 0.075
LINE	WEIGHT	19	19	75 x 75	ROUND	0	Line Weight 19, 0.075
LINE	WEIGHT	15	19	75 x 75	ROUND	0	Line Weight 15, 0.075

3.3.4 Gerber - Formatter Table (continued) .

Type	Qualifier	Value	Pos	Size	Shape	Angle	Description
TRACE	WIDTH	100	20	100 x 100	ROUND	0	Trace, 0.100
LINE	WEIGHT	13	20	100 x 100	ROUND	0	Line Weight 13, 0.100
LINE	WEIGHT	20	20	100 x 100	ROUND	0	Line Weight 20, 0.100
LINE	WEIGHT	21	20	100 x 100	ROUND	0	Line Weight 21, 0.100
TRACE	WIDTH	125	21	125 x 125	ROUND	0	Trace, 0.125
LINE	WEIGHT	14	21	125 x 125	ROUND	0	Line Weight 14, 0.125
LINE	WEIGHT	16	21	125 x 125	ROUND	0	Line Weight 16, 0.125
LINE	WEIGHT	22	21	125 x 125	ROUND	0	Line Weight 22, 0.125
TRACE	WIDTH	150	22	150 x 150	ROUND	0	Trace, 0.150
LINE	WEIGHT	17	22	150 x 150	ROUND	0	Line Weight 17, 0.150
LINE	WEIGHT	23	22	150 x 150	ROUND	0	Line Weight 23, 0.150
PIN	PIN_CODE	1	24	62 x 62	ROUND	0	Norm. Land, 0.062
PIN	PIN_CODE	10	24	62 x 62	ROUND	0	Norm. Land, 0.062
PIN	PIN_CODE	11	24	62 x 62	ROUND	0	GND Land, 0.062
PIN	PIN_CODE	12	24	62 x 62	ROUND	0	VCC Land, 0.062
PIN	PIN_CODE	58	24	62 x 62	ROUND	0	Via, 0.062
PIN	PIN_CODE	59	24	62 x 62	ROUND	0	Via, 0.062
PIN	PIN_CODE	60	24	62 x 62	ROUND	0	Via, 0.062
PIN	PIN_CODE	28	24	62 x 62	ROUND	0	Mounting Hole, 0.063
PIN	PIN_CODE	78	24	62 x 62	ROUND	0	Mounting Hole, 0.063
PIN	PIN_CODE	247	97	50 x 50	SQUARE	0	Surface Pin(Layer 1), 0.050
PIN	PIN_CODE	248	98	62 x 62	SQUARE	0	Surface Pin(Layer 1), 0.062
PIN	PIN_CODE	249	99	75 x 75	SQUARE	0	Surface Pin(Layer 1), 0.075
PIN	PIN_CODE	250	100	86 x 86	SQUARE	0	Surface Pin(Layer 1), 0.086
PIN	PIN_CODE	251	101	100 x 100	SQUARE	0	Surface Pin(Layer 1), 0.100
PIN	PIN_CODE	252	102	125 x 125	SQUARE	0	Surface Pin(Layer 1), 0.125
PIN	PIN_CODE	253	103	20 x 50	RECTNGL	0	Surface Pin(Layer 1), 0.020 x 0.050
PIN	PIN_CODE	254	104	50 x 20	RECTNGL	0	Surface Pin(Layer 1), 0.050 x 0.020

3.3.4 continued

The results of this table are summarized in the following tables:

Circles and Mounting Holes

Weight	Flash (Land)	:	Weight	Draw (Path)
1	0.040	:	0,3	0.015
6	0.050	:	2	0.010
8,18	0.062	:	4	0.020
9,19	0.075	:	5	0.025
11	0.086	:	10,12	0.050
13,21	0.100	:	15	0.075
14,16	0.125	:	20	0.100
17	0.150	:	22	0.125
		:	23	0.150

Lines, Line Strings, Arcs, Paths, Lettering and Shapes (On levels 1-8):

Weight	Draw (Land)	:	Width	Draw (Path)
2	0.010	:	10	0.010
3	0.015	:	15	0.015
4	0.020	:	20	0.020
5	0.025	:	25	0.025
10,12	0.050	:	50	0.050
15	0.075	:	75	0.075
20	0.100	:	100	0.100
22	0.125	:	125	0.125
23	0.150	:	150	0.150

3.3.4 Gerber - Gerber Data Reader

The only parameters which the seed job modifies are located under the 'Files' menu. In the 'Definitions' section of this menu, the 'Format' and 'Step Mode' have been changed to '2.3' and 'Absolute' respectively.

3.4 NC Drill

The following default tool table is included with the seed job. This table can be edited and received to another file.

Tool Num	Pin/Hole Code	Hit Count	Spindl Rate	Phy Tool	Use	Feed Rate (IPM)	Linear Feed (IPM)	Reverse Feed (IPM)	Dia (IN)
1	57	5000	20000	0	prim	100	0	0	0.0280
2	1	5000	20000	0	prim	100	0	0	0.0350
2	2	5000	20000	0	prim	100	0	0	0.0350
2	3	5000	20000	0	prim	100	0	0	0.0350
2	11	5000	20000	0	prim	100	0	0	0.0350
2	12	5000	20000	0	prim	100	0	0	0.0350
2	13	5000	20000	0	prim	100	0	0	0.0350
2	14	5000	20000	0	prim	100	0	0	0.0350
2	15	5000	20000	0	prim	100	0	0	0.0350
2	16	5000	20000	0	prim	100	0	0	0.0350
2	49	5000	20000	0	prim	100	0	0	0.0350
2	59	5000	20000	0	prim	100	0	0	0.0350
3	4	5000	20000	0	prim	100	0	0	0.0410
3	17	5000	20000	0	prim	100	0	0	0.0410
3	18	5000	20000	0	prim	100	0	0	0.0410
4	5	5000	20000	0	prim	100	0	0	0.0550
4	6	5000	20000	0	prim	100	0	0	0.0550
4	19	5000	20000	0	prim	100	0	0	0.0550
4	20	5000	20000	0	prim	100	0	0	0.0550
4	21	5000	20000	0	prim	100	0	0	0.0550
4	22	5000	20000	0	prim	100	0	0	0.0550
5	7	5000	20000	0	prim	100	0	0	0.0860
5	8	5000	20000	0	prim	100	0	0	0.0860
5	23	5000	20000	0	prim	100	0	0	0.0860
5	24	5000	20000	0	prim	100	0	0	0.0860
6	28	5000	20000	0	prim	100	0	0	0.0630
6	78	5000	20000	0	prim	100	0	0	0.0630
7	31	5000	20000	0	prim	100	0	0	0.1090
7	81	5000	20000	0	prim	100	0	0	0.1090
8	9	5000	20000	0	prim	100	0	0	0.1250
8	32	5000	20000	0	prim	100	0	0	0.1250
8	82	5000	20000	0	prim	100	0	0	0.1250
9	29	5000	20000	0	prim	100	0	0	0.0780
10	34	5000	20000	0	prim	100	0	0	0.1560

3.4 continued

Tool Num	Pin/Hole Code	Hit Count	Spindl Rate	Phy Tool	Use	Feed Rate (IPM)	Linear Feed (IPM)	Reverse Feed (IPM)	Dia (IN)
10	84	5000	20000	0	prim	100	0	0	0.1560
11	36	5000	20000	0	prim	100	0	0	0.1880
11	86	5000	20000	0	prim	100	0	0	0.1880
12	40	5000	20000	0	prim	100	0	0	0.2500
12	90	5000	20000	0	prim	100	0	0	0.2500
13	199	5000	20000	0	prim	100	0	0	0.0930
14	92	5000	20000	0	prim	100	0	0	0.0890
15	91	5000	20000	0	prim	100	0	0	0.1200

3.5 Wire Wrap

The following default wire wrap bin table is included with the seed job.

Bin Number	Wire Length	

1	0.75	<-- actually .5 wire
2	1.25	
3	1.75	
4	2.25	
5	2.75	
6	3.25	
7	3.75	
8	4.25	
9	4.75	
10	5.25	
11	5.75	
12	6.25	
13	6.75	
14	7.25	
15	7.75	
16	8.25	
17	8.75	
18	9.25	
19	9.75	
20	10.25	
21	10.75	
22	11.25	
23	11.75	
24	12.75	
25	13.75	
26	14.75	
27	15.75	
28	16.75	
29	17.75	

SECTION IV

VAX TO PCB ENGINEER TRANSLATION

4.1 Create New PCB Engineer Job

Log in to the Engineer product and select PCB Engineer. Next, select Create and from Network Job. Select is3 as the source node and select the green check. Select 00_pcb_40_seed as the Source job, key-in your jobname and select the green check in the upper right corner of the window.

4.2 Receive VAX Design File

Select CLICK from the top of the 8-button menu and, when prompted, enter your VAX username and password. Key-in "curdir write" and press Return, this will change the protections of this jobs directory. Then, key-in "vget (vax filename)" and press Return. Finally, key-in "mv (vax filename) design.dgn".

4.3 Receive The Schematic Netlist

Follow the procedure outlined in Section I, paragraph 1.3.

Note: Attach new format before netlisting, old formats will cause netlist errors.

4.4 Create The Libraries

Follow the procedure outlined in Section I, paragraph 1.4.

4.5 Compile The Netlist

Follow the procedure outlined in Section I, paragraph 1.5.

4.6 Verify The Job Parameters

Follow the procedure outlined in Section I, paragraph 1.6.

4.7 Run Replace Component

Under the 8 button menu select

PLACEMENT

REPLACE COMPONENT

Replace all the cells with the same cells.

ex. Replacement List
N24PC, N24PC

after the replacement list is complete, hit the green check.

WARNING: Any modified cell needs to be placed in the library before Replace component is run.

4.8 Netload The Board

Follow the procedure outlined in Section I, paragraph 1.9.

4.9 Schematic Component Difference

Follow the procedure outlined in Section I, paragraph 1.10.

4.10 Back Annotate

Follow the procedure outlined in Section I, paragraph 1.11.

4.11 Re-Place The Mounting Holes

Enter the design file, then delete and re-place all mounting holes (Reference Section I, paragraph 1.7.D).

4.12 Replace the Board Outline & Routing Border

You may use the "copy contour" command from the following path: ENG, setup, contour, copy contour. Copy the existing board outline & routing border, and delete the old.

SECTION V
USING PCBGET

5.1 Create Blank PCB Engineer Job

Log-in to the Engineer product and select PCB Engineer. Next, select "Create" and then "From" "Network Job". Select isj as the source node and then select the green check. Select 00_blank_job as the Source job, key-in your jobname (the same job_name that the job had when it was "pcbput" to the VAX) and select the green check in the upper right corner of the window.

5.2 Receive The Job From The VAX

Select CLIX from the top of the 8-button menu and, when prompted, enter your VAX username and password. Then, key-in "pcbget" and press Return. The job is now restored.

SECTION VI

TYPICAL WIRE-WRAP JOB FLOW

6.1 Create The New Schematic:

Seed jobs exist on is3 for wire-wrap applications. Each seed job is unique per the wire-wrap board part number. Each seed job has a blank sheet 1 and a sheet number 99 which contains the schematic of the power and ground system of that particular board.

If you have not drawn any of the schematic, then "Create", "From network job", on "Source node" "is3", from "Source job" - select the job name which matches the part number of the wire-wrap board. Then key-in the appropriate job name for this job and select the green check. Next, draw your schematic, as appropriate, in sheets 1-98.

If the schematic already exists, then sheet 99 must be added to it. To do this, follow the procedure outlined above, except give it a dummy job name. While still in this dummy job, enter DES and pull up sheet 99. Then use the "Save As" command to save sheet 99 as sheet 99 of the wire-wrap job you are working on. Exit DES and delete this dummy job.

Create an INTELLIGENT flat schematic, refer to the D/131 DES User's Guide, section VII, titled Intelligent Schematic Requirements. Also, verify that all of the required Component Dictionary, Component Supply File and Layout Cell Library entries have been made.

NOTE: The cathode of diodes and the positive side of polarized capacitors must be pin number 2.

6.2 Netlist The Schematic:

First, you must determine if a net equivalence file needs to be generated. The PCB Engineer system requires that netnames of "VCC" and "GND" be used for the +5V digital power source. If you, or sheet 99, used other names for these nets (i.e. +5V, 5V, V1, gnd, Gnd), then a net equivalence file must be created. A typical example is a wire-wrap board which has 4 planes/busses. Sheet 99 would have been created with net names of V1, V2, V3 and GND.

6.2 continued

You may have used +5V, +15V, -15V and GND in your schematic. A net equivalence file is required. Go to a CLIX window and type "iedit job_name.equ" (The name of the net equivalency file MUST start with the job_name or else it will not be saved by the DESPUT command). Then type the following:

```
VCC +5V V1
+15V V2
-15V V3
```

When the netlist is created, the +5V and V1 nets will be renamed to VCC in the netlist output file. Also, V2 will be renamed +15V and V3 will be renamed - 15V. If this is not done, V2 and +15V will become 2 separate, unconnected, nets in the netlist. Similarly, VCC, +5V and V1, as well as -15V and V3, would all be separate, unconnected, nets.

To exit from "iedit", select the file folder which does not have any lines on it. Then select the delete window ICON in the upper left corner.

Generate the netlist and specify "net.equ" as the "NET EQUIV FILE".

6.3 Create The New Wire-Wrap Job (same job name as the flat schematic):

Seed jobs exist on is3 for wire-wrap applications. Each seed job is unique per the wire-wrap board part number.

"Create the new job "From network job", on "Source node" "is3", from "Source job" - select the job name which matches the part number of the wire-wrap board. Then key-in the appropriate job name for this job and select the green check.

6.4 Receive The Schematic Netlist:

Follow the same procedure as outlined in Section I, paragraph 1.3.

6.5 Create The Libraries:

Follow the same procedure as outlined in Section I, paragraph 1.4.

6.6 Compile The Netlist:

Follow the same procedure as outlined in Section I, paragraph 1.5.

6.7 Define Job Parameters:

Follow the same procedure as outlined in Section I, paragraph 1.6.

6.8 Board Area:

Follow the same procedure as outlined in Section I, paragraph 1.7, omit paragraph B.

6.9 Place The Components:

Follow the same procedure as outlined in Section I, paragraph 1.8.

6.10 Netload The Board:

Follow the same procedure as outlined in Section I, paragraph 1.9.

6.11 Schematic Component Difference:

Follow the same procedure as outlined in Section I, paragraph 1.10.

6.12 Back Annotate (This is to assure that the design is good prior to executing potentially destructive steps):

Follow the same procedure as outlined in Section I, paragraph 1.11.

6.13 PCBPUT the job to the VAX (Makes a backup copy of the job, in case of a catastrophe):

Follow the same procedure as outlined in Section I, paragraph 1.10.

6.14 Generate Power And Ground SLIs:

Generate power and ground SLIs only, using "minimum spanning tree" and select "Delete existing SLIs".

6.15 Find/Correct Multiple Connect Points:

The only way to generate power and ground SLIs is by "minimum spanning tree". This method is not exactly what we want. It does not limit the number of wraps which can go on one pin. A program has been written to identify those pins with more than 2 wraps on them and report the X and Y coordinates of those pins.

Enter a CLIX window, when prompted, enter your VAX username and password. Then key-in "slxy", the results will be displayed and printed.

Enter the design file and "modify" the SLIs, which appear on the printout, in such a way as to eliminate the multiple connect points.

Then, return to the CLIX window and key-in "slxy" again, to verify that all of the multiple connect points have been resolved.

6.16 Generate The Remaining SLIs:

Generate the remaining SLIs, using "chaining". Select "Generate all signal nets" and DO NOT select "Delete existing SLIs".

Note: No more than 2 wraps per post are allowed.

6.17 Create Wire-Wrap Punch Tape File:

From the 8-button menu, select "CAM Post Processors", then "Wirewrap Utilities" and finally "Wirewrap".

From the Wirewrap menu select:

Machine name	sl_wwm-600
Wire Order LEVEL 1	(long wires down first)
Wire Order LEVEL 2	
Wire Length	
Side of Board	Back
Ref-Pin Origin	(i.e.) U1 - 1 (Place origin of IC at furthest upper left-hand corner as possible)

Then, select the green check.

6.18 Punch The Wire-Wrap Tape:

Enter the File Manager and select "Punch". Then select the following:

File to Punch	Wrap File Color 0
Punch Machines	Paper Tape Punch
Punch Format	Wire Wrap

Before selecting the green check, prepare the punch machine to punch a tape.

6.18 continued

From the File Manager, select "Print", and print the "Wirewrap Summary" file to the "Eng_Laser" printer.

Note: If the chad bucket is full, holes won't punch properly.

6.19 Top Drawing Creation:

Follow the procedure outlined in Section I, paragraph 1.28.

6.20 What To Send To FAB:

1. Wire-Wrap Tape
2. Wire-Wrap Summary Listing
3. Top Drawing - used only to determine proper board orientation for wrapping.

SECTION VII

CREATING WIRE-WRAP SEED JOBS

7.1 Create The New Schematic:

Use the part number of the wire-wrap board as the job_name. Create a schematic with sheets 1 and 99. Leave sheet 1 blank and draw the schematic of the power and ground system, of the wire-wrap board, on sheet 99. Use "J" numbers, for the wire-wrap power and ground pins, starting at J101 (example: VCC could be J101-J206 and GND could be J301-J406). Be sure to include any connections to edge connectors. For the "type" field of the power and ground pins, use "bdx-pp01". Then "netlist" the job.

7.2 Create The Wire-Wrap Board Design File:

Follow the same procedures that you would to create a PCB.

Exceptions:

1. Create the job from network job "ww_40_seed", located on the server.
2. Draw the outline of the wire-wrap board, showing physical size and locations of power, ground and connector pins, on level 20.
3. Place all power and ground pins as well as any connectors which connect to the power or ground system.
4. Route the board. No T junctions or vias.
5. Verify that the "ACCESS" privilege to this job, and the DES job, are set to "others read".
6. Move the PCB and DES seed jobs to the server.

SECTION VIII

PCB RELEASE DRAWING CREATION

- 8.1 Using the File Manager, receive a file named "Top E Size", "Top D Size" or "Top C Size", as appropriate, from the job named 00_Top_Drawing found on is_3.
- 8.2 Go to clix window and type drift_ref to attach the drafting format. (Then select Graphics from the 8 button menu and select the top drawing from the menu. Fill in the appropriate text fields and file information in lower right corner.
- 8.3 Add generic notes (NOPC1) from HARDWARE.CEL and create a hole size chart (see example). Also delete the first two fields in the parts list and replace with (LMPC1) also from HARDWARE.CEL. To modify NOPC1 or LMPC1, the cell will need to be dropped. Modify as required. Add (REV1) from HARDWARE.CEL in upper right hand corner. At this point, fill in rest of the parts list, revision block, and add any special requirements that may be needed.
- 8.4 From the menu, scale the reference file (PCB), if possible. Make the reference file at least 2 to 1 for clarity. Using the Move Reference File command, move the PCB file to a location that doesn't interfere with the notes or parts list but leaves enough room for dimensions. Identify NC.ORIGIN and mounting hole diameter. Dimensions are from NCORIGIN (see example).
- 8.5 To create a releasable NC printout, go to clix window and type NCHEADER. This will create an NCREPORT File in file directory.
- 8.6 After completion of steps 8.1 thru 8.5, the engineer should look over the plots and sign or redmark as required. The final release package should consist of plots of the top sheet, the schematics and a printout of the NCREPORT sheet (example sheet provided).

APPENDIX I

SAMPLE FORMS

ZFB0:(131026)APERTURE.DOC;4
T54

Page 1

19-NOV-1990 14

DATA FORMAT

Format: 2.3
Truncation: Leading
Step Mode: Absolute

D_Code	Width	Flash/Draw	Geometry
D10	0.040	Flash	Round
D11	0.050	Flash	Round
D12	0.075	Flash	Round
D13	0.086	Flash	Round
D14	0.100	Flash	Round
D15	0.005	Draw	Round
D16	0.010	Draw	Round
D17	0.015	Draw	Round
D18	0.020	Draw	Round
D19	0.025	Draw	Round
D70	UNUSED		
D71	UNUSED		
D20	0.125	Flash	Round
D21	0.150	Flash	Round
D22	0.175	Flash	Round
D23	0.040	Draw	Round
D24	UNUSED		
D25	0.050	Draw	Round
D26	0.075	Draw	Round
D27	0.100	Draw	Round
D28	0.125	Draw	Round
D29	0.150	Draw	Round
D72	UNUSED		
D73	0.062	Flash	Round
D100	0.050	Flash	Square
D101	0.062	Flash	Square
D102	0.075	Flash	Square
D103	0.086	Flash	Square
D104	0.100	Flash	Square
D105	0.125	Flash	Square
D106	0.020 X 0.050	Flash	Rectangle
D107	0.050 X 0.020	Flash	Rectangle

Appendix I: Sample Forms

ZFB0:[131026]TWO_LAYER.DOC;4
4:12

Page 1

13-DEC-1989 1

DD _____ Name _____ x _____

Aperture File: TEQ.IAD

Data Format: 2.3 Leading

Step Mode: Absolute

Special Aperatures: None

File	Description
1	DD_A00
2	DD_B00
3	SM_A00
4	SM_B00
5	DD_C00

LTC START: _____

LTC FINISH: _____

LTC TIME: _____

PLOT START: _____

PLOT FINISH: _____

PLOT TIME: _____

PIECES OF FILM: _____

SIZE OF FILM: 1/2

FULL

Appendix I: Sample Forms

_ZFBO:[131026]FOUR_LAYER.DOC;5

13-DEC-1989 14:12

Page 1

DD _____ Name _____ X _____

Aperture File: TEQ.YAD

Data Format: 2.3 Leading

Step Mode: Absolute

Special Aperatures: None

File Description

1	DD_A00
2	DD_B00
3	DD_C00
4	DD_D00
5	SH_A00
6	SH_D00
7	DD_E00

LTC START: _____	LTC FINISH: _____	LTC TIME: _____
PLOT START: _____	PLOT FINISH: _____	PLOT TIME: _____
PIECES OF FILM: _____	SIZE OF FILM: 1/2	FULL

_ZFBO:[131026]SIX_LAYER.DOC:4

13-DEC-1989 14:12

Page 1

DD _____ Name _____ X _____

Aperture File: TEO.IAD

Data Format: 2.3 Leading

Step Mode: Absolute

Special Apertures: None

File	Description
1	DD_A00
2	DD_B00
3	DD_C00
4	DD_D00
5	DD_E00
6	DD_F00
7	SH_A00
8	SH_F00
9	DD_G00

LTC START: _____	LTC FINISH: _____	LTC TIME: _____
PLOT START: _____	PLOT FINISH: _____	PLOT TIME: _____
PIECES OF FILM: _____	SIZE OF FILM: 1/2 FULL	

_ZFBO:[131026]EIGHT_LAYER.DOC;4

13-DEC-1989 14:14

Page 1

DD _____ Name _____ X _____

Aperture File: TEQ.IAD

Data Format: 2.3 Leading

Step Mode: Absolute

Special Apertures: None

File	Description
------	-------------

1	DD_A00
---	--------

2	DD_B00
---	--------

3	DD_C00
---	--------

4	DD_D00
---	--------

5	DD_E00
---	--------

6	DD_F00
---	--------

7	DD_G00
---	--------

8	DD_H00
---	--------

9	SM_A00
---	--------

10	SM_H00
----	--------

11	DD_I00
----	--------

LTC START: _____ LTC FINISH: _____ LTC TIME: _____

PLOT START: _____ PLOT FINISH: _____ PLOT TIME: _____

PIECES OF FILM: _____ SIZE OF FILM: 1/2 FULL

RELEASE DATE _____
SHEET 1 OF 1

5) RELATED CHANGES:

1. 2. 3. 4. 5. 6. 7. 8.

ADD TO AUTO DIST.

SPECIAL INSTRUCTIONS:
(THIS ISSUE ONLY)

(OPTIONAL)

2610W-171-250 KRB1 1984-05e-171-W0192

ENT 1234

REF ID: A66113

KANSAS CITY DIVISION
KCD-573 (4/89)

- 1) ENTER DRAWING SIZE 12, A, B, C, D, E, F OR J1.
- 2) ENTER STORAGE MEDIA FOR SPECIFICATION OR GRAPHIC CAD DRAWING TAGS, CMS, CMGS, ICE, IGR, TSO, TSOG, WP, WPG, B60, B60G)
ENTER MLT FOR MULTI-SHEET GRAPHIC DRAWING CONSISTING OF
INDIVIDUAL SHEETS WITH DIFFERENT STRG MEDIA(S).
- 3) ENTER SOURCE MEDIA(S) FOR MLT DRAWING OR FOR GRAPHIC PORTION(S) OF
CMS0, TSOG, WPG OR B60G SPECIFICATION.
(VALID ENTRIES, AGS, DAS, IBM, ICE, IGR, MAN).
- 4) ENTER CONTROL NUMBER SUFFIX IF APPLICABLE.
(6) INCLUDE APPROPRIATE PREFIX (AY, CH, PL, PS, SS, ETC.).
- 7) DRAWING RELEASE CODE AS DEFINED IN DS-103.

**DATE
FILMED**

11 / 10 / 93

END