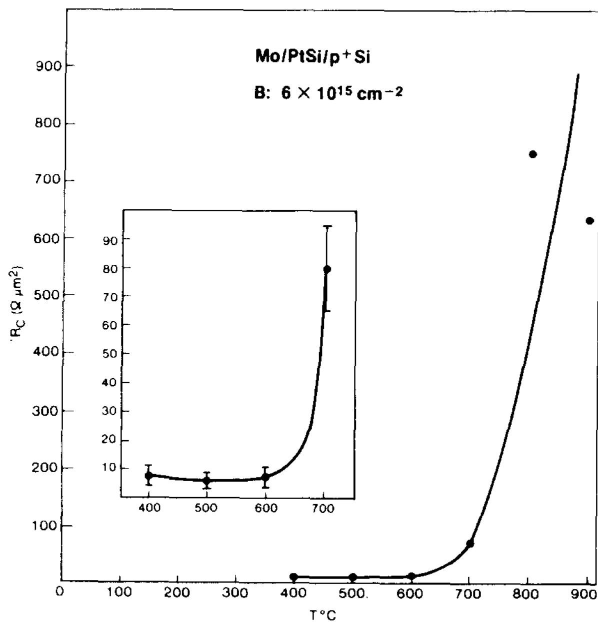

FIG. 4. Specific contact resistance of Mo/PtSi/p^+ Si contacts as a function of anneal temperature.

shown in Figs. 3 and 4, above 700 °C the contact resistance rises markedly beyond useful limits ($< 100\,\Omega\,\mu m^2$) for VLSI. Some samples were directly sintered at 700 °C for 120 min. The results of this experiment were similar to those obtained at this temperature from progressively sintered samples described above. It thus seems that the Mo/PtSi metallization system is metallurgically stable under moderate heat treatments up to 700 °C.

The temperature effect obtained in this study is similar to that measured by Mochizuki *et al.*[3] for direct molybdenum contacts to n^+ silicon, where beyond 700 °C the contact resistance for the Mo/Si system rose sharply. Mochizuki *et al.* suggested that the effect was due to formation of molybdenum silicide in the contact areas. Similar reactions seem to happen in the Mo/PtSi/Si system. Prolonged heating at elevated temperature seems to be promoting the migration of Mo atoms through the PtSi barrier. Thus, the PtSi/Si interface is degraded as a new Mo/Si, or rather $MoSi_2$/Si, is possibly formed, giving rise to similar results as reported by Mochizuki and his coworkers. In summary, our results indicate that the Mo/PtSi metallization system is suitable for VLSI applications. It has desirable thermal properties in addition to the good ohmic contacts that PtSi usually provides.

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Rapid isothermal anneal of ^{75}As implanted silicon

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Silicon wafers implanted with ^{75}As have been annealed with a Varian IA-200 isothermal annealer. The anneal occurs in vacuum using radiation from a resistively heated sheet of graphite. The anneal quality depends on the graphite heater temperature and exposure time. If the anneal time is too short implantation damage remains and if the time is too long measurable losses of As occur causing the sheet resistance to increase. The loss of As can be prevented by depositing 0.05 μm of SiO_2 on the wafer before annealing.

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As semiconductor device dimensions shrink, the need for precise control of dopant profiles becomes more important. In recent years various methods of rapid annealing of ion implantation damage with minimal dopant redistribution have been explored.[1-3] These techniques include the use of lasers and electron beams operated in both the pulsed and continuous modes. In these processes the absorbed energy is confined to the near surface region where the temperature will reach 900 °C or more for the continuous lasers and electron beams. For pulsed beam annealing the near surface ac-

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tually melts, leading to redistribution of the dopant in the thin molten region. There has also been considerable interest in the technique of isothermal annealing, where the entire wafer is heated to 900 °C or greater for times on the order of 1–10 s.[4] This type of annealing has been accomplished using high intensity arc lamps[5] and large area scanned electron beams.[6,7] Tsaur *et al.*[8] have annealed As implanted silicon by placing the sample in contact with a graphite strip heater in a forming gas ambient. Recently Fulks *et al.*[9] reported using a resistively heated graphite sheet as a blackbody radiation source for annealing ion implanted silicon. The wafer is heated by uniform absorption of the infrared radiation throughout the bulk of the wafer.

In this letter we will discuss our results for ^{75}As implanted silicon that has been annealed with a Varian IA-200 isothermal annealer. This system is similar to the prototype system which was described earlier by Fulks *et al.*[9] The radiation source is a slotted sheet of graphite whose temperature is monitored with a tungsten rhenium thermcouple. The annealing takes place in a vacuum $\sim 2\times 10^{-5}$ Torr. The wafer is ~ 1 cm from the heater during the anneal and all heat transfer is by radiation. A molybdenum shutter is used to control the exposure time and molybdenum reflectors are located around the heater and wafer to minimize energy loss. The wafers enter and exit the vacuum system by automatic interlocks identical to those used on a Varian/Extrion Wayflow end station for an ion implanter.

The silicon wafers used in this experiment were 3 in., (100) boron doped, 7–17 Ω cm. The bare wafers were implanted with ^{75}As at an energy of 100 keV and doses ranging from 1×10^{14} to 2.5×10^{15}/cm^2. The wafers were annealed with the graphite heater temperature ranging from 1100 to 1350 °C as measured by the tungsten rhenium thermocouple. The exposure times ranged from 5 to 30 s. A four point probe was used to measure the sheet resistance after annealing. Rutherford backscattering-ion channeling was performed with a 2-MeV He$^+$ beam to determine the residual damage, dopant diffusion, and percentage of substitutional arsenic in the lattice.

Figure 1 shows sheet resistance versus anneal time for three different implant doses and a heater temperature of 1150 °C. After a 5-s exposure the wafer still had a milky appearance indicating the near surface region was amorphous and we were unable to obtain a sheet resistance reading. After a 10-s anneal the wafers appeared visually as single crystal silicon, although the minimum sheet resistance was not achieved until the anneal time reached 15 s. For anneal times of 20 s or greater the sheet resistance increases from the minimum achieved at 15 s. Similar results were achieved with different heater temperatures, although the minimum shifted to shorter times with increasing heater temperatures and longer times with decreasing heater temperatures. The standard deviation in sheet resistance across the wafer was less than 2%. The sheet resistance value of 85 $\Omega/\square$ achieved for the 1×10^{15}/cm^2 implant, 15-s anneal is comparable to a 90 $\Omega/\square$ sheet resistance achieved by conventional thermal annealing at 1000 °C, 10 min in N_2. Slip lines were observed on wafers annealed with a heater temperature of 1300 °C or greater unless the exposure time was 10 s or less.

Figure 2 presents channeling spectra for He$^+$ scattering from silicon samples implanted with ^{75}As to a dose of 1×10^{15}/cm^2. The as-implanted spectra as well as those spectra obtained from samples exposed to the heater for 5, 10, and 15 s with a heater temperature of 1150 °C are shown. The as-implanted yield reaches the random yield indicating the silicon has been rendered amorphous to a depth of ~ 0.11 μm. After a 5-s anneal the amorphous region decreases by only 0.01 μm indicating annealing has just begun to occur by solid phase epitaxy. During the first 5 s the wafer temperature is just starting to rise and solid phase epitaxy does not occur until the temperature is greater than 500 °C. This explains why we were unable to obtain a sheet resistance reading for this time and temperature since the dopant still resides in an amorphous region. As mentioned earlier this result was expected since the wafer still had a milky appearance. After a 10-s anneal the channeling spectra indicate the removal of essentially all of the implant damage except for a small increase in the scattering yield in the depth range 0.11–0.14 μm. This is assumed to be due to defects generated dur-

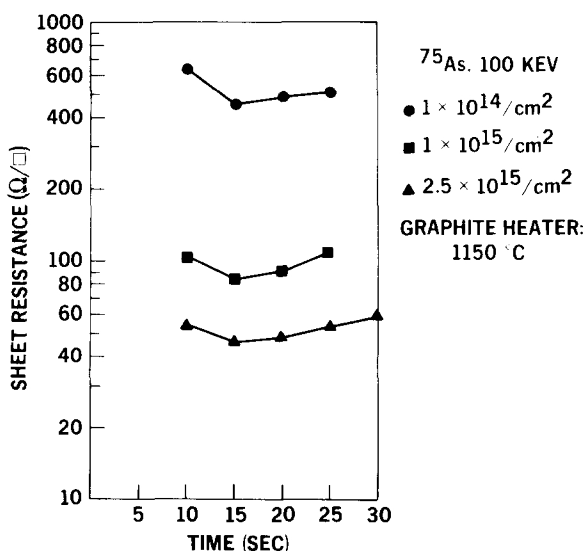

FIG. 1. Sheet resistance vs anneal time for the graphite heater at 1150 °C.

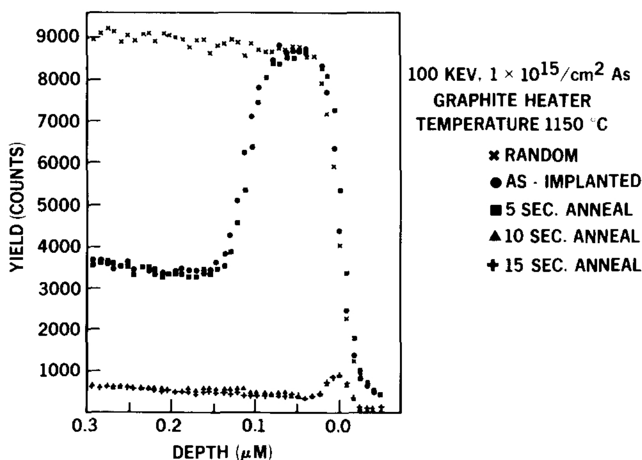

FIG. 2. 2.0-MeV He$^+$ channeling spectra for Si samples implanted with 1×10^{15}/cm^2 As and isothermally annealed with the graphite heater at 1150 °C. The He$^+$ beam was aligned with a ⟨110⟩ axis.

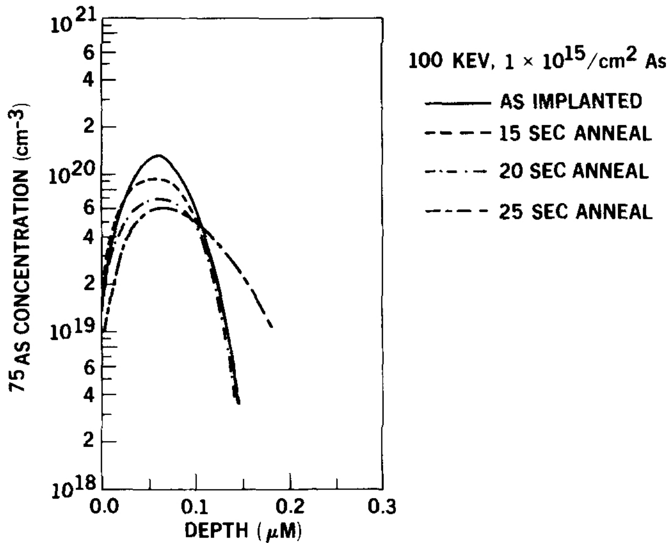

FIG. 3. ^{75}As concentration profiles after rapid isothermal annealing. The graphite heater temperature was 1150 °C.

ing the implant at the amorphous single crystal silicon interface by beam induced heating. This is similar to the spectra obtained after cw laser annealing although the scattering yield is not as pronounced.[10] Therefore, we conclude that during the second 5 s the wafer temperature is well in excess of 500 °C and complete regrowth has occurred. However, the time and temperature combination was not yet sufficient to remove all of the implantation induced defects. After a 15-s anneal the channeling spectra show no evidence of residual damage or defects and the χ_{min} was less than 5% indicating good single crystal silicon. The χ_{min} for virgin silicon was measured to be 3%. There was essentially no change in the channeling spectra for longer anneal times.

The ^{75}As profiles for wafers implanted to a dose of $1\times10^{15}/cm^2$ and annealed with the heater at 1150 °C are presented in Fig. 3. The As profile does not change measurably from the as-implanted profile after a 5- or 10-s anneal. Since only 0.01 μm of silicon has annealed after 5 s, none of the As is substitutional in this case. After a 10-s anneal 68% of the As was located on a substitutional lattice site as determined from the channeling measurements. Some diffusion of As toward the surface has occurred after a 15-s anneal and a slight drop in the peak concentration has also occurred. The As is 78% substitutional in this sample. However, there is approximately an 8% loss of As as measured by RBS. After a 20-s anneal a further drop in the peak concentration was observed and 21% of the As has been lost. The 25-s anneal at 1150 °C produces a significant diffusion of the implanted dopant and 29% of the As has been lost. The change in the As profile between a 20- and 25-s anneal implies a diffusion coefficient of $\sim9\times10^{-13}$ cm^2/s which is significantly higher than the intrinsic diffusion coefficient for As in Si at 1150 °C. However, the concentration enhanced diffusion coefficient predicted by the model of Tsai *et al.*[11] is $\sim8\times10^{-13}$ cm^2/s for As concentrations of $\sim7\times10^{19}$/cm^3 which is in excellent agreement with our data. In these last two samples 78% of the As was substitutional. The fact that the As concentration decreases at the surface relative to the bulk concentration indicates As is being lost from the surface. The loss of implanted As was even more pronounced at higher temperatures where nearly 60% of the implanted dopant was lost during a 25 s, 1200 °C anneal. This resulted in an increase of more than 50% in the sheet resistance. Due to the rapid diffusion of As at these temperatures more As would reach the surface where it would be lost. This loss of As explains the increase in sheet resistance with increasing anneal time that was seen in Fig. 1. We have minimized the loss of As by depositing 0.05 μm of sputtered SiO_2 on the wafer after the implant and before the anneal. In this case the sheet resistance is essentially constant for 15-, 20-, and 25-s anneal times.

In summary we have used a Varian IA-200 isothermal annealing system to anneal ^{75}As implanted silicon wafers. If there is no cap on the wafers, the sheet resistance decreases, reaches a minimum, and then increases with increasing anneal time. This is explained by the fact that for shorter times (< 10 s) the implantation damage does not completely anneal. For times greater than 15 s a significant amount of As has been lost into the vacuum system. The loss of As increases with anneal time and heater temperature. The loss of As can be prevented by depositing 0.05 μm of SiO_2 on the wafer prior to annealing.

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