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SEU and SEL Response of the Westinghouse 64K E^{2}PROM, Analog Devices AD7876 12-bit ADC, and the Intel 82527 Serial Communications Controller*

F.W. Sexton, G.L. Hash, M.P. Connors, J.R. Murray,
J.R. Schwank, P.S. Winokur, and E.G. Bradley
Sandia National Laboratories
Albuquerque, NM 87185-1083

Abstract

The Westinghouse SA3823 64K E^{2}PROM radiation-hardened SONOS non-volatile memory exhibited a single-event-upset (SEU) threshold in the read mode of 60 MeV-cm^2/mg and 40 MeV-cm^2/mg for data latch errors. The minimum threshold for address latch errors was 35 MeV-cm^2/mg. Hard errors were observed with Kr at V_P = 8.5 V and with Xe at programming voltages (V_P) as low as 7.5 V. No hard errors were observed with Cu at any angle up to V_P = 11 V. The system specification of no hard errors for Ar ions or lighter was exceeded. No single-event latchup (SEL) was observed in these devices for the conditions examined. The Analog Devices AD7876 12-bit analog-to-digital converter (ADC) had an upset threshold of 2 MeV-cm^2/mg for all values of input voltage (V_{in}), while the worst-case saturation cross section of ~2×10^{-3} cm^2 as measured with V_{in} = 4.49 V. No latchup was observed. The Intel 82C527 serial communications controller exhibited a minimum threshold for upset of 2 MeV-cm^2/mg and a saturation cross section of about 5×10^{-4} cm^2. For latchup the minimum threshold was measured at 17 MeV-cm^2/mg, and cross section saturated at about 3×10^{-4} cm^2. Error rates for the expected applications are presented.

I. Introduction

As space missions become more complex, system designers are opting for relatively simple hardware designs that require sophisticated software. This reliance on software-intensive designs also gives more flexibility to respond to design changes, especially important for short lead-time missions. Often, system software is written to reprogrammable non-volatile memory devices, so that software can be upgraded anytime before launch and even on-orbit if uplink capability is provided. On-orbit reprogramming capability also allows the designer to respond to hardware problems or changes in the mission profile that requires an unforeseen maneuver. This flexibility has been the key to mission success in the ALEXIS mission, for example [1].

Other space applications require fast high-resolution analog-to-digital converters (ADCs) to convert sensor information to a digital format for subsequent processing and transmission to earth stations. Finally, serial data links are used extensively to connect various payloads to communication downlinks, and to interconnect system and payload processors for overall control and housekeeping functions on a spacecraft.

This paper reports on the single-event-upset (SEU) and single-event-latchup (SEL) response of three devices that are being considered for space applications: the Westinghouse 64K E^{2}PROM, Analog Devices AD7876 12-bit ADC, and the Intel 82527 Serial Communications Controller. Expected error rates for specific environments are presented.

II. Experimental Details

Devices tested in this study were exercised using an hp 82000 model D50 ASIC tester.

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The physical test setup consisted of the hp 82000, a special 100-ohm low-noise ribbon cable, a device-under-test (DUT) board with DUT socket. A custom vacuum plate with ribbon cable connectors was used to pass test signals into the vacuum chamber and connect with the DUT board. Timing was maintained by calibrating timing signals at the DUT socket. Various vector sets were developed for each part type to exercise specific data paths. These are described in the results section below. Where devices were heated, a ceramic strip heater was mounted between the DUT and socket. DUT temperature was monitored with a thermocouple between the heater and DUT. In cases where devices were not heated, temperature was only monitored.

Single-event-effects (SEE) tests of the SA3823 were performed at Lawrence Berkeley Laboratories 88-inch cyclotron in the Aerospace SEU test chamber. Tests of the AD7876 and Intel 82527 were performed at the Brookhaven National Laboratories tandem van de Graaff accelerator single-event-upset test facility. Ions and energies used for these tests are summarized in Tables 1 and 2.

TABLE 1. Ions used for the SA3823 SEE tests at Lawrence Berkeley National Laboratories.

Ion	Energy (MeV)	LET(Si) MeV-cm²/mg	Range (μm)
Ar	175	15	45
Cu	283	30	42
Kr	366	40	43
Xe	603	63	50

III. Results

A. Westinghouse SA3823 E²PROM

The SA3823 is an 8K x 8 bit CMOS/SNOS E²PROM designed by Sandia [2] and fabricated at Westinghouse in a radiation-hardened double-level metal process. A block diagram of major elements of the SA3823 is shown in Figure 1. Control circuitry is omitted for clarity. The SA3823 is designed to be read one byte at a time and written one page (64 bytes) at a time. The memory address is stored in the address latches ($A_{0\text{-}12}$), which control the page and byte addresses. In a read operation, one byte of data is directly output via the sense amplifiers and output buffers. Data is not latched into data buffers. To accomplish a write operation, 64 data bytes are loaded into the page buffer data latches (for a total of 512 data bits) and then written into a page of the memory array. The byte address is determined by address $A_{0\text{-}5}$, while the page address is controlled by the address $A_{6\text{-}12}$.

TABLE 2. Ions used for the AD7876 and Intel 82527 SEE tests.

Ion	Energy (MeV)	LET (Si) (MeV-cm²/mg)	Range (μm in Si)
C	99.6	1.44	186.2
F	141.9	3.35	122.8
Mg	160.6	6.0	83.3
Cl	213.6	11.4	64.8
Ni	269	26.5	42.9
Au	348.5	82.2	28.4

Three types of errors can occur in a typical E²PROM as a result of a heavy-ion strike.

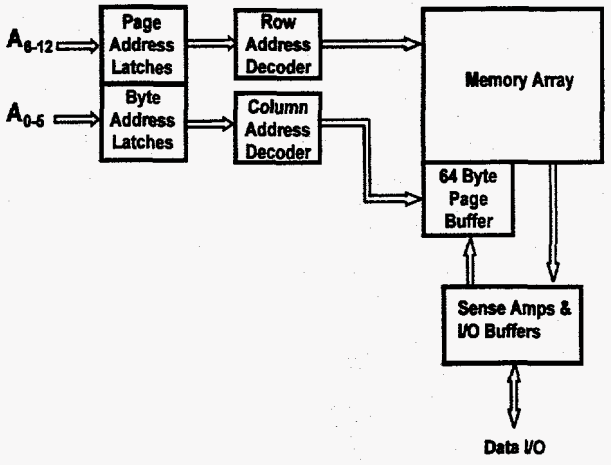

Figure 1: Functional block diagram of the SA3823 64K E²PROM. After Ref. [2].

Errors can occur while reading the memory due to a heavy-ion strike to address or data latches in the page buffer. This is called a read error. Errors can also occur due to strikes in the sense amplifiers and output buffers during a read operation. The contents of the memory cell itself is unchanged by this type of error and no permanent damage results. Errors can occur during a write operation, also due to a heavy-ion strike to address or data latches. In this type of error the memory cell is not damaged, but the information stored in the memory is corrupted. The third type is a single-event gate rupture that occurs during a write operation. This hard error results in permanent damage to a memory cell or, in some cases, to a group of memory cells (for example, an entire column may be inoperable). Direct upsets in E^2PROM memory cells are not likely with existing technologies, given the amount of charge stored on the floating gate and the limited path length through the floating gate material.

The test sample consisted of six devices from diffusion lot 21116, date code 4892, packaged in a 32-pin side-brazed DIP. For the SA3823 read error test, a checkerboard pattern was written to the memory array before exposure. A continuous loop on the read cycle was performed during exposure with power supply voltage (V_{DD}) set to 4.75 V and write voltage (V_W) set to - 4.0 V. Because the LET (linear energy transfer) threshold for a read upset was relatively high, it was difficult to observe this type of error without damaging the part due to hard errors. A few errors were observed at an effective LET of 60 MeV-cm^2/mg or greater (Figure 2 solid circles). This is consistent with errors to the sense amplifiers in this design. A more effective read test could have been performed by lowering V_W to 0 V, but the test vectors wouldn't function properly under this bias condition.

As discussed earlier, write errors can result from upsets in either the data latches or the address latches. For the data latch tests, a background checkerboard pattern was written to the memory array, then an inverse checkerboard pattern was written to the data latches (not to the memory) prior to exposure. The part was then exposed to a total fluence of 10^7 ions/cm^2. After the exposure, the contents of the data latches were written to the first page of memory. Errors in the stored pattern in the first page of memory were counted as data latch errors. The error cross section for these types of errors at V_{DD} = 4.5 V are plotted in Figure 2 as filled squares. Minimum upset threshold for data latch errors was 40 MeV-cm^2/mg, while saturation cross section was ~ 6x10^{-6} cm^2.

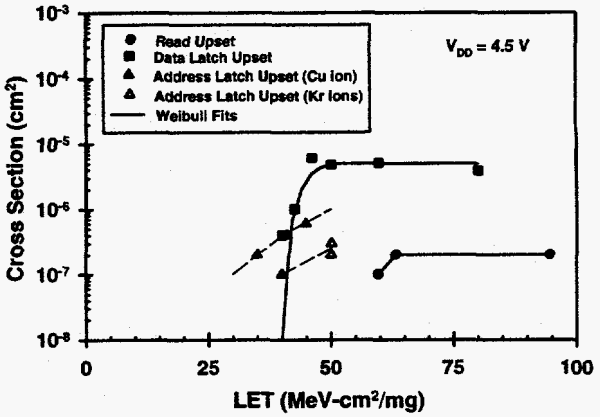

Figure 2: Error cross section for three types of upset in the SA3823 as a function of ion LET. The dashed lines are a guide to the eye, while the solid lines are a Weibull fit to the data.

In the address latch tests, a pattern of all zeros was written to the memory array, then a pattern of all ones was written to the data latches before exposure. The address latches were written to all zeros (00_H), and then the part was then exposed to a fluence of 10^7 ions/cm^2. After exposure and before the address latch contents were reset, a write operation was completed and the entire contents of the memory were read. If a page other than 00_H was written to all ones, an address latch error occurred and the number of bits that were upset was determined from the page address containing all ones. For example, a page address of 26_H indicated that 3 address latch bits were upset (26_H is equivalent to a binary

code of 00100110). As seen in Figure 2, the minimum upset threshold for address latch errors was 35 MeV-cm^2/mg with Cu ions (filled triangles). The address latch upset data taken with Kr ions (open triangles) did not intercept the lower LET Cu data. Although the statistics for this data is sparse, it suggests an ion species dependence for the address latch errors, with more errors observed with Cu than with Kr at the same effective LET. Ion dependent effects have been observed in the past [3]. However, further tests should be performed to improve the statistics of the data. Data was insufficient to determine saturation cross section.

Hard error dependence was studied by cycling on a write/read sequence over the entire array. In this test, the array was written to a checkerboard pattern, then the contents of the memory was read out. Both V_{DD} and V_W were varied over a range of programming voltages (V_P), equal to the absolute sum of V_{DD} and V_W. In these tests, we began with low V_P and proceeded from high to low angles of incidence for a given ion species. V_P was increased and the procedure repeated until a hard error was detected, or the next heavier ion species was selected and the sequence begun again. In the initial tests, once a hard error occurred in a part, the part in the test chamber was changed and a new series of tests begun. Later in the week, the test program was modified so that hard errors could be masked out and the same part could be used for several tests. Hard error data is summarized in Table 3. No hard errors were observed with Cu up to V_p = 11 V or with Kr at V_p = 8.25 V at any angle. Hard errors were observed with Kr at V_p = 8.5 V and with Xe at V_p as low as 7.5 V. The errors observed with Xe did not occur during the hard error test described above, but were observed during read error and data/address latch tests. The devices were exposed to several shots with Xe before these hard errors were observed, and are probably due to upsets in the write control logic that cause the part to initiate a write sequence. These errors are called write logic upsets in Table 3, below.

TABLE 3. Summary of hard error tests for the SA3823.

Serial Number	V_p (V)	Ion/ Angle	Result
446, 507	11	Cu/all angles	passed, no HE
549	8.0	Kr/all angles	passed, no HE
549	8.25	Kr/0°	passed, no HE
549	8.5	Kr/0°	3 pages
549	9.0	Kr/30°	1 page
507	9.0	Kr/30°	1 bit
517	9.0	Kr/48°	1 bit
446	7.5	Xe/48°	3 pages Write logic upset
516	9.0	Xe/48°	2 columns Write logic upset

A comparison of the hard error failure threshold voltage (V_{ft}) with theory is shown in Figure 3. For this plot, we assume that V_{ft} is equal to the lowest programming voltage at which a hard error was observed for a given ion and angle of incidence. Shown on the x-axis is the inverse of normal incidence LET. The solid lines were calculated using the model developed by Wrobel [4] for composite nitride/ oxides stacks and the measured oxide and nitride values for the Westinghouse process. As seen in Figure 3, the limited IC data does not match the theory very well. This difference may be due to the fact that the dielectric stack for this technology has a capping oxide between the nitride and polysilicon gate material, while the samples studied in Wrobel's work were simpler structures without this capping oxide. Further studies are necessary to

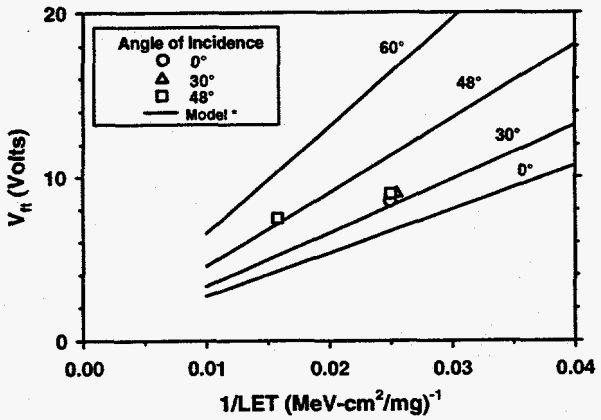

Figure 3: Expected failure threshold voltage (solid lines) for a composite nitride-oxide dielectric structure is compared to the measured hard error data (symbols) for the SA3823. The model is after Ref [4].

develop an improved model for failure threshold voltage for this technology.

B. AD7876 12-bit ADC

The AD7876 is a 12-bit successive-approximation analog-to-digital converter [5] fabricated in the non-hardened LC²MOS process. Major functional elements of the AD7876 are shown in Figure 4.

The test sample consisted of three parts of the AD7876-BQ. Due to time limitations, only one part was tested. The AD7876BQ is packaged in a 24-pin narrow ceramic dual-in-line package (DIP) from date code 9210 and marked on back with DF15032.1, Taiwan. Parts were delidded at Sandia prior to test. Part functionality was verified by exercising it with various test patterns prior to irradiation.

For SEU tests, positive power supply voltage (V_{DD}) was set at 4.76 V and the negative power supply (V_{SS}) was set at -4.76 V for worst-case conditions. Clock frequency was set at 2.5 MHz. Device temperature was monitored during testing with a thermocouple mounted between the device and socket. Nominal DUT temperature was 25°C. Latchup tests were performed with power supply voltages set to 5.5 V and -5.5 V, respectively, at a nominal temperature of 25°C.

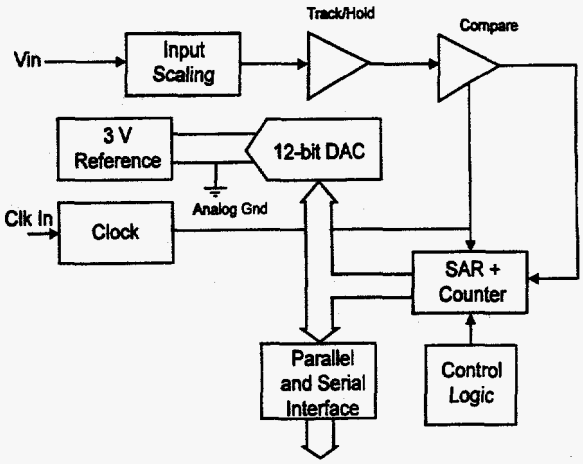

Figure 4: Major functional elements of the AD7876 12-bit ADC. After Ref. [5].

The AD7876 ADC was tested with a fixed DC input voltage (V_{in}) while continuously clocking the device to initiate a conversion cycle. The digital output was compared to the expected value at the end of each clock cycle. Any differences in output above the noise level were counted as an error. Dependence of upset sensitivity with input voltage, which determines the expected digital output, was characterized, as shown in Table 4.

TABLE 4. Mapping of V_{in} to expected data for the AD7876 ADC.

AD7876	
V_{in} (V)	Expected Value
-9.76	82x
-0.00	FFx
+0.05	00x
4.49	39x
8.79	70x

Measured error cross section for the AD7876 is shown in Figure 5 as a function LET and expected data (in hexadecimal notation). Note that in these tests the lower 4 bits were not tested due to noise problems. Accordingly, the last digit of expected data is represented as an 'x.' The worst-case pattern observed during these tests corresponded to an expected value

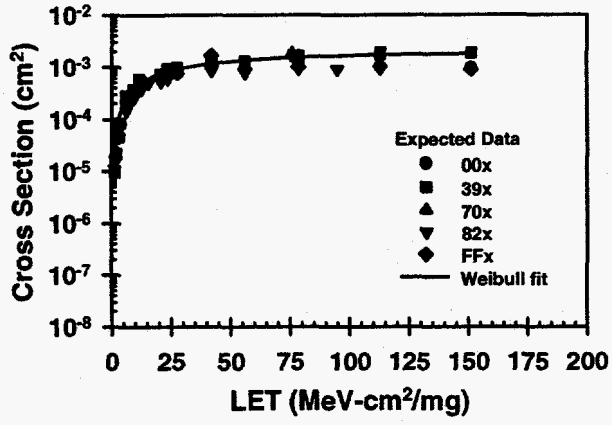

Figure 5: Error cross section for the AD7876 12-bit ADC as a function of expected data. The line is a Weibull fit to the "39x" data.

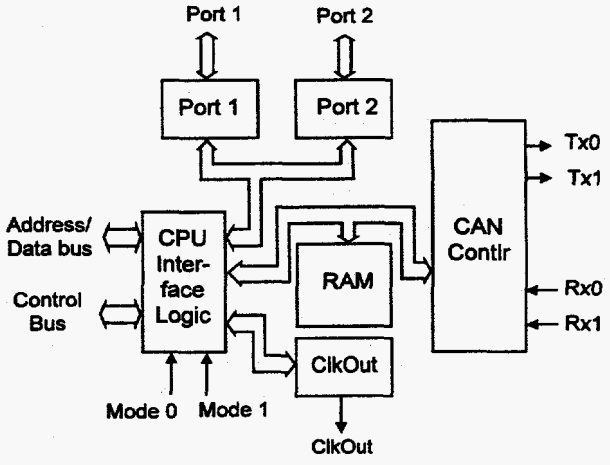

Figure 6: Functional block diagram of the Intel 82527 serial communications controller. After Ref. [7].

of 39x (V_{in}= 4.49 V). Minimum upset threshold was 2 MeV-cm²/mg, while saturation cross section was $2x10^{-3}$ cm². No latchup was observed with any input voltage during these tests.

The noise problem we encountered may have several sources. Digital switching noise may have caused some problems, since the analog and digital grounds were not separated on the DUT board used in these tests. [In subsequent tests at BNL, a DUT board with separate analog and digital grounds did not completely solve this noise problem on a different part type.] Noise could also emanate from equipment on the vacuum chamber, such as pumps and diagnostic electronics. A possible solution that arose in subsequent discussions [6], was to use decoupling capacitors on all inputs, especially the analog voltage input.

C. Intel 82527 Serial Communications Controller

The Intel 82527 serial communications controller performs serial communications according to the CAN 2.0 specification to allow interfacing to a microprocessor [7]. This part is fabricated at Chandler, AZ with the commercial (non-hardened) SAMP-B CHMOS III process in 10-μm epitaxial silicon. A functional block diagram of the 82527 is shown in Figure 6.

The 82527 includes 15 message registers, each consisting of 8 bytes. Three different patterns were loaded into these registers: a pattern of all ones, all zeros, or alternate ones and zeros. After loading a pattern the tester began cycling on a read operation until an error was detected. The original pattern was rewritten and the sequence repeated.

The test sample consisted of two devices. Both were marked with Intel control number Q9327. Parts were marked with customer control number DK123437. Parts were packaged in plastic leadless chip carriers (LCC) that had been delidded with an acid etching process by Analytical Solutions, Albuquerque, to allow the heavy-ion beam to impinge on the integrated circuit.

The upset cross section and latchup response for the Intel 82527 are shown in Figures 7 and 8. These data were corrected for energy loss in the overlayers based on technology information provided by the manufacturer [8]. With a checkerboard data pattern, a sharp upset threshold (Figure 7) was observed beginning at about 2 MeV-cm²/mg and saturating at about $5x10^{-4}$ cm². No dependence on temperature was observed from 25 to 90°C. No data could be obtained above 25 MeV-cm²/mg due to latchup.

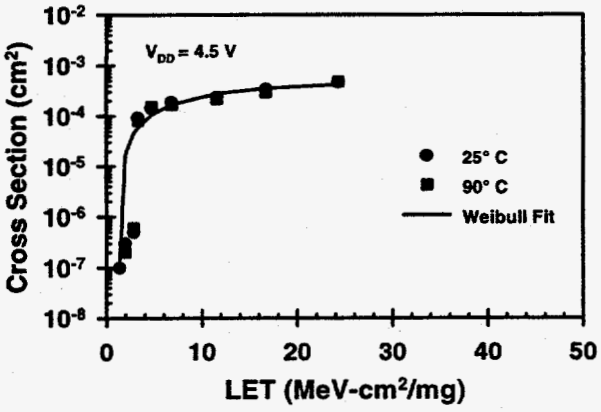

Figure 7: Upset cross section for the Intel 82527 serial communications controller as a function of temperature. The line is a Weibull fit to the data.

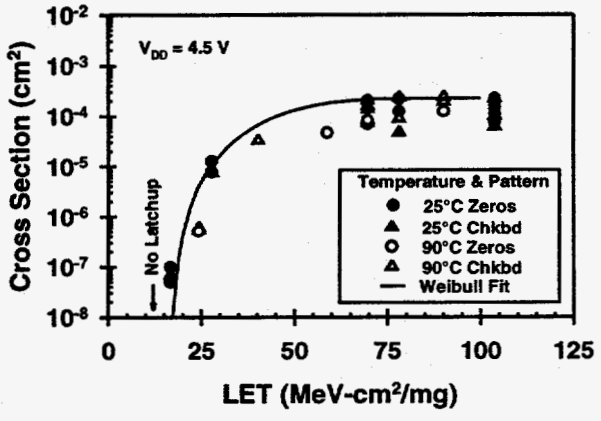

Figure 8: Latchup cross section for the 82527 serial communications controller as a function of temperature and data pattern. The solid line is a Weibull fit to the data.

As seen in Figure 8, latchup threshold was about 17 MeV-cm²/mg and saturation was about $3x10^{-4}$ cm². Temperature had a small effect on saturation cross section, but little effect on threshold.

IV. Error Rate Calculations

Error rate calculations were made for the GPS block 2R orbit at 20190 km and 55° inclination, and 300 mil aluminum shielding. Adams' 10% worst-case model [9] was assumed for the environment. The SPACERAD 2.0 code from Severn Communications [10] was used for these calculations. Weibull fits to the data of Figure 2 were used as inputs to the code and error rates were calculated using an integral cross section curve. The data were adjusted for number of bits in the data path (8 bits for a read error, and 512 bits for a data error) to derive units of error/bit-day.

Error rates are summarized in Table 5. For this high altitude orbit, environment conditions (orbit-averaged vs. worst-case and quiet vs. stormy geomagnetic conditions) had little effect on the error rate. Charge collection depth had a significant effect on error rates (up to two orders of magnitude), but the expected error rates were always well below the standard specification of 10^{-10} errors/bit-day. A worst-case assumption of 1-μm charge-collection depth and no funneling results in expected error rates of $8.8x10^{-13}$ and $7.5x10^{-14}$ errors/bit-day for read errors and data errors, respectively.

TABLE 5. Expected error rates for the SA3823 64K E²PROM in errors-bit-day.

Error Type	Charge-collection depth (μm)	Orbit avg quiet geomag.	Orbit w.c. stormy geomag
Read Error	1	8.47E-13	8.81E-13
Read Error	4	8.04E-15	8.12E-15
Data Error	1	7.41E-14	7.50E-14
Data Error	4	2.30E-15	2.33E-15

The combined error rate for the AD7876 ADC due to galactic cosmic rays (GCR) and trapped protons is given in Table 6, assuming a charge-collection depth of 2 μm. Calculations were performed for a FORTE orbit at 800 km and 65.5° inclination. For GCR, Adams' 10% worst-case environment model [9] was used. Two shielding cases were modeled: 1) the normal 160 mil Al shielding from the spacecraft and electronics boxes, and 2) an additional 250 mil Ta shielding. Error rates averaged over the

full orbit with quiet geomagnetic conditions are compared with worst-case orbit response and stormy geomagnetic conditions. The proton environment assumed was the AP8MIN spectrum and the IGRF/DGRF magnetic field model. Proton sensitivity was calculated using the empirical approach developed by Petersen [11], where threshold energy is estimated from the heavy-ion 10% threshold. Since this technique cannot estimate saturation cross section for protons, a Bendel one-parameter model [12] was assumed.

For the AD7876, error rates increased ~ 3x for the orbit worst-case flux under stormy geomagnetic condition compared to the orbit averaged flux under quiet geomagnetic conditions.

TABLE 6. Combined error rates for both protons and heavy ions expected for the AD7876. Numbers are in units of errors/device-day.

Environment Conditions	160 mil Al	250 mil Ta
orbit avg, quiet geomag	9.5E-3	7.2E-3
orbit worst-case, stormy geomag	2.9E-2	2.0E-2

Detailed results of error-rate calculations are shown in Table 7, for the two environment models and two shielding thicknesses. The first four rows show error rates due to GCRs. Calculations were also performed for different values of depletion layer depth (Ld) and funneling depth (Lf). Referring to Table 6, varying charge collection depth from 2 to 10 μm had little effect on error rate, as did assuming 0 or 1 μm for funneling. Adding 250 mil Ta shielding decreased the error rate by about 15%, from 9.5×10^{-3} to 7.2×10^{-3} errors/device-day for a charge collection depth of 2 μm. By far the largest effect on error rate was the assumed environment, increasing by a factor of 2-3x from orbit-average, quiet geomagnetic conditions to orbit worst-case, stormy geomagnetic conditions.

TABLE 7. Detailed error rates for the AD7876 ADC. Numbers are in units of errors/device-day.

Ld (μm)	Lf (μm)	160 mil Al	250 mil Ta
Orbit average / quiet geomagnetic storm conditions			
2	0	9.37E-3	7.15E-3
4	0	9.23E-3	7.12E-3
10	0	9.07E-3	6.94E-3
4	1	7.99E-3	6.09E-3
Proton error rate		1.16E-4	7.67E-5
Orbit worst-case / stormy geomagnetic conditions			
2	0	2.45E-2	1.67E-2
4	0	2.42E-2	1.66E-2
10	0	2.34E-2	1.62E-2
4	1	2.07E-2	1.42E-2
Proton error rate		4.54E-3	3.01E-3

The assumed environment had a larger effect on trapped-proton-induced errors than GCR-induced errors (see Table 7). Error rates increased about 40x from orbit-average, quiet geomagnetic conditions to orbit worst-case, stormy geomagnetic conditions. Adding 250 mil Ta shielding decreased error rates by about 35%. The estimated threshold for proton upset is 19 MeV using the Petersen approach [11] to estimating proton threshold from heavy-ion data. While the Bendel one-parameter model has been shown to be conservative for some devices [13], it is prudent to keep in mind the uncertainty of the proton estimates discussed above. Proton measurements should be made on devices that will be flown in systems to reduce the uncertainty of proton-induced error rates. However, GCR-induced upsets are expected to dominate error rates for the AD7876.

Calculated error rates for the Intel 82527 are shown in Table 8 for the Forte orbit with 160 mils Al or 250 mils Ta shielding, respectively. Error rates are given in units of errors/bit-day for the message registers in this part. For this

part, error rates are dominated by proton upsets. Proton threshold was estimated to be about 18 MeV, again using the Petersen method and the Bendel one-parameter model. As in the AD7876, shielding improved the error rates only marginally, while environment assumptions had a factor of 3x effect.

TABLE 8. Error rates for the Intel 82527 in the Forte orbit in units of errors/bit-day.

Environment	160 mil Al	250 mil Ta
GCR orbit average quiet magnetic	9.3E-7	7.0E-7
GCR orbit worst-case stormy geomagnetic	3.2E-6	2.1E-6
Trapped protons orbit average quiet geomagnetic	2.0E-4	1.3E-4
Trapped protons orbit worst-case stormy geomagnetic	7.8E-3	5.2E-3
Total orb average quiet geomagnetic	2.0E-4	1.3E-4
Total orb worst-case stormy geomagnetic	7.8E-3	5.2E-3

V. Summary

Upset and latchup data have been presented for three part types that are being considered or will be used in Sandia-designed subsystems. As expected, the commercial parts had low upset thresholds, ~ 2 MeV-cm²/mg, while the hardened SA3823 had a minimum upset threshold of ~35 MeV-cm²/mg for address latch upsets. Latchup was not observed in the SA3823 or the AD7876. Latchup threshold for the Intel 82527 was about 20 MeV-cm²/mg. Error rates for galactic cosmic ray and trapped protons were calculated where appropriate.

Acknowledgments

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