3000

MASTER

BDX-613-994 (Rev.)

STATIC CHARGE AND CURRENT
LEAKAGE EFFECTS RELATING
TO MANUFACTURE OF JFET
ASSEMBLIES

PDO 6984756, Final Report

M. L. Waddell, Project Leader

Project Team:

G. L. Asher
L. S. Carter
W. J. Kirk
F. H. Lewis
G. E. Pinick

Published May 1974

Prepared for the
United States Atomic Energy Commission
Under Contract Number AT(29-1)-613 USAEC

**Kansas City
Division**

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

STATIC CHARGE AND CURRENT
LEAKAGE EFFECTS RELATING
TO MANUFACTURE OF JFET
ASSEMBLIES

BDX-613-994 (Rev.)

Published May 1974

Prepared by:
L. S. Carter
Department 845

Project Leader:
M. L. Waddell
Department 845

Project Team:
G. L. Asher
L. S. Carter
W. J. Kirk
F. H. Lewis
G. E. Pinick

PDO 6984756
Final Report

NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Atomic Energy Commission, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

Technical Communications

**Kansas City
Division**

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

GB

**THIS PAGE
WAS INTENTIONALLY
LEFT BLANK**

**STATIC CHARGE AND CURRENT LEAKAGE EFFECTS RELATING TO
MANUFACTURE OF JFET ASSEMBLIES**

BDX-613-994 (Rev.), UNCLASSIFIED Final Report, Published May 1974

Prepared by L. S. Carter, D/845, under PDO 6984756

This work consisted of a study of the effects of static electricity on field effect transistors and investigation of precautions necessary to minimize surface leakage currents on the boards that contain these devices. Methods of preventing JFET degradation or catastrophic failure as a result of static discharge from the bodies of production personnel were developed. Some of the common sources of board contamination were identified, and cleaning and handling procedures were established.

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Atomic Energy Commission, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

THE BENDIX CORPORATION

KANSAS CITY DIVISION

KANSAS CITY, MISSOURI

A prime contractor for the
Atomic Energy Commission
Contract Number AT(28-1)-613 USAEC

THIS PAGE
WAS INTENTIONALLY
LEFT BLANK

CONTENTS

Section	Page
SUMMARY	11
DISCUSSION	13
SCOPE AND PURPOSE	13
ACTIVITY	13
<u>Static Study</u>	13
<u>Leakage-Current Effects</u>	30
ACCOMPLISHMENTS	38
<u>Static-Study Conclusions</u>	38
<u>Current-Leakage Effects Conclusions</u>	39
FUTURE WORK	40
REFERENCES	41

THIS PAGE
WAS INTENTIONALLY
LEFT BLANK

ILLUSTRATIONS

Figure		Page
1	Modified Petrick ⁸ Body Resistance Measurement Method	16
2	Static-Discharge Test Circuit	16
3	Degraded 2N2608 JFET	17
4	Voltage Versus Series Resistance for 2N4118A JFET Degradation	24
5	Static Voltage Versus Discharge Time, Person at 10-Percent RH	25
6	Isolation Box	26
7	Simplified Switching Diagram	27
8	Electrostatic Voltages Generated By a Person Walking	28
9	Electrostatic Voltages Generated By Repetitively Standing and Sitting	29
10	Resistivity-Test PC Board Pattern	31
11	Surface Resistivity Measurement Setup	32
12	Volume Resistivity Measurement Setup	32
13	Contaminant Study Test Setup	33
14	Typical Volume Resistivity Plot	35
15	Typical Plot of Surface Resistivity Versus Temperature	36
16	Surface Resistance Versus Relative Humidity at Selected Temperatures	37
17	Effects of Various Contaminants on Surface Resistance	38

THIS PAGE
WAS INTENTIONALLY
LEFT BLANK

TABLES

Number		Page
1	Human Body Capacitance	14
2	Human Body Capacitance and Equivalent Series Resistance	15
3	Effects of Capacitance and Voltage on JFET Degradation	20
4	Effect of Multiple Pulses on 2N4118A JFET.	22
5	Effects of Series Gate Resistance on 2N4118A JFET Static Degradation	23
6	Average Voltages Generated at Relative Humidity ≤ 10 Percent	30
7	Comparison of Printed Circuit Board Laminate Material.	34

THIS PAGE
WAS INTENTIONALLY
LEFT BLANK

SUMMARY

Electronic devices that contain junction field effect transistors (JFET's) are often characterized by high-impedance low-current operating conditions. Special precautions are necessary to prevent JFET damage from static discharges. Control of cleaning processes is necessary to minimize manufacturing-process contamination that may cause excessive current leakage and consequent degradation of device operation.

The findings of this work established the following:

- The susceptibility of junction field effect transistors to static discharges;
- The magnitudes of static charges accumulated under various environmental conditions;
- The effectiveness of various methods of reducing or eliminating static charge accumulation under different manufacturing environmental conditions; and
- The various types of manufacturing process contamination which augment leakage current.

An electrical model of the human body was developed and used to determine the static voltage levels that cause degradation or failure of JFET's. A method to continuously measure and graphically display static voltages was developed. Static voltages on personnel performing routine manufacturing activities were monitored in various environments to determine whether the static charges generated were sufficient to damage JFET's. Deionizers, wrist straps, conductive flooring, and conductive shoes were investigated for effectiveness in preventing static accumulation. Static charges greater than 3000 volts were measured on personnel performing routine activities in factory areas without static preventative measures or environmental controls. Some types of JFET's sustained damage from a 100-volt static discharge, although most devices did not degrade or catastrophically fail below 140 volts. A change in the gate-to-drain or gate-to-source breakdown voltage proved an accurate indication of degradation.

Deionizers accelerate the decay of static charges on personnel, but do not limit static generation. Conductive flooring and conductive chairs limit static accumulation to 500 volts during routine operator activities. When conductive shoes are worn also, the static accumulation is generally less than 60 or 100 volts--depending on the floor material. The additional use

of a grounded wrist strap further reduces the static accumulation to about 30 volts. With other factors equal, higher static charges are accumulated in a low-humidity environment.

The operation of JFET circuits containing discrete resistances in the 100-megohm range can be impaired if stray leakage current exceeds a few nanoamperes. Surface resistances on printed wiring boards and components must be at least 10 gigohms if this condition is to be satisfied. The effects of several manufacturing process contaminants on surface resistance were found to approach this 10-gigohm limit. The process contaminants investigated were moisture, rosin, flux, and fingerprint residues (both body excretions and foreign substances such as handcreams). Polyurethane foam encapsulation and general environmental contaminants resulting from open storage were not detrimental to the proper electrical operation of JFET assemblies.

Of all the process contaminants investigated, only fingerprint residue consistently reduced surface resistance to values near or below the 10-gigohm limit. Reductions in surface resistance caused by moisture and rosin can approach this limit and can be considered potential problems. Preventative measures and effective cleaning techniques reduce the effects of process contaminants.

DISCUSSION

SCOPE AND PURPOSE

This work was done to establish safe techniques to support production of assemblies containing junction field effect transistors (JFET's). These devices are being used more extensively in new product designs.

JFET devices are static sensitive and the application circuitry is characterized by impedances in the gigohm range and operating currents as low as a few nanoamperes. A static study determined the static voltage level at which JFET degradation or catastrophic failure occurs, the static voltage levels generated by manufacturing personnel, and the methods of limiting static buildup on the bodies of the operators.

These high-impedance, low-current JFET circuits necessitate the use of printed circuit boards with surface resistances greater than 10 gigohms to limit current leakage between circuit paths to less than one nanoampere. A study identified major manufacturing contaminants that cause excessive current leakage.

ACTIVITY

Static Study

Device Susceptibility

A literature search resulted in an understanding of the causes and magnitudes of static electricity on personnel. An energy-storage model of the human body was developed to obtain consistent results of the effects of static electricity on JFET's.

Published values of body capacitance and body resistance range from 100 to 10,000 picofarads and from approximately 0 to 18000 ohms.¹⁻¹⁴ Because of the large disparity in these published values, measurements were made to obtain typical values of body capacitance and body resistance. The body capacitance data in Table 1 were obtained with a Tektronix Model 130 LC Meter. The body capacitance and body resistance data shown in Table 2 were obtained by using the measurement method shown in Figure 1. The data from both measurement methods are comparable; therefore, a capacitance of 100 to 200 picofarads and a resistance of 100 ohms appear representative of values expected on personnel.

Table 1. Human Body Capacitance

Operator Position	Floor Covering	Body Capacitance (pF)	
		≈30 Percent RH	≈10 Percent RH
Standing Shoes on	Bare concrete	120	
	Vinyl over concrete		190
	0.75-inch plywood		118
	Grounded metal plate	160	215
	Guarded metal plate	70	103
Standing Stockings only	Bare concrete	150	
	Vinyl over concrete		405**
	0.75-inch plywood		125
	Grounded metal plate*		1430**
Sitting on chair Feet off floor	Bare Concrete	90	
	Bare concrete with guarded chair	50	
	Vinyl over concrete		110
	Vinyl over concrete with guarded chair		57
	0.75-inch plywood		99
	Grounded metal plate		125
Sitting on chair Shoes on floor	Bare concrete	140	
	Bare concrete on guarded chair	100	
	Vinyl over concrete		186
	Vinyl over concrete with guarded chair		150
	0.75-inch plywood		131
	Grounded metal plate		225
Chair only No Operator	Bare concrete	55	
	Guarded plate over bare concrete	40	
<p>*Two 4-mil (0.1 mm) polyethylene sheets between feet and plate</p> <p>**Values above 300 pF were measured with 260 pF in series with meter:</p> $C_{\text{body capacitance}} = (C_{\text{measured}}) (260) / (260 - C_{\text{measured}}).$			

Table 2. Human Body Capacitance and Equivalent Series Resistance

Test Condition	Voltage	I_{pk} (A)	Time Constant (Micro second)	R_H (Ohms)	C_H (pF)
Standing on bare concrete floor	200	0.18	0.18	110	162
	500	0.44	0.20	135	177
	1000	0.88	0.18	135	159
	2000	1.68	0.18	190	150
Sitting on chair on bare concrete feet off floor	200	0.176	0.16	135	141
	1000	0.88	0.15	135	132
	2000	1.84	0.15	87	138
Calibration:					
135 pF	500	0.48	0.16	40	135
270 pF	500	0.50	0.31	0	270
Note: Test method shown in Figure 1.					

After the electrical equivalent of the human body had been established, the susceptibility of JFET's to electrostatic discharge was determined. Four types of JFET's were used in these tests--2N2608, 2N3112, 2N3971, and 2N4118A. Using the circuit shown in Figure 2, various values of capacitors were discharged into the gates of samples of the four types. Each JFET received one discharge pulse at each test voltage, starting at 70 volts and increasing until the gate-to-source breakdown voltage at 5.0 microamperes decreased significantly or the reverse breakdown voltage was less than 3.0 volts. The first condition was the test for degradation, the second was the test for catastrophic failure. No series resistor (R_H) was used in the tests. Photographs of a 2N2608 JFET that was degraded during these tests is shown in Figure 3. Table 3 is the result of these tests. After finding the 2N4118A the most susceptible to damage from electrostatic discharges, an operator charged to various levels discharged himself through the gates of several 2N4118A JFET's. These experiments simulating actual conditions verified that the tests using an electrical model yielded valid results. These results also are shown in Table 3.

Text continues on page 19.

FULL VIEW AT LEFT IS AT 150X
 DETAILS BELOW ARE AT 1200X.

Figure 3. Degraded 2N2608 JFET

To determine whether static discharges have a cumulative effect on JFET's, five 2N4118A's were tested under multiple-pulse conditions. Each JFET received ten discharge pulses at each test voltage, starting at 70 volts and continuing at higher voltages until degradation or catastrophic failure occurred. The test circuit shown in Figure 2 was used. C_H was 218 picofarads. No series resistance (R_H) was used. These results are shown in Table 4. The single-pulse data from Table 3 also is shown for comparison. The voltage levels at which failures occurred were comparable for both methods of testing. All failures occurred during the first four pulses; therefore, a cumulative effect did not appear probable.

The effects of human resistances were investigated. The circuit of Figure 1 was used, with C_H fixed at 218 picofarads. The test voltage was increased after each pulse into the gate of each 2N4118A JFET until degradation or failure of the device occurred. Table 5 lists the failure voltages versus the series resistance. Figure 4 is a log-log plot of the data in Table 5.

A limited study on the relationships between static electricity and COS/MOS and MOS/FET devices was then conducted. As stated in RCA literature:¹⁵

The breakdown voltage of an MOS gate is generally on the order of 100 volts. . . . the MOS gate oxide will be shorted as a result of only one voltage excursion to the breakdown limit. . . . a very low-energy source (such as a static charge) is capable of developing this voltage. . . . a protection circuit. . . is incorporated in all RCA COS/MOS integrated circuits to eliminate this problem.

Several RCA CD4000A-series COS/MOS devices were evaluated. Results indicate the static discharge voltage at which degradation occurs is at least twice that of JFET's. If the precautions taken sufficiently protect a JFET from static discharge damage, the same precautions should protect a CD4000A series COS/MOS device.

A MOS/FET General Instrument MEM 520C P channel enhancement mode silicon insulated-gate FET was tested to obtain preliminary data on susceptibility to damage from static discharge. Initial data showed device degradation occurred from static discharges as low as 60 volts. Additional testing is necessary to determine a minimum failure voltage level, but the device is at least as susceptible as the 2N4118A JFET to static discharge.

Text continues on page 24.

Table 3. Effects of Capacitance and Voltage on JFET Static Degradation

Test Voltage	Static Discharge Test Circuit (By JFET Type)									
	2N2608			2N3112			2N3971			
Capacitance (pF)	97	218	425	97	218	425	97	218	425	
70										
85										
100										
120										
140										
160								D		
190								D		
230								D		
270	D							CD		
320		D						D	C	
380			DDD		DD			CDD	C	
450										
530		DD			DDDD	D	DD	D		
620		DDDDD						D	D	
730		DDDD			DDDD	DD				
860		D		D	D			D		
1000		DD		D	DDD		D	DDD		
1105	D	DD			DD					
1190					DD					
1275										
1360										
1445					CD			DD		
1530				D	CD			DD		
Each letter represents one data point: D = Degraded C = Catastrophic failure										

				Operator Discharge			
				2N4118A			
				Standing		Sitting	
	2N4118A			Power Supply Charge	Static Movement Charge	Power Supply Charge	Static Movement Charge
	97	218	425	190	118	110	99
	C CCD C D D C C C C D D D C C D D D C D C C C			D D C C D	C D D	D C D D D	

Table 4. Effect of Multiple Pulses on 2N4118A JFET

Test Voltage (Volts)	Single Pulse Mode	Number of Pulses at Test Voltage									
		1	2	3	4	5	6	7	8	9	10
70											
85											
100											
120											
140											
160											
190	D			DC							
230	CCCD		D								
270	DDCD		D		C						
320	DCDC										
380	CC										
450											
530											
620											
730											
860											
1000											
1105											
1190											
1275											
Each letter represents one data point. D = Degraded C = Catastrophic											

Table 5. Series Gate Resistance Versus 2N4118A Degradation Voltage

Test Voltage (Volts)	Series Gate Resistance (Ohms)					
	100	1.1k	27k	50k	100k	3.6M
140						
160						
190	X					
230	XXXX					
270	XXXX	X				
320	XXXX					
380	XX					
450		X				
530		XXX				
620						
730						
860						
1000						
1100						
1200						
1300						
1400						
1500			XX			
1600						
1700			XX	X		
1800						
1900						
2000						
2100						
2200				XX		
2300				X	XX	
2400				X	X	
2500				X	X	
2600						X
2700						
2800				X	X	
2900				X		
3000						X
3100						
3200					X	X
3300						
3400						X
3500						X
3600

Figure 4. Voltage Versus Series Resistance for 2N4118A JFET Degradation

Charge Accumulation Measurements with a Static Meter

A method to measure the static charges on personnel was developed. Previously published works described various methods of measuring instantaneous static voltages on personnel. One frequently employed method required that a person touch an electrostatic voltmeter lead each time a reading was desired. Another method was to have a person touch a capacitor of a known value. By measuring the charge on the capacitor, the charge on the person could be calculated. Both of these techniques gave only an instantaneous reading; whereas, in actual situations, the static voltage can be expected to vary with changes in personnel activity and environment. To develop a method to continuously monitor the static voltages on personnel, a Custom Materials, Incorporated CMI-7777M Static Meter was procured. This meter is a pistol-shaped instrument that indicates positive and negative static voltages up to 200 kilovolts without contacting the surfaces to be measured. A special high-resistance voltage-measuring element located in the barrel of the meter couples to the atmosphere by means of a radioactive beta emitter (tritium). A voltage assumed by the internal element is dependent on the strength of the voltage field. The voltage read on the meter of the CMI-7777M is the difference between the potential on the object under test and ground when the meter is held by a grounded operator. The meter scale to be read depends on the distance from the object being measured to the tip of the meter.

The calibrated distances are 2, 6, and 12 inches (51, 152 and 304 mm). Because of the difficulty encountered in keeping the distance between the meter and the voltage source (a person) constant, the meter was modified by attaching a copper plate to the front of the meter at a fixed, calibrated distance. A cable was attached to connect the object being measured to the plate. This method provides a visual indication of the static voltage levels existing on an object or a person.

Using this method, discharge curves of static voltages stored on a human under various environmental conditions were plotted, as shown in Figure 5. When generating the curves of Figure 5 it became evident that even a slight movement can affect the instantaneous static voltage level. Therefore, a continuous graphic method of recording static levels on a person was required. When using such a method, the effects of sitting down, standing up, and walking can be monitored, recorded, and analyzed.

Figure 5. Static Voltage Versus Discharge Time, Person at 10-Percent RH

Charge Accumulation Measurements With an Isolation Box

A Keithley Model 615 Digital Electrometer with a Model 2501 Static Detector Head and a Model 370 Chart Recorder was procured. The detector provides a 10,000:1 voltage-division ratio when held 0.375-inch (9.525 mm) away from a charged plane of at least 3-inches (76 mm) diameter. The electrometer measures the resulting voltage and the recorder provides a continuous graphical record of varying static voltages on a person performing typical activities.

There were two problems in this system:

- A 0.375-inch separation between the detector and the voltage source (a person) had to be maintained for accurate measurements.
- A ground reference drift began 15 seconds after zeroing. The detector was designed for short duration measurements; therefore, the manufacturer recommends rezeroing the detector after every 15-second measurement.¹⁶

A phenolic isolation box (Figure 6) was constructed. Phenolic was chosen for minimal piezoelectric and triboelectric effects. Cotton phenolic was chosen over linen phenolic for a higher volume resistivity. A copper disc of

Figure 6. Isolation Box

3.5 inches (88.9 mm) diameter was positioned inside the isolation box in front of the detector at a separation distance of 0.375 inches. A graphite-lubricated cable, used to minimize spurious potentials caused by internal cable friction, was used to connect the disc to the static source (a person). A momentary switch on the detector references the detector to the potential at its face. If the potential at the face of the detector is 0.0 volts when the switch is released, the detector is referenced to ground. A sequencer and a solenoid references the detector to ground every 10 seconds (Figure 7), without discharging the static source, thus preventing the detector drift. Varying electrostatic charges can thus be continuously monitored and graphically recorded.

Figure 7. Simplified Switching Diagram

Two typical graphical recordings are shown in Figures 8 and 9. Figure 8 is a recording of the electrostatic voltages generated by a person in a 10-percent rh environment walking on a vinyl tile floor with conventional street shoes. The average voltage generated was 300 volts. A typical maximum under these conditions is 400 volts. Figure 9 is a recording of the electrostatic voltages generated by a person repetitively sitting down and standing up while wearing street shoes. A standard nonconductive office chair was used, and the floor was covered with conductive Velostat* floor mats. The relative humidity was 10 percent. A large spike greater than the average voltage level occurs during the standing and sitting movements. This recording also demonstrates that under the specified conditions the polarity of the static voltage changes when a person stands up or sits down.

Figure 8. Electrostatic Voltages Generated By a Person Walking

*Trademark of Custom Materials, Incorporated, Chelmsford, Massachusetts.

Figure 9. Electrostatic Voltages Generated By Repetitively Standing and Sitting

Charge Reduction Methods

After the system for continuously monitoring static charges was developed, evaluation of methods to reduce or prevent static buildup was begun. Relative humidity proved a major factor in the magnitude of the static charges generated. As the relative humidity increases, the average static charge generated by a person decreases. For example, a person walking generated an average of 400 volts in a 10-percent relative humidity environment, but generated only 300 volts at 30 percent rh. The capability of obtaining and controlling humidity over a wide range limited this analysis of rh environmental effects.

Other investigations compared the effectiveness of various types of floors and shoes in preventing static charges. Table 6 summarizes the results of comparisons. There is an inter-relationship between static prevention techniques. For example, Table 6 shows that persons wearing regular street shoes generated lower static voltages on Velostat than on Conductile; however, when wearing conductive shoes, Conductile limits static voltages better than Velostat. Since sitting down and standing up generated higher static charges than other routine activities, a conductive chair was evaluated. The conductive chair, when used in conjunction with a conductive floor, resulted in a reduction of static charges by a factor of 10 in a 3.5-percent rh environment.

A wrist strap connecting the operator to earth ground was effective in minimizing static charges. A current limiting resistor in the wrist strap is strongly recommended for operator safety. Without such a resistor, an

Table 6. Average Voltages Generated at Relative Humidity ≤ 10 Percent

Floor Type	Shoe Type	Voltages During Operator Activities		
		Normal Walking	Sitting Down/ Standing Up ¹	Typical Maximum
Tile (Vinyl)	Regular Street	400	>500	>2000
Conductive Mat (Velostat ²)	Regular Street	50	200	400
Conductive Mat (Velostat ²)	Conductive	20	50	100
Conductive Tile (Conductile ³)	Regular Street	250	350	500
Conductive Tile (Conductile ³)	Conductive	20	30	60
¹ Includes use of conductive chairs; wrist straps were not worn by the operator. ² Trademark: Custom Materials Incorporated. ³ Trademark: Vinyl Plastics Incorporated.				

operator contacting a current source can result in sufficient current flow to cause electrocution. If there are earth grounds where an operator can create a low-impedance path from a current source to ground, the use of an effective ground-fault interrupt system should be considered. Such a system would also protect an operator wearing a defective wrist strap in which the current limiting resistor is shorted. Ground-fault interrupt devices were not investigated in this study; therefore, protection claims by the manufacturer should be investigated before installing such a device.

Leakage-Current Effects

In electronic assemblies containing JFET's and resistive components in the 100 megohm range, stray leakage currents greater than 1.0 nanoampere flowing between circuit paths can cause circuit malfunction or failure. This study determined the leakage current effects of different types of contaminants encountered in manufacturing environments or created by manufacturing processes.

Rosins and fluxes necessary in the soldering process were investigated, and the effects on leakage currents were determined. The change in leakage current caused by moisture absorption in printed circuit board laminate material was determined. The leakage effects of contaminants directly caused by a person, such as body salts and handcreams (categorized in this report as fingerprint residue), were determined.

Test Method Development

A method of measuring surface and volume resistivity in accordance with ASTM D257-66¹⁷ was developed to measure leakage current. Test boards 3.5-inches (90 mm) square in two stock thicknesses--0.031 and 0.062 inch (0.787 and 1.57 mm)--were constructed as shown in Figure 10. A gap was etched on one side of each test board. Five gap widths were investigated: 0.020 inch (0.51 mm), 0.040 inch (1.02 mm), 0.060 inch (1.52 mm), 0.100 inch (2.54 mm), and 0.250 inch (6.35 mm). These test boards were copper clad on both sides, tin/lead plated, and solder leveled. Sample boards were constructed for three types of board laminates: GH (MIL 2141893), which is the type of laminate required on the JFET assemblies of concern; GB (MIL 2141797); and GE (MIL 2141935). The last two are other laminates commonly used on electronic assemblies.

Figure 10. Resistivity-Test PC Board Pattern

The surface- and volume-resistivity measurement methods (Figures 11 and 12) were used in the test setup shown in Figure 13. Two dependencies, electrification time and test temperature, were verified. Electrification time (length of time voltage is applied before measurement) was found to affect the volume resistivity measurement. Figure 14 illustrates a typical time dependency. To negate the effects of this dependency, a standard electrification time of 5 minutes was used in all surface- and volume-resistivity tests. The second dependency concerned test temperature and surface resistance. The surface resistance (Figure 15) decreased with an increase in the test temperature. Because of this variable, the temperature for all subsequent testing at a constant temperature was fixed at 175°F (79.5°C) as a worst-case value of surface resistance.

Figure 11. Surface Resistivity Measurement Setup

Figure 12. Volume Resistivity Measurement Setup

Figure 13. Contaminant Study Test Setup

Type GH laminate material was compared to Types GB and GE to determine whether the resistivities are comparable. As shown in Table 7, the average surface and volume resistivities were similar for all three types. The average surface resistance is in the 10 teraohm range, which provides an acceptable design margin for the 10 gigohm operating limit.

Contaminant Evaluations

The first contaminant effect evaluated was moisture absorption by the printed circuit board laminate material. Figure 16 shows the extent of surface resistance reduction as the relative humidity increases. The surface resistance decreased by a factor of approximately 10 when the relative humidity increased from less than 10 percent to approximately 50 percent. Even at 50-percent rh the resistance level was still more than 10 gigohms.

Table 7. Comparison of Printed Circuit Board Laminate Material

Laminate Type	Surface Resistivity T_{Ω}	Volume Resistivity $T\Omega$ -in ($T\Omega$ -mm)	Surface Resistance $T\Omega$
GB	0.021	247 (6273)	6.9
GE	0.035	508 (12903)	11.5
GH	0.060	190 (4826)	20.0
Test Temperature: 175°F (79.5°C) Board Thickness: 0.031 inch (0.787 mm) Gap Width: 0.020 inch (0.51 mm)			

Leakage current effects from rosins and human-caused process contaminants were evaluated. Rosins included residues resulting from soldering operations and fluxes (nonactivated, mildly activated, and activated). The human-caused process contaminants referred to as fingerprint residue include not only body excretions such as salts, but also foreign substances such as handcreams. Fingerprint residue was obtained by having various personnel place thumbprints across the gap on uncontaminated test boards. Figure 17 illustrates the range of surface resistances after contamination and prior to any effort to remove the contaminant. The surface resistance of the test boards fell below the 10 gigohm minimum limit when contaminated with fingerprint residue, and approached this minimum limit when contaminated with soldering flux. Activated flux approaches the level of concern, but it is rarely used in electronic assemblies. Moisture effects approach the limit at 50-percent rh, and can be expected to become more of a problem at higher rh levels.

The effects of process contaminants such as those shown in Figure 17 can be controlled by effective prevention or removal techniques. Moisture contamination is inherent in manufacturing environments, but it can be reduced by a low-rh environment and by incorporation of high-temperature baking and drying techniques at critical stages in the assembly process.

Since rosins and fluxes are necessary to the soldering process, effective removal methods, as opposed to prevention techniques, must be used. Contaminant removal methods are being developed to improve encapsulant

Figure 14. Typical Volume Resistivity Plot

adhesion and prevent high-voltage corona. The results of these efforts will be applicable also to control of leakage currents, and will be considered in selecting the most-effective cleaning techniques with respect to assembly configuration and component density.

Since fingerprint residue represents the most serious problem in surface-resistance degradation, control is essential. Wearing hand protection (fingercots or gloves) is effective in limiting the occurrence of fingerprint residue, but an effective residue removal technique is required also. Because of the wide variation in the chemical content of fingerprint residue, any single solvent is effective in removing only specific portions of the residue. Multiple-solvent processes which are to be developed will be used in establishing the overall most-effective fingerprint residue removal procedure.

Text continues on page 38.

Figure 15. Typical Plot of Surface Resistivity Versus Temperature

Figure 16. Surface Resistance Versus Relative Humidity at Selected Temperatures

Figure 17. Effects of Various Contaminants on Surface Resistance

In another series of investigations, test boards decreased in surface resistance to the 100-teraohm range after 2-week open storage in various manufacturing areas. Since the resulting surface resistance is well above the 10-gigohm limit, leakage current effects due to open storage is not a concern. Also, five uncontaminated boards were encapsulated in polyurethane foam, and surface resistance was measured before and after encapsulation. Again, the surface resistance decreased, but not sufficiently to cause concern.

ACCOMPLISHMENTS

Static-Study Conclusions

As a result of the static study, several specific conclusions were reached.

- Static discharges as low as 100 volts can cause catastrophic JFET failure, although a typical minimum is closer to 140 volts.
- A system was developed and used to continuously monitor and determine the effectiveness of static prevention techniques in limiting static buildup to a specific voltage level.

- The effectiveness of a static reducing technique depends on other techniques being used. For example, when considering conductive floors and shoes, a Velostat floor is more effective when regular shoes are worn, and a Conductile floor is more effective with conductive shoes.
- A body capacitance of 100 to 200 picofarads and a body resistance of 100 ohms are values typical of a person.
- An accumulative effect of multiple static discharges into a JFET causing catastrophic failure is not probable.
- Portable deionizers are ineffective in limiting static buildup on personnel; increased relative humidity is much more effective.

The following conclusions on specific devices were reached:

- The 2N4118A JFET is more susceptible to damage from static discharges than the 2N2606, the 2N3112, or the 2N3971.
- The gate protection circuit in CD4000A Series RCA COS/MOS integrated circuits protects the device from static discharges to at least 250 volts.

Current Leakage Effects Conclusions

After determining that Types GB, GE and GH printed circuit board laminates have similar surface and volume resistivities and will not contribute significantly to the leakage current when clean, the following conclusions were reached concerning the current leakage effects of process contaminants.

- Fingerprint residue (containing body excretions such as salts and foreign materials such as handcreams) caused the greatest reduction in surface resistance and is the problem most difficult to control.
- Moisture absorption alone on printed circuit boards in a factory environment with up to 50-percent rh will not cause leakage currents in excess of 1.0 nanoampere under the operating conditions outlined.
- Neither open storage nor encapsulation in polyurethane foam significantly reduced surface resistance.

FUTURE WORK

The findings of this work are being applied in a new facility in which units containing JFET's and other high-impedance, low-current devices will be assembled. Precautions being taken to prevent static buildup include the use of conductive flooring, conductive furniture, and conductive shoes. Wrist straps will be worn by the operators while they are at their work stations. Use of a ground-fault interrupt system is being considered. Moisture effects will be minimal, since the relative humidity is less than 10 percent. Operators will wear hand protection to prevent contamination of printed wiring boards from fingerprint residue and will perform soldering and assembly activities at vertical-flow clean benches.

Several areas which could benefit from further effort came to attention during this work.

- Prevention of static discharges may be desired for numerous reasons. Common examples include prevention of accidentally discharging explosive devices, materials, or flammable gases and degradation of static-sensitive components such as JFET's. The degree of protection required may range from tens of volts to thousands of volts. There is no conclusive guide to determine the type of facility necessary to limit static discharge to a stated requirement. The development of such a guide is recommended.
- The development of a procedure and a standardized test setup to initially and periodically verify the effectiveness of a static-reducing facility is recommended.
- The cataloging of commonly-used devices according to susceptibility to static damage also is recommended. Catastrophic and degrading failure mechanisms should be established and their relationship to repeated discharges should be determined.
- The relationship between static buildup, preventative techniques, and humidity should be more-fully defined. Limitation of available facilities with controlled and variable humidity restricted this area of investigation.
- The effectiveness of ground-fault interrupt systems should be investigated for use in areas where conductive floors, metal furniture, and an earth ground present a potential shock hazard.

REFERENCES

SOURCES CITED

- ¹ Martin Lenzliner, "Gate Protection of MIS Devices," IEEE Transactions on Electron Devices, Volume ED-18, Number 4, April, 1971, pp. 249-257.
- ² A. R. Morse, comment on "Field Treatment of Electrical Shock Cases-1" by W. B. Kouwenhoven and W. R. Milnor, AIEE Transactions Power Apparatus and Systems, Volume 76, April, 1957, pp. 82-87.
- ³ Ralph H. Lee, "Electrical Safety in Industrial Plants," IEEE Spectrum, June, 1971, pp. 51-55.
- ⁴ Using Electrically-Operated Equipment Safely with the Monitored Cardiac Patient, Hewlett-Packard Company, Waltham, Massachusetts, March, 1970, p. 22.
- ⁵ A. E. Molinski, "Effects of Electricity on the Human Body," Mining Congress Journal, Volume 56, Number 7, July, 1970, pp. 64-68.
- ⁶ Gordon D. Friedlander, "Electricity in Hospitals: Elimination of Lethal Hazards," IEEE Spectrum, September, 1971, pp. 40-51.
- ⁷ Louis J. Montesi, "The Development of a Fixed Gap Electrostatic Spark Discharge Apparatus for Characterizing Explosives," Proceedings of the Sixth Symposium on Electroexplosive Devices, San Francisco, California, July 8-10, 1969, pp. 2-8.1.
- ⁸ John T. Petrick, "Discharge of an Electrostatically Charged Human," Proceedings of the Sixth Symposium on Electroexplosive Devices, San Francisco, California, July 8-10, 1969, pp. 3-5.1.
- ⁹ Francis B. Silsbee, Static Electricity, National Bureau of Standards Circular C438, June 10, 1942, p. 23.
- ¹⁰ C. F. Schroeder, Jr., "Energy Transfer in Electrostatic Arcs," Proceedings of the Fifth Symposium on Electroexplosive Devices, Franklin Institute, Philadelphia, Pennsylvania, June 13-14, 1967, p. 2-5.1.

- ¹¹ F. G. Eichel, "Electrostatics," Chemical Engineering, March 13, 1967, pp. 153-167.
- ¹² Boyd C. Taylor, "Electrostatic-Insensitive Detonator for Precise Synchronization," Proceedings of the Sixth Symposium on Electroexplosive Devices, San Francisco, California, July 8-10, 1969, pp. 1-10.1.
- ¹³ L. D. Pitts, "Demythologizing Electrostatics," Proceedings of the Sixth Symposium on Electroexplosive Devices, San Francisco, California, July 8-10, 1969, pp. 3-7.1.
- ¹⁴ "Static Electricity," National Fire Codes, Volume 9, Number 77, 1966, National Fire Protection Association, Boston, Massachusetts, 1970-71, pp. 44-77.
- ¹⁵ R. R. Painter, Gate-Oxide Protection Circuit in RCA COS/MOS Digital Integrated Circuits, Application Note ICAN-6218, RCA Solid State Division Somerville, New Jersey.
- ¹⁶ "Static Charge Measurements Using Keithley Equipment" Product Notes, Keithley Instruments, Incorporated, Cleveland, Ohio.
- ¹⁷ "Standard Methods of Test for DC Resistance or Conductance of Insulating Material," American Standards for Testing Materials No. D257-66, American Society for Testing and Materials, Philadelphia, Pennsylvania, 1972, Part 29, pp. 176-196.

SOURCES CONSULTED

Electrometer Measurements, Keithley Instruments, Incorporated, Cleveland, Ohio, 1972.

Standard Method of Test for Electrical Resistance of Conductive Resilient Flooring, American Society for Testing and Materials, Philadelphia, Pennsylvania, F150-72.

Floor Coverings, Resilient, Nontextile: Sampling and Testing, Federal Test Method Standard Number 501a.

AMC Safety Manual, United States Army Material Command, AMCR 385-224, June, 1964.

Ceramic Tile for Floors and Walls, Simplified Practice Recommendation R61-61, United States Department of Commerce, Washington, D. C.

R. M. Lumley and W. J. Neiswender, "Personnel Grounding-A Case History," IEEE Transactions on Industry and General Applications, Volume IGA-2, Number 5, September/October, 1966.

S. E. Rose, "Static Electricity Can Cause Bipolar IC Failures," Evaluation Engineering, May/June, 1971.

D. G. Stroh, "Static Electricity Can Kill Transistors," Electronics, January, 12, 1962.

L. C. Hamiter, Jr., "How Reliable are MOS IC's? As good as bipolars, says NASA," Electronics, June 23, 1969.

R. J. Nowac, "How Not to Get a Charge Out of Static Electricity," Machine Design, September 2, 1971.

C. F. Hedlund, "Proposed Chapter III, Static and Lightning Protection Grounding Static Grounding," sic. IEEE Conference Record of 1970 Industrial and Commercial Power Systems and Electric Space Heating and Air Conditioning Joint Technical Conference, IEEE, Incorporated, 70 C 8 IGA, 1970.

MOS/FET Devices are Destroyed by Static Electricity, Custom Materials, Incorporated, Chelmsford, Massachusetts.

"Gases", National Fire Codes, National Fire Protection Association, Volume 2, pp. 33-48, 1971-72.

D. M. Taylor and T. J. Lewis, "Electrical Conduction in Polyethylene Terephthalate and Polyethylene Films," Journal of Physics. D: Applied Physics, Volume 4, 1971, pp. 1346-1357.

Choong-Ki Kim and Martin Lenzlinger, "Charge Transfer in Charge-Coupled Devices," Journal of Applied Physics, Volume 42, Number 9, August, 1971, pp. 3586-3594.

E. Sacher, "Direct-Current Conductivity of Polyethylene Terephthalate," Journal of Macromolecular Science. Physics, Volume B4, Issue Number 2, June, 1970, pp. 441-448.

A. C. Lilly, Jr., and John R. McDowell, "High-Field Conduction in Films of Mylar and Teflon," Journal of Applied Physics, Volume 39, Number 1, January, 1968, pp. 141-147.

G. Legyel, "Schottky Emission and Conduction in Some Organic Insulating Materials," Journal of Applied Physics, Volume 37, Number 2, February, 1966, pp. 807-810.

V. Adamec, "Nature of Anomalous Conductivity of Polymeric Insulating Materials," Institute of Electrical Engineers Proceedings, Volume 112 Number 2, February 1965, pp. 405-407.

R. I. Witt, J. J. Chapman, and B. L. Raskin, "Measuring of Surface and Volume Resistances," Modern Plastics, Volume 24, Number 8, April, 1947, p. 141.