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**PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK
OF THE LOW COST SILICON SOLAR ARRAY PROJECT**

Technical Quarterly Report No. 3, April-June 1978
Motorola Report No. 2345/3

By
M. G. Coleman
E. M. Pastirik
R. A. Pryor

Work Performed Under Contract No. NAS-7-100-954847

Motorola Incorporated
Semiconductor Group
Phoenix, Arizona

U.S. Department of Energy

Solar Energy

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TECHNICAL QUARTERLY REPORT NO. 3

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by

M. G. Coleman, E. M. Pastirik, and R. A. Pryor

PREPARED BY

MOTOROLA INC. SEMICONDUCTOR GROUP
5005 E. McDowell Road
Phoenix, Arizona 85005

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Project No. 2345

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The previously reported study on wax masking has been critically reviewed. This system is based upon a wax-solvent technique. Further studies have been performed on wax masking, and a melted wax application has been found preferable to the wax-solvent technology.

Photoresponse data have been obtained for ion implanted phosphorous and arsenic into p-type test wafers as well as boron into n-type test wafers. The resulting cells, corrected for texture etching and antireflection coat addition, would be expected to perform as well as the best diffused cells in current production.

Improvements have been made in the plated metallization process which is being developed under separate contract. The immersion layer deposited by a new plating chemistry is uniform and adherent, showing promise for improved yield and performance, and reduced cost.

Texture etching technology advancements have been made, allowing the formation of smaller and more uniformly-sized textured peaks. This is done in a simple etching bath with no physical constraints. The smaller peaks have a very favorable impact upon other process steps, and can greatly reduce the incidence of handling-induced damage. These improvements are now being incorporated into the process sequence being developed on this program. A discussion of process verification is presented.

2.0 INTRODUCTION

There is a high probability that flat plate solar photovoltaic modules will become a major source of electricity generation throughout most of the world, and that the silicon solar cell will be preferred generating element. In order to provide a realistic framework on which to build an effective program of R&D and demonstration for silicon solar cell modules, a series of objectives has been established to lead to a 1986 goal of 50¢/peak watt. At this price, solar-generated electricity will be able to compete with electric power generated by any other means, provided the solar cell modules are sufficiently reliable (e.g., have a mean life of 20 years).

To reach the 1986 JPL goal will require several advancements: 1) a cheaper source of pure silicon, 2) a much more economical way of transforming the source silicon into large, thin, (essentially) single crystal substrates having a controlled geometry, 3) an economical, large module package that will protect the interconnected solar cells it contains for at least 20 years from degradation caused by exposure to the weather, 4) an automated process sequence that produces high efficiency, reliable, cheap solar cells, tests them, interconnects them, and encapsulates them, and 5) a large market, of the order of 500 Mw/year.

When the JPL/ERDA LSSA Project started, the Motorola Solar Energy R&D Department participated in the Phase I of the Automated Array Assembly Task. The Phase I study identified a few potentially powerful process sequences for silicon solar cell production, and experimentally verified the overall consistency of the process sequence. It concluded that no basic technological innovations were necessary for solar cell fabrication or encapsulation in order to meet the long range LSSA Project goals. Detailed economic analyses

were performed, based on today's technologies, and showed that it should be possible to meet the JPL cost projections for solar panels.

The overall conclusion of the Array Automated Assembly Task, Phase 1, was one of cautious optimism. The present program, for Phase 2, has as its objective the further development of specific process steps (in a specified, powerful process sequence) leading to a completely specified solar cell (and module) production process sequence. This sequence must be capable of a high degree of automation and control. A detailed economic analysis is a major part of the program to ensure that the most cost-effective approach is taken.

3.0 TECHNICAL DISCUSSION

3.1 WAX MASKING TECHNOLOGY

Masking of portions of a solar cell substrate against chemical attack can be achieved through application of a wax. Earlier in this contract effort, methods of applying a wax from a wax-solvent solution were investigated and found satisfactory. Further, a wax which met the requirements for this process sequence was identified, Multiwax 195M.

The utilization of solvents to dissolve the wax for application to the substrates has some drawbacks. The most efficient solvents have undesirable environmental impacts. The wax-solvent solutions require preparation, adding slightly of the cost of the process and ultimately of the solar cell. Further, the solvents are an expense themselves; while partially recoverable, some solvents are consumed in the process.

Efforts have, thus, been made to investigate alternatives to applying wax from a wax-solvent solution. A melted wax application appears to be a more satisfactory process.

3.1.1 MELTED WAX MASKING

The wax selected for use in solvent-wax masking solutions, Multiwax 195M melts at 90°C, forming a low viscosity liquid which is easily handled. The availability of inexpensive equipment to attain and maintain the melting temperature of this wax suggested use of this wax for application in melted form.

3.1.2 ADVANTAGES AND DISADVANTAGES OF MELTED WAX APPLICATION

The first apparent advantage to the melted wax method is that of convenience. The wax, as delivered, is a hard solid. Preparation of the solvent-wax solutions involves the crushing of the wax and mixing with a suitable solvent. The duration

of the mixing process is relatively long--several hours-- and is required to achieve a saturated solution of wax in the solvent (necessary for process control). With a melted wax system, the masking agent is in usable form as received from the manufacturer, with the only preparation being that of melting. In addition to the convenience of ready use, the time-consuming solution preparation step is eliminated.

The cost savings effected by reduction of preparation time are further increased by elimination of the required solvents. All of the solvents found to be effective in forming wax solutions are derived from petroleum and are likely to suffer from both decreased supply and increased price in the future. Use of wax solutions also demands evaporation of solvent from the wax coating after application. Although recovery of vaporized solvent is possible, the process is neither cost-free nor totally effective. Recovery also involves reclamation of the solvent in reuseable form -- a complication to the process.

With any solvent-based process, the consequences of personnel exposure must be considered. All of the acceptable solvents are volatile, odiferous, and toxic. Some are flammable. Worker exposure to solvent fumes at some point in processing seems inevitable. Even though proper ventilation can reduce exposure, and reclamation can reduce the amount of lost solvent, it is inevitable that some solvent will be discharged to the atmosphere -- an ecologically undesirable situation.

Aside from eliminating the cost and environmental problems of solvent use, melted wax offers improvement of masking performance. Direct application of melted wax results in a thicker, denser wax coating than can be readily achieved through the use of wax solutions. Although coatings produced by solvent solutions have been found satisfactory in limited laboratory production,

the large-scale use of the process implies the need for more stringent process controls, especially for textured surfaces. The thick, dense coating produced by direct application of liquid wax ensures improved masking performance.

Application of a melted wax eliminates the requirement of drying the layer applied from a wax-solvent system. This elimination of solvent removal from the mask layer also affords added reliability, through a decrease in masking defects seen in any solid-solvent system (including photoresist materials). In efforts to decrease the time necessary for the solvent drive-out required by the use of solvent-wax solutions, higher temperatures and vacuum drying techniques were researched. It has been found that certain conditions of temperature and vacuum, either alone or in combination, caused the eruption of solvent vapor bubbles within the wax layer, resulting in porosity and pinhole defects through the masking layer. Use of pure wax, from which no solvents are removed, eliminates this problem.

The use of liquid wax does present some problems. After application to a surface, the wax tends to shrink upon cooling, tending to withdraw slightly from the edges of the coated surface. The application of a thicker wax coating also implies increased difficulty in removing the coating after processing. These disadvantages have already been largely overcome, as will be discussed later.

3.1.3 APPLICATION OF MELTED WAX

The melted wax may be applied by any of the methods useful for solvent-wax solutions. All silicon-based surfaces encountered in cell manufacture are easily wet by wax, e.g., bare silicon, silicon dioxide, silicon nitride, and various deposited and applied masking and dopant glasses.

Direct printing of melted wax on cell surfaces has proven successful, as has spray application. In both cases, heating of the entire substrate has been found advantageous.

A straightforward method of application to round substrates is by spinning. A standard photoresist spinner is used in this method. The cell is placed on a vacuum chuck and a small quantity of liquid wax is applied. Rapid rotation of the cell then produces a smooth, level wax coating. The availability of automatic photoresist equipment makes this technique immediately applicable with present equipment, although to produce optimum results, minor modifications are desirable. Automatic dispensers for photoresist need only be heated, for example, by wrapping with heating tape to allow delivery of melted wax. Heating of the cell surface has been found to produce more consistent results than the use of unheated surfaces. This has been done with hot air, but may be accomplished in numerous ways. Cooling of the cell to harden the applied coating may be necessary and can be conveniently arranged by use of a cool air stream directed at the cells as they leave the spinner chuck. One additional modification completes the system. As the cell is spun to level the wax, excess wax is thrown from the wafer, collecting and solidifying in the spinner shield. Heating of this shield allows the wax to flow back into the wax supply receptacle for reuse.

For irregularly shaped cells which cannot be spun, such as ribbon substrates, alternate application techniques have been investigated. In its simplest form, application is effected by covering a glass or ceramic plate with a film of melted wax and manually pressing the cell surface against the plate. This method produces a continuous film without wetting the back of the cell. Although the wax layer produced in this way is somewhat more uneven than that obtained by spinning, the unevenness does not hinder masking performance. Refinement of the method should allow automation of the process. Use of a

rotating porcelain cylinder dipping into a pool of melted wax has proven practical. The rotating cylinder, easily wet by wax, acquires a thin, continuous film which is transferred to the cell surface upon contact.

As mentioned previously, a problem encountered with the use of melted wax is that of shrinkage. This can be alleviated by the use of appropriate fillers in the wax. The fillers used are finely powdered substances that produce a suspension of solid particles in the wax, promoting dimensional stability. The successful filler material should be insoluble in water and the commonly used acid etchants, be soft enough to avoid abrading the cell surface, and be readily available at low cost. The common mineral, fluorite (calcium fluoride) fulfills each of these requirements, and has been used with success in our experiments.

3.1.4 REMOVAL OF WAX

Removal of the wax coating can be accomplished, as with the wax-solvent system, by dissolution with solvents. The use of thicker wax coatings produced by melted wax, and the incorporation of filler materials into the wax, does present problems, however. For example, the use of greater amounts of solvent than is customary with the thin solvent-wax solution films will be required to effectively remove melted wax films. Any filler material in the wax will simply settle to the bottom of the solvent container. The solvent and wax can be separated from each other by distillation, during which the filler will remain with the wax, making reformulation unnecessary. The use of solvents, nevertheless, is undesirable for the reasons given earlier.

An alternate removal process which avoids solvent use entirely has been investigated. It has been found that wax can be removed from cell surfaces by immersion of the cells in hot water, during which the wax melts and floats to

the surface in an easily removed layer. The process is incomplete when pure water at its boiling point is used; about 70% of the applied wax is removed. Addition of dense salts such as ammonium sulfate to the water raises the boiling temperature and density of the water so that more complete removal results.

This technique is also capable of automation. Currently available equipment exists that cleans silicon wafers by directing a high pressure stream of water onto the wafer surface. Simple modification will result in a device that produces a stream of hot water that will effectively remove the wax from the cell surface. The water-wax mixture that results can be directed into a settling tank where the immiscibility of the wax and water (and their density differences) will cause separation of the wax into a floating layer upon the water. If the tank is heated, the wax can be drawn off as a liquid for use in masking incoming cells. The water solution can also be reused, resulting in essentially no waste of any materials. In preliminary tests of this technique, separation of filler material from the wax has been shown to be small.

The traces of wax that remain on a cell surface after water clean process can be removed by an oxygen plasma cleaning, which would normally be utilized prior to either silicon nitride deposition or ion implantation, the next steps in the process sequence.

The objective of this study is to perform a detailed systematic investigation of solar cell characteristics influenced by implant conditions (voltage, beam current, beam traversals, dose), impurity species (P, As, B), cell type (n-on-p, p-on-n), and anneal cycle.

Experiments have been performed with phosphorous (P^{31}), boron (B^{11}), and arsenic (As^{75}) implants. Implant energies have ranged from 35 KeV to 195 KeV and ion doses have been varied from 10^{14} cm^{-2} to $3 \times 10^{16} \text{ cm}^{-2}$ at beam currents up to 2 mA for phosphorous and arsenic and up to 1 mA for boron. In order to make direct comparisons between different implants, activation anneals have all been performed utilizing a 30 minute cycle at 900°C . This annealing cycle should be sufficient to totally activate the implanted species and, experimentally, it has proven to be very effective. Using this anneal, variations of implant voltage and dose that were incorporated in the study have resulted in junction sheet resistance ranges of 8 to $560 \Omega/\square$ for phosphorous, 30 to $670 \Omega/\square$ for boron, and 35 to $820 \Omega/\square$ for arsenic. Many of these sheet resistance data were presented in Technical Quarterly Report No. 2, showing that the empirical behavior of sheet resistance versus implant dose and energy at high dose rates are in agreement with values published in the technical literature, much of which work was done at low dose rates.

Effects of ion implant parameters on solar cell photoresponse are being studied experimentally. Photoresponse behavior of test solar cells can be observed in Figures 1 through 10. These figures present photogeneration current and open circuit voltage data as functions of ion dose and implant energy. Figures 1 through 5 give data for P^{31} implants, Figures 6 through 8 give data for B^{11} implants, and Figures 9 and 10 give data for As^{75} implants. Arsenic and phosphorous implants were performed into bare, polished, boron-doped, 3 inch

FIGURE 1

PHOTORESPONSE DATA: 35 KeV PHOSPHOROUS

IMPLANT AT 7 DEGREE ANGLE

FIGURE 2

PHOTORESPONSE DATA: 105 KeV PHOSPHOROUS

IMPLANT AT 7 DEGREE ANGLE

FIGURE 3

PHOTORESPONSE DATA: 105 KeV PHOSPHOROUS

IMPLANT AT 5.5 DEGREE ANGLE

FIGURE 4

PHOTORESPONSE DATA: 175 KeV PHOSPHOROUS

IMPLANT AT 5.5 DEGREE ANGLE

FIGURE 5
PHOTORESPONSE DATA: 195 KeV PHOSPHOROUS
IMPLANT AT 5.5 DEGREE ANGLE

FIGURE 6

PHOTORESPONSE DATA: 35 KeV BORON

IMPLANT AT 5.5 DEGREE ANGLE

FIGURE 7

PHOTORESPONSE DATA: 100 KeV BORON

IMPLANT AT 5.5 DEGREE ANGLE

FIGURE 8

PHOTORESPONSE DATA: 195 KeV BORON

IMPLANT AT 5.5 DEGREE ANGLE

FIGURE 9

PHOTORESPONSE DATA: 105 KeV ARSENIC

IMPLANT AT 7 DEGREE ANGLE

FIGURE 10
PHOTORESPONSE DATA: 195 KeV ARSENIC
IMPLANT AT 7 DEGREE ANGLE

diameter test wafers with substrate resistivities between 0.6 and 1.4 Ω -cm. Boron implants were performed into bare, polished, phosphorous doped, 3 inch diameter test wafers with substrate resistivities between 5 and 7 Ω -cm. Subsequent to the implants, the cells were annealed at 900°C for 30 minutes in an atmosphere of nitrogen with 2% oxygen. The small percentage of oxygen was used in the nitrogen ambient to prevent the possibility of nitrogen damage to the silicon surface.

After the anneal, the bare test cells were electrically characterized. Open circuit voltage was measured under a quartz-halogen lamp at one sun intensity by using a high impedance digital voltmeter (Keithley). Under the same lamp, photogeneration current was measured by observing the reverse biased diode characteristics with a curve-tracer (Tektronix). The generation current behavior can be observed in the third quadrant, even though, with no metal contacts yet applied, the cell has appreciable internal resistance. The current and voltage thus measured are indicative of solar cell performance.

Several conclusions can be drawn from the data of Figures 1 - 10. First, overall performance of the test solar cells is very reasonable, considering that no antireflective coating or texture etching was used. Of course, larger current and voltage values will be obtained when an anti-reflection coating and metal contacts are applied. (Photocurrent should be about 50% higher, and V_{OC} should be increased by about 35 mV; if this proves to be the case in completed cells, then both n-on-p and p-on-n solar cells made by high beam current ion implantation will be competitive with the very best of today's diffused product.)

A second conclusion is that the open circuit voltage behaves as expected. Higher ion doses and lower sheet resistances in general tend to yield higher

V_{OC} values. This is likely to be due to a simple "emitter efficiency" effect. Heavier doping in the emitter reduces the junction reverse saturation current and increases V_{OC} .

A third conclusion is that generation current (I_{gen}) tends to decrease with increased ion dose (and the consequently decreased sheet resistance). In some cases, such as the arsenic data of Figure 9, this effect is quite pronounced. There are several possible reasons for this. Higher dose and lower sheet resistance imply a deeper junction after annealing. Both the implanted impurity profile and impurity diffusion effects are responsible for junction depth increase. Deeper junctions can yield lower photogeneration current because of lost short wavelength response.

Moreover, too large an ion dose means that peak impurity concentration may exceed solid solubility. If C_p is the peak concentration in cm^{-3} of the implanted impurity profile, and ΔR_p is the range parameter of the implant (in cm), then the ion dose (N/A) in cm^{-2} is given as

$$N/A = \sqrt{2\pi} (\Delta R_p) C_p.$$

The solid solubility of arsenic in silicon at 900°C is approximately 10^{21} cm^{-3} .

If this is to be the peak concentration, then a dose of $N/A = 5.5 \times 10^{15} \text{ cm}^{-2}$ is required at an implant energy of 105 KeV. Hence, for doses greater than $5.5 \times 10^{15} \text{ cm}^{-2}$ there is a risk of exceeding solid solubility of arsenic.

The comparable doses for boron and phosphorous at 105 KeV and 900°C are $4.7 \times 10^{15} \text{ cm}^{-2}$ and $7.2 \times 10^{15} \text{ cm}^{-2}$, respectively. If solid solubility is exceeded, permanent lattice damage may result, electrically inactive dopant will be present, minority carrier lifetime will be degraded, and an appreciable so-called "dead-layer" may be formed which will result in reduced I_{gen} .

The empirical data trends of Figures 1 - 10 indicate that a trade-off is to be made between V_{OC} and I_{gen} . As V_{OC} is increased, I_{gen} may be reduced.

This fact, along with solid solubility considerations, leads to the conclusion that the range of interest for further work should be narrowed to doses between $3 \times 10^{14} \text{ cm}^{-2}$ and $3 \times 10^{15} \text{ cm}^{-2}$ for smooth-surfaced solar cells. This would result in a range of sheet resistances between 30 and 200 $\Omega/\square$ for phosphorous, between 60 and 250 $\Omega/\square$ for boron, and between 50 and 250 $\Omega/\square$ for arsenic. These values are in agreement with reasonable diffused solar cell fabrication parameters as well.

The data discussed above are for bare, smooth-surface silicon. If a textured surface is considered, then doses greater by a factor of 1.73 will be needed to supply the same dopant per unit area, since the textured surface area is effectively 1.73 times greater than a smooth surface. Since the ion beam must enter the $\langle 111 \rangle$ textured surface facet at an appreciable angle, the resulting junction will be shallower than for a smooth $\langle 100 \rangle$ test wafer. These geometrical effects of a textured surface have been widely discussed. In any case, a higher implant energy must be used to obtain the same junction depth on a textured surface as that of a polished surface. Furthermore, if the implant is to be performed through an antireflective dielectric coating on the silicon surface, then additional energy will be needed to penetrate the dielectric layer.

Another subject for further work is the activation anneal cycle; an optimum thermal anneal for the process being developed is yet to be determined. Initial experiments have been performed. A group of 20 wafers (0.6 to 1.4 $\Omega\text{-cm}$, $\langle 100 \rangle$, p-type, bare, polished on one side) was fabricated into test solar cells by implanting the polished front with P^{31} for front junction formation at a dose of $3 \times 10^{15} \text{ cm}^{-2}$ at 35 KeV and implanting the back with B^{11} at a dose of $1 \times 10^{16} \text{ cm}^{-2}$ at 35 KeV for BSF and contact enhancement. After implant the lot was split in two. One half was annealed at 900°C for 30 minutes in nitrogen with 2% oxygen. The other half was given a 2 hour soak at 550°C

before ramping up (for 20 minutes) to 900°C and then being held at 900°C for 30 minutes. This was also done in nitrogen and oxygen. After the anneal, all cells were coated with a silicon nitride antireflective coating using a low pressure CVD furnace. The polished front sides were then patterned with a metal contact grid pattern and the cell backs were stripped of dielectric. At this point the cells were electrically tested to determine solar cell performance.

Open circuit voltage, V_{OC} , and photogeneration current, I_{gen} , were measured for each half group of test cells. No significant difference was found between the two groups. The first group (900°C only) had an average V_{OC} of 591 mV (with 6 mV standard deviation) and an average I_{gen} of 1483 mA (with 44 mA standard deviation). The second group (550°C and then 900°C) had an average V_{OC} 590 mV (with 3 mV standard deviation) and an average I_{gen} of 1477 mA (with 29 mA standard deviation).

Additional thermal anneal studies are underway. Temperatures, and temperature cycles, in the range between 400°C and 1000°C are being considered.

The palladium-nickel-solder metallization system has been detailed in Quarterly Technical Report No. 2. Advanced development of this metallization technique has proceeded under JPL Contract No. 954689, "Metallization of Large Silicon Wafers". The system is comprised of three layers. Palladium, through the formation of palladium silicide at elevated temperatures, makes ohmic contact to the silicon surface. Nickel, plated on top of the palladium silicide layer, forms a solderable interface. Lead-tin solder on the nickel provides a high conductivity at low cost and allows a convenient means for interconnection of cells.

In the development of this system, emphasis has been placed on metal adhesion and the ability of the metal system to withstand high temperature solder reflow operations during cell interconnection. The only acceptable mode of contact adhesion failure is fracture of the silicon substrate beneath the contact.

To apply this metallization, three chemical plating baths are employed. Palladium is deposited first with an immersion solution and then in an electroless bath; nickel is subsequently deposited with an electroless solution. Advances in the immersion palladium bath chemistry have resulted in a much improved immersion palladium deposition.

Until recently, the state-of-the-art immersion palladium solutions produced palladium deposits as reported in Quarterly Technical Report No. 1 for JPL Contract No. 954689; scanning Electron Microscope (SEM) photographs of a typical deposit of this type on a silicon surface are shown in Figure 1:1 for an immersion palladium solution prepared with water, fluoboric acid, hydrochloric acid, and palladium chloride. The formation of discontinuous granular

(a) 75 sec. immersion

(b) 150 sec. immersion

FIGURE 11: IMMERSION PALLADIUM PLATING WITH FLUOBORIC ACID SOLUTION

clumps of palladium, and perhaps palladium salts^{*}, is typical of this solution (and many others). Such a palladium deposit is not very adherent until it has been heat treated, presumably forming palladium silicide (Pd_2Si). Even then, much non-adherent material can be removed upon mechanical or hydraulic scrubbing. This loose material is probably palladium and palladium salts from the tops of the granular clumps. Furthermore, during electroless palladium deposition, the initiation of plating will occur preferentially at the clumps, and may not form intimately on the silicon surface area between the clumps. This is obviously not the most desirable plated film topology, and could result in a non-uniform palladium silicide layer formation even after electroless plating. Consequently, reduced adhesive strength was sometimes obtained between the silicon surface and the metal contact layers.

Figure 12 shows SEM photographs of a palladium layer deposited with a newly developed immersion palladium solution. In this case, a continuous layer of palladium^{**} has been formed on the silicon surface. Such a layer should

^{*} During sintering of the immersion palladium layer, a metallic-looking deposit gradually built up on the quartz furnace tube. This deposit was analyzed as silicon. The most satisfactory explanation for how it got there involves halogen (chlorine) transport of silicon from the heated silicon wafers to the cooler furnace wall. A possible conclusion is that at least part of the deposited film was palladium chloride.

^{**} Deposits of silicon do not appear on the quartz furnace tube when immersion palladium layers deposited by the new chemistry are sintered. This suggests that the film contains little or no chlorine (e.g. no palladium chloride).

(a) N+ front textured surface showing large Pd grains on top of continuous, fine-grained Pd layer.

(b) P+ back smooth surface showing continuous, fine-grained Pd layer.

FIGURE 12: IMMERSION PALLADIUM PLATING FROM NEWLY DEVELOPED CHEMISTRY.

be capable of satisfying the requirements for formation of a very adherent layer of Pd_2Si .

The new immersion palladium solution eliminates the fluoboric acid (HBF_4) in favor of a low concentration of ammonium fluoride (NH_4F). The other constituents are water, palladium chloride (PdCl_2), and hydrochloric acid (HCl). This solution plates a thin, metallic immersion layer with little or no loose palladium. The immersion layer will withstand a vigorous mechanical scrub and will consistently initiate adherent electroless plating.

The new plating chemistry is being incorporated into the overall process sequence being developed under this contract. An improvement in yield of highly adherent metal, and thus in the long term reliability of solar cells, is expected. Since the immersion layer is now completely continuous, it is possible that the electroless layer can be thinned, reducing the cost of this metallization (See Technical Progress Report Number 2) to a value which is easily consistent with processing costs budgeted for a less than 50¢/watt solar cell module.

The utilization of a textured front surface on a silicon solar cell has been shown to increase solar cell efficiency. This increase is a direct result of less reflection of light from the cell surface. The textured surface is comprised of a continuous field of pyramids; the base of each pyramid is a (100) plane, while the faces of the pyramids are (111) planes. Light normally incident to the plane of the substrate, and the plane of the pyramid bases, is either refracted into the silicon or is reflected directly onto an adjacent pyramid face. Reflected light, thus, is given a second incidence on the silicon surface. The geometries and effects of such textured surfaces have been widely discussed.

The formation of pyramidally textured silicon surfaces is achieved by means of any one of several anisotropic etchants. These may be formulated from several compounds known to etch silicon, such as various ammoniacal compounds and amines, hydrazine, or alkali hydroxides. These compounds display the ability to dissolve crystalline silicon at different rates depending on the direction of dissolution through the crystal. By proper choice of etchant, directional preference, and crystal orientation, an etchant that produces the desired pyramidal surface can be specified.

The choice of etchant is limited by considerations in addition to etching efficiency. The amines and ammoniacal compounds pose problems of toxicity and availability, as well as those of odor and volatility. The extreme toxic nature of hydrazine is well documented. Hydrazine also possesses chemical reactivity that precludes its use; it reacts explosively with some of the commonly used cell processing reagents, raising problems associated with storage and contamination. The preferred etchants are those based on the plentiful and inexpensive alkali hydroxides. These compounds are easily stored and

present less of a health hazard than many of the acids presently used in cell manufacture. In addition, the alkali hydroxides have been thoroughly researched as to chemical and biological behavior and seem least likely to be the objects of government-regulated use in the future.

The etch now in use consists of an aqueous solution of any of the available alkali hydroxides along with various abundant commercially available organic compounds, which moderate the etching power of the hydroxide and increase the directional nature of its attack on silicon. In order to increase the speed of dissolution, the etchant composition is customarily used at elevated temperatures of from 50°C to 100°C. At these temperatures, the etchant produces the desired fully textured surface in 30 to 65 minutes.

From optical considerations, the size and distribution of the pyramidal peaks is unimportant. Light is reflected and refracted from large peaks, small peaks, or a mixture of large and small peaks in an identical manner. In terms of processing convenience, however, control of pyramid height is desirable. Large pyramids can cause problems in the masking and metallization processes used. Further, isolated large peaks, surrounded by a field of smaller pyramids present small, high areas that are very susceptible to damage from handling; depending on where they are and when in the process sequence the damage occurs, the effects can be appreciable on solar cell performance.

Several techniques have been discussed in the industry for controlling peak size. These, in general, require special treatment of the silicon surface or require special mechanical constraints during etching to initiate and maintain the desired peak size. We have found recently that peak size can be controlled solely by varying the composition and temperature of the texture-etch solution, eliminating the need for any special silicon treatment or external mechanical fixtures that may be required by other texture etching conditions.

The etchant composition used is easily prepared and has been characterized as to the effects of temperature and composition. As an advantage, spent etchant can be replenished -- apparently for an appreciable length of time -- by the addition of controlled amounts of fresh hydroxide, thus assuring minimal waste of consumed material.

This improved control of peak size by texture etching is being incorporated into the process sequence under development. The results are expected to be improved control and process yield, concomitant with low (and perhaps reduced) cost.

3.5 VERIFICATION OF PERFORMANCE

Verification (control) points have been defined for each process step and for the process sequence. In general, the process sequence can only be considered successful if a high yield is obtained at the module level.

Testing of cells going into the modules and testing of completed modules, thus, are two key control points. Other key control points are utilized for evaluation of cells in-process, and must be related to final cell performance.

3.5.1 VERIFICATION OF PLASMA ETCHING

3.5.1.1 PLASMA SILICON ETCHING

Verification of satisfactory process control for plasma silicon etching is indirect and requires a time-lag between process performance and process verification. Following etching, completeness of damage removal can be verified by etch-pit techniques, or by analytical techniques such as X-ray topography. Etch-pit counting is limited to observing major amounts of residual damage; since it also etches the silicon, it can remove small amounts of residual damage. The process controls should, ideally, ensure that a minimum amount of undamaged silicon is removed while still ensuring complete removal of the damaged layer. Accurate knowledge and control of the amount of damage created by a particular sawing technique is critical to economical operation of the sawing process. For example, if insufficient material is removed, final cell performance will be degraded. On the other hand, if too much material is removed, the process expends more time than necessary, consumes more materials, etc. Routine analysis of the depth of saw damage is, thus, a necessary control point.

3.5.1.2 PLASMA SILICON NITRIDE ETCHING

Process verification of silicon nitride patterning is accomplished primarily by visual inspection, utilizing both optical microscopy and scanning electron microscopy (SEM). In addition to inspection for completeness of removal, inspection must also be made for silicon etching and for nitride removal in undesired areas. The latter is, of course, dependent upon the quality of the masking. The other key parameter is pattern line width, which is also verified by visual inspection.

3.5.2 VERIFICATION OF WAX MASKING

Verification of the quality of the wax masking again relies upon visual criteria. Control inspection may be readily performed both after application and after etching. Both are capable of being done in-line by automatic equipment.

3.5.3 ION IMPLANTATION PERFORMANCE

In addition to in-process monitoring of the implant dose and voltage, control of ion implantation parameters relies upon measurement of substrates after activation anneal. The most rapid turn-around of information can be achieved through sheet resistance and photoresponse measurements, either on a continuous basis or through selective sampling.

3.5.4 PROCESS SEQUENCE VERIFICATION

Proof of total cell process sequence performance can only be measured meaningfully through electrical testing of completed solar cells, followed by the successful interconnection and encapsulation of the cells.

Here, visual inspection is also useful in identifying potential reliability problems.

Control points should be incorporated into the process sequence, at least on a sampling basis, sufficient to guarantee that rapid, unambiguous identification of a processing problem can be made. The unambiguous feature of such trouble-shooting is of key importance. Sufficient data should be compiled during processing to make an unambiguous analysis. For example, it is necessary to distinguish whether a cell having a poor cell fill factor is the result of a defective p-n junction, contamination by a lifetime killer, high sheet resistance of the upper P-N junction region, metal ingression to the vicinity of the p-n junction, or metallization of exposed areas of the p-n junction as a result of etched or broken textured peaks.

4.0 CONCLUSIONS

Several conclusions can be drawn from the work reported during this period.

The application of melted wax as a masking material appears to be practical and effective, and to offer significant potential cost and environmental advantages over the use of wax-solvent solutions.

Photoresponse data from test wafers indicate that implant doses for optimum solar cell performance fall within the approximate range of $3 \times 10^{14} \text{ cm}^{-2}$ to $3 \times 10^{15} \text{ cm}^{-2}$ for phosphorous, arsenic, and boron dopant implants. Further, these data indicate, after making adjustments for the effects of front surface texturing and antireflection coating, that cells made with implantation of any of these dopants (for both n-on-p and p-on-n cells) would be competitive with the best diffused cells now commercially available.

Recent advances in immersion palladium plating technology show promise of improved control and greater reliability over earlier chemical formulations; in addition, the realization of very low cost is possible.

Control of textured surface peak size can be obtained by simple bath parameters (composition and temperature); there is no need to employ more complicated mechanical techniques to obtain small, uniform peaks.

5.0 RECOMMENDATIONS

No specific recommendations can be made at this time.

6.0 CURRENT PROBLEMS

There are no current problems which remain unresolved.

7.0 WORK PLAN STATUS

The work plan is on schedule with the exception of the experimental portion of the ion implantation studies which, because of its interaction with other planned work, has resulted in the expenditure of fewer hours than planned. This is being rectified, and should be caught up by the end of the program.

8.0 LIST OF ACTION ITEMS

No items requiring unusual action have come to light during this report period.

9.0 MILESTONES

Status of the program is shown in the Milestone Chart.

	1	2	3	4	5	6	7	8	9	10	11	12	13
	O	N	D	J	F	M	A	M	J	J	A	S	O
<u>STUDY I</u>													
<u>TECHNOLOGY ADVANCEMENT</u>													
A. Wax Resist Technology Advancement													
B. Plasma Silicon Etching													
C. Plasma Silicon Nitride Etching													
D. Ion Implantation Technology													
E. Incorporation of Metallization Advancements from Parallel Study													
F. Process Sequence Enhancement													
<u>STUDY II</u>													
<u>VERIFICATION OF PERFORMANCE</u>													
A. Establish Verification Points													
B. Correlation of Verification Measurements													
C. Solar Cell and Module Fabrication													
D. Verification of Process Sequence Performance													
<u>STUDY III</u>													
<u>ECONOMIC ANALYSIS</u>													

MILESTONE CHART

MILESTONE CHART (continued)