Polycrystalline Thin Film Cadmium Telluride Solar Cells Fabricated by Electrodeposition

Annual Subcontract Report
20 March 1993 – 19 March 1994

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A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under contract No. DE-AC02-83CH10093

Prepared under Subcontract No. XG-211036-4

July 1994

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Executive Summary

This report contains results from the second year of a three-year program at Colorado School of Mines entitled "Polycrystalline Thin Film Cadmium Telluride Solar Cells Fabricated by Electrodeposition."

Section 6 describes the principal results of our work. The portion on transparent conducting oxides was primarily carried out by CSM students at NREL and is described in three publications listed in Appendix C. The high-quality ZnO produced in the work was incorporated in a copper indium diselenide cell which exhibited a world record efficiency of 16.4%.

Much of our effort was devoted to the improvement of cadmium sulfide films deposited by chemical bath deposition methods and annealed with or without a cadmium chloride treatment. Significant improvements in surface morphology were achieved.

Progress was also made in the electrochemical deposition of cadmium telluride during the reporting period. High quality films yielding CdS/CdTe/Au cells of greater than 10% efficiency are now being produced on a regular basis. Further work to improve film quality and to introduce appropriate doping is underway.

We have also explored the use of zinc telluride back contacts to form an n-i-p cell structure as previously used by Ametek. As discussed in Section 6d, we have not yet achieved any significant improvement in the cell series resistance by this approach.

We have initiated small-angle x-ray scattering studies (SAXS) to characterize crystal structures, residual stresses, and microstructures of both CdTe and CdS. Large SAXS signals have been observed in CdS, most likely due to scattering from grain boundaries. The signals observed to date from CdTe are much weaker indicating a more homogenous microstructure.

Finally, as described in Section 6f, we have begun to use the ADEPT modeling program, developed at Purdue University, to guide our understanding of the CdS/CdTe cell physics and the improvements which will most likely lead to significantly enhanced efficiencies. A number of representative modeling results are included in this section of the report.

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4. Background

As described in the Solicitation (LOI NO. RM-1-11036) which led to this contract, polycrystalline thin-film CdTe photovoltaics are considered among "the leading thin-film materials in terms of efficiency and long-term reliability". Prominent companies in the development of this technology have included Photon Energy and Ametek in the U.S., Matsushita in Japan, and British Petroleum in the U.K. In 1990, Ametek made a decision to abandon further development of CdTe photovoltaics and to donate all related assets (patents, laboratory know-how, and equipment) to the Colorado School of Mines Foundation. The Ametek facility was re-established at the Physics Department of the Colorado School of Mines and formed the basis, along with the laboratory know-how, for the current work.

The Ametek research, supported to a large extent by NREL (SERI), led to small cells of more than 11% efficiency. Moreover, the unique, low cost electrodeposition methods developed by Ametek for this material have attracted a great deal of interest. At the same time, additional basic research is still needed to improve upon the efficiencies and performance levels achieved to date. Among the significant issues are interface carrier recombination and top-layer photon absorption which presently limit the short-circuit current, junction recombination which limits the open-circuit voltage, and series-resistance losses which suppress the fill-factor. Cascade geometries based on CdTe-containing ternaries are also an area of interest. With respect to large-scale processing and manufacture, some of the pressing issues are the design of suitable equipment, efficient methods for making interconnections on large arrays, and suitable packaging.

The intent of the CSM contract is to build upon the Ametek experience and expertise regarding polycrystalline, thin-film, CdTe n-i-p solar cells to improve certain processing steps and the potential for economic, large-scale production. Improved efficiencies are also a major goal. Significant increases should be possible through interface and grain-boundary passivation, antireflection coatings, and other improvements. High-quality film growth techniques, materials analysis, device characterization, and device fabrication are all of particular interest in our work.

The Ametek n-i-p structure contains at least 3 different semiconducting layers (n-CdS, i-CdTe, and p-ZnTe), comprised of at least 4 different elements, as well as front and back ohmic contacts. The preferred embodiment involves a common anion at the p-i junction and a common cation at the i-n junction[1]. Intermediate layers are possible, which might be introduced to passivate defects or act as buffer layers since interdiffusion of materials at the boundaries can be problematic.

A variety of deposition procedures has previously been used for the respective layers. Although a spray pyrolysis technique for the CdS n-layer was developed and patented by Ametek, their highest efficiency cell was achieved with a dip coat method for this part of the structure. Their approach involved the use of CdCl_2 , NH_4OH , NH_4Cl and thiourea at about 100°C.

An important part of the Ametek technology is the CdTe i-layer electrodeposition process which leads to insulating, compensated CdTe, an essential feature of the overall structure. There

are trap states at one of the CdTe band edges which have been identified, in bulk samples, by DLTS and photoluminescence [2]. Their origin is thought to be Cd vacancies. However, other possibilities include grain boundaries and the internal surfaces of microvoids.

The Ametek technique for the fabrication of the ZnTe p-layer was vacuum thermal deposition. As part of the development of a more practical overall process, our project includes the investigation of non-vacuum methods for this step. To complete the process, non-vacuum methods for metallization would also be desirable.

5. Phase Two Tasks and Milestones

The Phase-Two film-growth activities were intended to involve all three layers of the n-i-p cell structure. For the CdS layer, dip coating was identified in Phase-One to be a viable technique. The major task regarding this layer in Phase-Two, then, was to optimize process conditions for improved performance. For the CdTe layer, we continue to use an electrodeposition process, but studies are being designed to improve the final product by better process control. The Phase-Two goal of this aspect of the project was to establish whether the i-layer could be improved with respect to grain size and/or grain boundary passivation by an improved electrochemical approach. With respect to the ZnTe layer, an effort was to be made to discover an alternative to vacuum deposition, such as electroplating. For all three layers, we were to explore the use of rapid thermal processing as an alternative to conventional annealing.

The second task, device fabrication, was to continue in Phase-Two. The goal was to establish a CSM capability for the fabrication of small-scale cells superior to those produced earlier at Ametek. We were also to develop the preliminary design of a large-scale process suitable for the production of CdTe modules.

The remaining tasks were materials analysis and device characterization including techniques to characterize the electrical potential distribution near grain boundaries and interfaces.

A list of specific Phase-Two tasks is given on the following page.

Phase Two Tasks

Task five (high quality film growth techniques)

1. Optimize the procedures of preference for the fabrication of TCOs, CdS, CdTe, ZnTe, and contact layers, including studies of the effects of photoenhancement on the electrochemical deposition of CdTe with respect to grain size, grain boundary passivation, and other characteristics of the product.
2. Conduct experiments with rapid thermal processing.
3. Combine the selected processes for individual layers into a single procedure for the fabrication of entire cells.
4. Determine the most effective processing steps for the mitigation of electronic traps.
5. Publish results in open literature.

Task six (device fabrication)

1. Demonstrate a 1 cm² cell which has been made using the preferred procedures.
2. Demonstrate a 12%, 1 cm² cell.
3. Develop a manufacturable module which incorporates these cells, including appropriate encapsulation.
4. Develop the preliminary design of a large-scale process suitable for the production of CdTe modules.

Task seven (material analysis and device characterization)

1. Demonstrate the use of STM or other techniques to characterize the electrical potential distribution near grain boundaries and interfaces as it relates to the depression of V_{oc} .

6. Accomplishments

a) Transparent Conducting Oxide Studies

Studies and the development of improved TCO coatings were continued at NREL by Mr. Yi Qu and Mr. Andrew Johnson under support of this contract.

Both ZnO and Al-doped ZnO (ZnO:Al) films were deposited and employed in the fabrication of CIS and CIGS solar cells. The ZnO films were deposited using a pure ZnO target at room temperature with a thickness of $\sim 500\text{\AA}$. The ZnO:Al films were deposited to a thickness of $\sim 3000\text{\AA}$ using an Al-doped target at a temperature of 100°C .

Structural, electrical and optical measurements were performed on films deposited on Corning 7059 glass substrates. The XRD results show that the films have a highly preferred orientation with the c-axis perpendicular to the substrate. The electrical resistivities are $\sim 1\text{-}10\ \Omega\text{-cm}$ (ZnO) and $2\text{-}4 \times 10^{-3}\ \Omega\text{-cm}$ (ZnO:Al), respectively. The optical transmission is 85-90% in the visible range.

A CIGS solar cell with a structure of glass/Mo/CIGS/CdS/ZnO:Al/Ni/Al/MgF₂ fabricated at NREL achieved a record efficiency of 15.9% with the employment of the high quality ZnO and ZnO:Al films during the period of this report. The current record efficiency is 16.4%.

Quantum efficiency measurements on this cell show that even though high efficiency has been achieved, some increase in efficiency is still possible by reducing absorption in the window layers. Because most of the absorption in the blue and visible range is caused by defect levels in the band gap, and because absorption in the near-infrared (NIR) is caused by free carriers, therefore, improvement of the structural properties of the film will be important. The carrier concentration can be reduced with improvement of carrier mobility without worsening the electrical conductivity. This leads to a reduced free carrier absorption in the NIR range.

Three publications describing this work are listed in the Appendix.

b) CdS Films

Cadmium sulfide films were deposited by a chemical bath deposition (CBD) method. Soda-lime glass substrates coated with SnO_2 (Nippon Sheet Glass) were used as substrates. The typical sample dimension was 2"x3" and the SnO_2 layer had a sheet resistance around $10 \Omega/\square$. The deposition procedure was reported elsewhere [3] and is similar to those described by other authors [4]. The concentrations of chemicals used in this work are listed in Table 6.b.1.

Figure 6.b.1 shows a relationship between the thickness and the deposition time obtained for a particular combination of chemical concentrations. The thickness increases with deposition time until the chemical reaction stops, after which the thickness remains constant. This type of behavior has been observed by various authors [5].

Translucent films were obtained by this method. The optical transmission spectra obtained from CdS films with different thicknesses are shown in Fig. 6.b.2 (a). Transmission for photon energies above the bandgap energy E_g correlates well with the thickness, i.e., better transmittance for thinner films. For photons with energy lower than E_g , the relationship between the transmittance and the thickness is not clear partly due to the interference fringes coming from several interfaces. The effect of CdCl_2 -treatment and annealing on transmittivity of these films is either negligible or slightly deleterious. A case of decreased transmission is given in Fig. 6.b.2(b).

The annealing with CdCl_2 treatment usually reveals white spots with sizes ranging from about 0.5 mm to 5 mm. Films annealed without CdCl_2 treatment do not show this feature. These spots are actually conglomerates of dendritic patterns of either Cd metal or some Cd-rich phase, as is indicated by energy dispersive x-ray spectroscopy (EDS) measurements made on the normal CdS and on the white spots. The EDS results are given in Table 6.b.2. For some CdS layers, we observed that the whole surface was covered with this dendritic pattern although in some cases the patterns were not very conspicuous to the naked eye.

Fig. 6.b.3(a) is an optical micrograph (OM) of a white spot showing the dendritic pattern and Fig. 6.b.3(b) is an SEM picture of the same region showing both the dendrites and the underlying CdS grains. We have experimental evidence that similar types of defects occur in CdCl_2 -treated CdTe films. The dimensions and the shapes of these patterns are strikingly similar to what Meyers et al. [6] observed in their CdS/CdTe cells using the electron beam induced current (EBIC) method. A possible mechanism for the formation of this pattern is either the uneven coating of CdCl_2 or Cd vapor transport from elsewhere on the surface to localized nucleation sites. Our preliminary experimental results support the latter possibility.

The white spots may act as shunt paths or blocking barriers, depending on the nature of the junctions formed with the CdS layer and subsequently with the CdTe layer, and thus cause poor cell performance. We indeed have observed that some junctions made on these CdS layers show low short-circuit currents. The dendritic pattern may also be responsible for the decrease of optical transmittance observed in some CdCl_2 -treated films, as mentioned earlier. CdCl_2

treatment on electrodeposited CdS is reported to improve the light J-V characteristics of CdS/CdTe cells [7]. Our results indicate that it may be only after a proper optimization that one would see a beneficial effect of CdCl₂ treatment on CdS made by the CBD method.

The surface morphology of CdS has been greatly improved by modifying the deposition procedure. The details of the new processing procedure will be published in a forthcoming paper. As is shown in Figs. 6.b.4(a) and 6.b.4(b), the "homogeneously nucleated particles" adsorbed on the surface have been reduced. The surface particles may become shunt paths if they fall out before or during the subsequent CdTe deposition. We will continue to investigate the effect of this "modification" on the properties of CdS films.

In order to study the effect of transparent conducting oxide (TCO) layers on the microstructures of CdS, we used substrates obtained from different manufacturers as listed in Table 6.b.3. Figs. 6.b.5 (a) and (b) show two different morphologies of SnO₂ layers. Fig. 6.b.4(b) and Fig. 6.b.6 are the surface of CdS layers deposited on these SnO₂ layers, respectively. The surface morphologies of CdS are close to that of the SnO₂ underneath. This suggests that the growth of CdS takes place ion-by-ion, not by the adsorption of colloidal CdS particles. Note that the CdS in Fig 6.b.6 shows almost no surface particles.

Fig. 6.b.1: Thickness vs. time relationship of CBD-grown CdS layers. Chemicals and their concentrations used for this run were: CdAc₂ (2 x 10⁻³M), NH₄Ac (40 x 10⁻³M), and (NH₂)₂CS (10x10⁻³ M). pH was 9.1 at the start.

Table 6.b.1 List of chemicals and their concentrations for CdS deposition.

Cadmium Acetate (Chloride)	$1.3 \times 10^{-3} \text{M}$
Ammonium Acetate (Chloride)	$5-6 \times 10^{-3} \text{M}$
Thiourea	$5-150 \times 10^{-3} \text{M}$
Ammonia	Used to adjust pH within 9 - 10

Table 6.b.2 Comparison of the composition analysis by EDS on two different regions of a CdS film: white spot and normal surface. The surface was coated with Au for SEM image enhancement.

Elements Region	Atomic%, Normal Region	Atomic%, White
Cd	29	46
S	37	19
Cl	0.00	0.00
Au	34	35

Table 6.b.3 List of SnO_2 /glass samples used for this study.

#	Type of Glass	Manufacturer of Coating	$R_s, \Omega/\square$
1	sodalime	Nippon Sheet Glass	4.2
2	sodalime	Nippon Sheet Glass	11
3	Corning7059	Solarex	9.1
4	sodalime	DAFC	7.3

Fig. 6.b.2 (a) Results of optical transmission measurements on as-deposited CdS films with different thicknesses. The films used here are the ones presented in Fig. 1. (b) Comparison of transmittance of 1000 Å thick CdS film before and after annealing. Chemicals and their concentrations were: CdCl₂ (2×10^{-3} M), NH₄Cl (5×10^{-3} M), and (NH₂)₂CS (150×10^{-3} M) (Measurement done by Dr. Y. Qu of CSM).

Figure 6.b.3 (a) Optical micrograph (x400) of CdS surface in white spotted region. (b) SEM picture of the same region showing CdS grains and the overlying dendrites.

Figure 6.b.4 SEM micrographs showing the surface of CdS films deposited (a) without process A and (b) with process A. Substrates were SnO₂-coated sodalime glass.

Figure 6.b.5 SEM pictures of SnO_2 surfaces. (a) SnO_2 on sodalime glass (sample 2) and (b) SnO_2 on Corning 7059 glass (sample 3).

Figure 6.b.6 SEM micrograph showing the surface of a CdS film deposited on SnO₂/Corning 7059 glass.

c. CdTe Deposition and Cell Fabrication

Significant progress was made in CdTe deposition during this reporting period. The "nodular growth" problem described in the previous annual report [8] was solved by closely controlling the tellurium concentration [Te]. The electrodeposition bath that had been used for module fabrication by Ametek was reassembled and is now being routinely used for CdTe deposition. High-quality CdTe films that have yielded 10.4% efficient CdS/CdTe/Au cells are grown reproducibly on a regular basis. The minority-carrier lifetime by time-resolved photoluminescence was measured by NREL to be 2.39 ns on a CSM CdTe film and a cell based on this film showed an efficiency of 9.58%.

The deposition conditions are similar to those described by Panicker et al.[9]. The films are annealed after CdCl₂ treatment at 410°C for 45 min in air. The samples are then rinsed and etched in 0.1% Br-MeOH solution for 30 s. We deposit Au back contacts through a mask by vacuum evaporation. The thickness of the Au contacts is not controlled and no heat treatment is done after the Au deposition. Indium solder is used for front contacts to the SnO₂ layers.

CdTe films grown by electrodeposition in our work have a faceted morphology as shown in Fig 6.c.1. This is usually a sign of high crystallinity. A cross-sectional SEM picture shown in Fig 6.c.2 reveals that the films have a dense, columnar structure. CdTe/CdS cells with areas of 0.03cm² and efficiencies up to 10.4% have been achieved from this process. Fig. 6.c.3 shows the result of current-voltage (J-V) measurement on such a cell. The cell has a series resistance of 5.3 Ω cm² which is significantly higher than those of cells reported in the literature [10]. The open-circuit voltage is significantly lower than the values reported by others [10].

The reason for the low V_{oc} may be due to (i) pinholes in the CdTe layers and/or CdS layers and (ii) the nature of the junction itself. Pinholes in the CdTe layers may be removed by a photoresist process. Table 6.c.1 illustrates the effect of the photoresist process. Two 1-cm² CdS/CdTe/Au cells were made on two CdTe pieces: one with the photoresist process (062393-1) and the other without (062393-2). As shown in Table 6.c.1, the two cells on 062393-1 show almost identical performances while the cells on 062393-2 show dramatic differences in V_{oc} 's and FF's probably due to pinholes. The pinholes are not observed in as-deposited films and it is only after CdCl₂ treatment and annealing that one can see them. We conclude that the photoresist process helps to produce uniform cell performances by removing the pinholes in CdTe layers. (The photoresist process which we have used in these studies is currently a proprietary technology.)

There is no post-deposition treatment for pinholes in the CdS layers. Therefore, a close control of the deposition and annealing process is required to obtain uniform, continuous films. The difficulty in this work is that there is no standard method to investigate the density of pinholes in CdS layers. Our experimental results show that V_{oc} typically increases with CdS thickness up to about 2000Å. CBD-grown CdS films thicker than 2000Å have not yet been tested. Thicker CdS films (3000Å) made by physical vapor deposition have been used to compare with CBD-grown films. The parameters of three dot cells are listed in Table 6.c.2. Although direct comparison between CBD-grown CdS and PVD-grown CdS is not yet possible

due to the thickness differences, these results indicate that V_{oc} 's as high as 0.762 V are achievable by electrodeposited CdTe films fabricated at CSM. We are currently developing a method to find an indication of the pinhole densities in the CdS layers and will correlate the results with the characteristics of cells based on those CdS layers.

Regarding the nature of the junction which affects the V_{oc} 's, the hole densities (p) of electrodeposited-CdTe layers are low ($< 10^{13} \text{ cm}^{-3}$) and as a result, the diffusion potential of the junction is low. On the other hand, p for vacuum-deposited CdTe films ranges between 5×10^{14} - $1 \times 10^{15} \text{ cm}^{-3}$, and p for CSS-deposited films may be as high as $1 \times 10^{16} \text{ cm}^{-3}$. The CdS/CdTe junctions based on the CdTe made by these techniques should have higher diffusion potentials and V_{oc} 's than electrodeposited CdTe cells. This point is discussed in Section 6f on modeling work using the ADEPT program. In addition, a lower hole density is detrimental to the contact resistance. In order to increase the hole density, an in-situ doping or post-deposition doping by diffusion during annealing may be considered.

In order to reduce the R_s of our cells we have made some C:Cu contacts to the CdTe layers based on procedures reported in the literature. Up to now, C:Cu contacts have shown performances inferior to those of plain Au contacts. We speculate that the electrodeposited CdTe films are electrically resistive, and that the contribution of the bulk series resistance from the CdTe layer to the total R_s is much larger than the contact resistance. Hence, reducing the back contact resistance may not have any significant effect. The other possibility is that the electrodeposited CdTe films have smaller grains and less dense microstructure than, e.g., vacuum-deposited CdTe so that diffusion of Cu into electrodeposited CdTe layers happens much faster and thus deteriorates the junctions. This idea implies that either a rigorous control of annealing conditions is required or that thicker CdTe layers should be used. The fabrication of ZnTe:Cu layers for back contacts is discussed later in Section 6d.

The combination of the best possible parameters obtained in this work, i.e., $V_{oc} = 0.762 \text{ V}$, $J_{sc} = 23.0 \text{ mA/cm}^2$, and $FF = 67.7\%$, gives a conversion efficiency of 11.9%. This number is slightly higher than the record efficiency of 11.2% that Ametek made using the same techniques. Even though the individual "best parameters" are not necessarily realizable in a single cell, we nevertheless believe that CSM has reproduced the Ametek technology and that further improvement of cell characteristics is possible.

Table 6.c.1. Comparison of CdTe cells with (#062393-1) and without (#062393-2) the photoresist treatment. The area of the cells was 1 cm^2 .

Sample#	Cell#	V_{oc} , V	J_{sc} , mA/cm^2	FF, %	Eff., %
062393-1	1	0.737	20.7	59.3	9.07
	2	0.729	20.7	58.5	8.85
062393-2	1	0.724	20.8	59.2	8.94
	2	0.601	20.5	37.8	4.67

Table 6.c.2. The cell parameters of CdTe/CdS cells which consist of electrodeposited CdTe on PVD-grown CdS films (3000Å thick). The area of the cells was 0.03 cm².

Sample#	Cell#	V _{oc} , V	J _{sc} , mA/cm ²	FF, %	Eff., %
063093	1	0.762	21.8	51.6	8.59
	2	0.750	23.0	56.7	9.84
	3	0.750	22.2	59.0	9.87

Fig. 6.c.1 SEM picture of electrodeposited CdTe film surface (#030493).

Figure 6.c.2. Cross-sectional SEM picture of electrodeposited CdTe film (#030493) deposited on a CdS/SnO₂/glass substrate.

CSM CdS/CdTe

Sample: YZ15-3(corner)

Temperature = 25.0°C

Dec 22, 1993 1:48 PM

Area = 0.03085 cm²

Spectrum: ASTM E 892-87 Global

Irradiance: 1000.0 Wm⁻²

$$V_{oc} = 0.7224 \text{ V}$$

$$I_{sc} = 0.6565 \text{ mA}$$

$$J_{sc} = 21.28 \text{ mAcm}^{-2}$$

$$\text{Fill Factor} = 67.68 \%$$

$$V_{max} = 0.5593 \text{ V}$$

$$I_{max} = 0.5739 \text{ mA}$$

$$P_{max} = 0.3210 \text{ mW}$$

$$\text{Efficiency} = 10.4 \%$$

Fig. 6.c.3 Light current-voltage measurement result on a CdS/CdTe/Au dot cell ($A=0.03 \text{ cm}^2$).

d. ZnTe:Cu Back Contacts

Although we have an ongoing effort to develop an alternative electro-chemical deposition technique, the ZnTe films doped with Cu described in this section were made by vacuum evaporation. The vacuum system is partitioned into two sections; one for a ZnTe powder source and the other for a Cu source. The ZnTe and Cu deposition rates are measured by separate thickness monitors. The deposition rates are typically 7-15 Å/sec for ZnTe and 0.35-2.2 Å/sec for Cu. Film thicknesses are about 1000Å. The source materials are evaporated from Mo boats and their temperatures are not directly controlled. The substrates are located at 20 cm above the sources and are not heated intentionally. The sources and the substrates are separated by a shutter. Some of the samples made in this study are listed in Table 6.d.1.

Metallic Te peaks were found in x-ray diffraction (XRD) patterns taken on some of the ZnTe films. ZnTe powders obtained from three different vendors and which were claimed to be "five nines" pure were used for comparison XRD measurements and we found that all contained several % of metallic Te (see Fig. 6.d.1). Materials from CERAC, ESPI, and Johnson Matthey were used in this investigation. It seems that the Te in the source material is the cause of the Te second phase in the deposited films. Raising the substrate temperature is one method to prevent the inclusion of Te into the films [11]. Another method is to remove the Te phase from the source material before the deposition by utilizing the difference between the vapor pressures of Te and ZnTe. The XRD pattern taken on a residual ZnTe powder source after several runs shows that the Te phase was removed (Fig. 6.d.1). The stoichiometry of the ZnTe source material seems to be Zn-rich judging from the fact that the zinc oxide phase is detected.

ZnTe films are obtained by maintaining the ZnTe source (using as-received material from vendors) at an intermediate temperature for about half an hour before opening the shutter. Fig. 6.d.2 shows an XRD pattern obtained from a ZnTe film which shows no peaks from any secondary phase. Optical transmission data are plotted in Fig. 6.d.3. The bandgap matches that reported for ZnTe very well and the transmittance values are similar to those reported by Ametek [12]. The sheet resistances of Cu-doped films prepared at CSM are between 2.0–5.0 $\Omega/\square$ which is much lower than those reported by Ametek [12]. This range seems to result from a Cu-rich phase as is shown in Fig. 6.d.4. When the Cu deposition rate is decreased to about 0.3Å/sec, we obtain a ZnTe film (#091493) with a sheet resistance of 6000 $\Omega/\square$ which is a typical number reported by Ametek, and the XRD pattern on this film does not show a second phase as shown in Fig. 6.d.4. Therefore, we conclude that the Ametek technology for depositing the ZnTe layer has been reproduced.

We have fabricated solar cells using the ZnTe:Cu contacts (#090293 and 091693). In order to see if the ZnTe:Cu layer helps reduce the series resistance of the cell, we compared the series resistance values obtained from CdS/CdTe/Au and CdS/CdTe/ZnTe:Cu/Au cells. The series resistance values were similar indicating that the ZnTe:Cu layer does not necessarily result in a better back contact. This result is confirmed by Dr. P. Meyers [13]. Since ZnTe contacts are not better than Au contacts in terms of R_s , ZnTe:Cu contacts will be applied only after we have optimized the CdS/CdTe junctions using Au back contacts.

Table 6.d.1 List of ZnTe films made by vacuum evaporation.

Sample No.	Substrate	Thick. Å	Cu doped?	Resistivity $\Omega / \square$	XRD	Comments
070893*	glass	1700	no	---	Te peaks only	Metallic appearance
072093	glass	1000	no	resistive	ZnTe peaks only	Transparent, red brown
072793-1*	glass	1000	no	---	---	Metallic appearance
072793-2*	glass	900	no	---	---	Metallic appearance
072893	glass	---	no	---	---	Metallic & red brown
073093	glass	1500	no	resistive	---	Transparent, red brown
080393	glass	2000	no	resistive	---	Transparent, red brown
080493	glass	2800	yes	5	---	Transparent, red brown
082693	glass	1300	no	---	---	Calibration for thickness monitor
083193-1	glass	3600	no	---	---	Calibration for thickness monitor
083193-2	glass	---	no	---	---	Calibration for thickness monitor
083193-3	glass	1400	yes	2	some CuTe peaks	Transparent, red brown
090293	CdTe	1700	yes	---	---	Cell's $R_s = 15 \Omega \text{ cm}^2$
091493	glass	1600	yes	6000	ZnTe peaks only	Transparent, red brown
091693	CdTe	1500	yes	---	---	Cell's $R_s = 16 \Omega \text{ cm}^2$

* Made by e-beam evaporation from chunks.

Chunk source used.

Fig. 6.d.1 XRD patterns of ZnTe powder used as source material for vacuum-deposition of ZnTe films: (a) as-received and (b) after several runs. The ZnTe powder was obtained from CERAC Inc., 5n purity.

Fig. 6.d.2 X-ray diffraction (XRD) pattern on a ZnTe film (500 Å) on glass deposited by vacuum evaporation. The substrate was at room temperature and a ZnTe powder sources was used.

Fig. 6.d.3 Optical transmission (measured by Dr. Yi Qu at NREL) data of an as-deposited, undoped ZnTe film on glass (v073093). The film was 1500Å thick.

Fig. 6.d.4 XRD patterns on as-deposited ZnTe:Cu/glass samples: (a) overdoped (#083193) and (b) lightly doped (#091493).

e. X-ray Studies

Both x-ray diffraction (XRD) and small-angle x-ray scattering (SAXS) are being used to characterize the crystal structures, residual stresses, and microstructures of CdTe and CdS thin films. Our recent application of SAXS to CdS films¹⁰ was the first use of this method to study such films, to our knowledge, and it yielded clear signals from dip-coated CdS before and after annealing as shown in Fig. 6.e.1(a). The change in shape of the SAXS curves leads to differences in size distributions of the scattering centers as suggested by the bar charts in Fig. 6.3.1(b). An increase in average size results from the annealing process. Possible origins of the scattering include grain-boundary scattering, microvoids, surface roughness, and multiple scattering. If attributed only to microvoids, for example, then based on the integrated intensity ($Q = \int I dh$) [14] we can give an upper limit to the volume fraction of 1.0 % in the as-deposited state. However, the growth of the scattering centers upon annealing, suggested by the size distributions, is consistent with expected grain growth due to this process. Although the XRD linewidths and SEM studies indicate the average grain size is much larger than those detected by SAXS, there could be non-negligible fractions of these very small grains remaining in the film after annealing and grain boundary scattering could be the source of the SAXS. Surface roughness does not seem likely based on STM and SEM observations of typical fluctuations of 50 nm coupled with no changes induced by annealing. At this stage of our studies we do not know whether multiple scattering effects are contributing to the SAXS.

Additional information on the microstructure is revealed by tilting a film in the x-ray beam. Sensitivity to this tilting indicates anisotropic SAXS due to oriented, non-spherical scattering centers. Decreases in intensity upon tilting indicate elongated scattering centers with their long axes preferentially oriented perpendicular to the film plane while increases in intensity could be due to pancake-like shapes lying preferentially within the film plane. A ratio of the integrated intensity measured in the non-tilted position to that measured at 45° (Q_0/Q_{45}) is a convenient method of describing this effect. A summary of the SAXS data from two CdS films prepared by dip-coating is given in Table 6.e.1. They behave similarly in that both show increases in SAXS upon a first annealing, although the amount of scattering is significantly different (based on the Q 's). A drop in Q after the second anneal of #1 is attributed to the further increase in average grain size so that the scattering regime is moved to lower angles where it is no longer detectable. Note also that there is a tilting effect before annealing(#2) and it disappears after annealing(#1). This is quite consistent with the more random distributions of grain orientations detected by XRD after annealing [8].

In order to compare the microstructures of CdTe films prepared by different methods, we first studied PVD-grown materials because it is easier to prepare special samples for SAXS measurements by this method than by electrodeposition. The SAXS characterization of a 0.12 μm CdS film deposited by PVD at NREL revealed no detectable signal, indicating a more homogeneous microstructure than the dip-coated material. Fig 6.e.2 shows this data in its raw form comparing the substrate signal with that from the CdS/substrate signal. Although this sample is much thinner than the dip-coated films, the SAXS signal is clearly much weaker even after normalizing by film thickness and an upper limit to the Q is included in Table 6.e.1. No tilting experiment was attempted due to the weak signal. XRD from the same film showed the

CdS to be the hexagonal phase but the linewidths from some of the peaks were significantly broadened consistent with the presence of at least some fraction of quite small grains or with the presence of inhomogeneous strain. Independent grain-size results from SEM or STM are not yet available.

Our first SAXS studies of CdTe have been made with PVD films deposited at NREL on SiO₂-coated c-Si substrates. Two films have been examined, one in the as-deposited state (#K112393) and the second after in-situ annealing (#K113093). Figure 6.e.3 shows the SAXS data which, when compared to that from CdS in Fig. 6.e.1, is comparatively much weaker and shows signals above the flat background level only below $h=1.5 \text{ nm}^{-1}$. The Q's of these two films are 0.03 and 0.12, respectively, in the same units as in Table 6.e.1. These small values suggest a very homogeneous microstructure. For example, such Q's, if attributed to microvoids, yield maximum volume fractions of 0.02 and 0.06 %. In view of the rather large size of the scattering centers, 10 nm, indicated by the signals at low h only, voids are not likely. Grain boundary scattering is the more likely mechanism and the increase due to the in-situ annealing is consistent with some recrystallization (revealed by XRD presented below) and formation of some smaller grains during this process.

XRD patterns from the same films used for the SAXS study are shown in Fig 6.e.4. There is a clear difference in that only the (111) planes are detected in the as-deposited film while all grain orientations are present after the in-situ annealing. Note that the vertical scale is the square root of the x-ray intensity in order to bring out any weaker peaks. There is a small peak due to Te precipitates (the only peak seen is that due to the (101) planes and these produce the strongest line of the Te pattern). We considered whether such precipitates could be the origin of the enhanced SAXS of this sample compared to that of the as-deposited sample, but a calculation of the required volume fraction of Te to give the observed Q is much too large (about 30%, due to the similarity of the electron densities of Te and CdTe). The XRD intensity of the Te peak is only 0.2% that of the CdTe (111) peak. No Te peaks were detected in the as-deposited film, suggesting that preferential evaporation of Cd during annealing leaves excess Te that then precipitates into pure Te particles.

Fig. 6.e.5 shows details of the CdTe (111) and (333) peaks. Little difference is seen in positions or widths of the (111) peaks but a clear shift to higher angles due to in-situ annealing is observed for the (333) peaks. The $K_{\alpha 1}$ and $K_{\alpha 2}$ peaks are also well resolved at this higher angle as expected due to the improved resolution at higher angles. The lower valley between these two peaks for the annealed film is indicative of a slightly narrower linewidth in this state. The differences in the (111) and (333) peaks at first seem contradictory since they are really from the same family of lattice planes, with the (333) being just the third-order Bragg peak of the (111). However, a more complete treatment of all the peaks in the form of a so-called Nelson-Riley plot, as shown in Fig. 6.e.7, demonstrates the source of the contradiction. A non-zero slope in this type of plot is indicative of the sample being not in the correct position relative to the rotation axis of the Bragg diffractometer (mounting the samples in exactly the correct position can be problematical for some sample geometries). Extrapolation of the data to $\cos^2\theta/\sin\theta$ yields an error-free value of the lattice constant. The values for the as-deposited and annealed samples are thus 0.6494 nm and 0.6475 nm, resp., both of which are distinct from that of pure CdTe

Table 6.e.1. SAXS results from CdS films deposited on crystalline Si wafers (75 μm thick) with a predeposit of ZnO (dip-coated samples) or SiO_2 (PVD sample).

Sample	Treatment	thickness (μm)	Q_0 (10^{-6}nm^{-2})	Q_0/Q_{45}
ZnO	as-deposited	.01	≤ 0.08	--
Dip-coated #1	as-deposited	~ 1.0	2.4	--
	annealed $450^\circ\text{C} \times 50\text{min}$		12	1.0
	annealed $450^\circ\text{C} \times 100\text{min}$		3.5	--
Dip-coated #2	as-deposited	~ 1.5	1.3	< 1
	annealed $450^\circ\text{C} \times 50\text{min}$		3.5	--
PVD#1	as-deposited	0.12	≤ 0.5	--

powder, 0.6483 (assumed stress-free, shown in Fig. 6.e.7). Based on the differences and the elastic constants of CdTe, we find the as-deposited film to be under a compressive residual stress of 48 MPa and the annealed film under a tensile residual stress of 35 MPa. The difference in thermal expansion coefficients of Si and CdTe could contribute to this effect. These values are $4.68 \times 10^{-6}/\text{K}$ and $4.9 \times 10^{-6}/\text{K}$, respectively.

Evidence of residual stresses is also found in the electrodeposited CdTe material on sodalime glass substrate as demonstrated in Fig. 6.e.8, which compares the lattice constants found after the CdCl_2 -annealing treatment and that from the pure CdTe powder. Note that the near-zero slopes here show more accurate sample positioning. In this case there is a clear compressive residual stress and its magnitude is 32 MPa, somewhat smaller than either of the two above stresses. The different substrate for this film (sodalime glass) could be a source of the different state of stress in the annealed state compared to that from the annealed film on Si. Also, the annealing conditions were significantly different, but both films show the recrystallization effect and the transition to more random grain orientations as documented by the intensity data in Table 6.e.2.

Table 6.e.2. Comparison of relative XRD peak intensities (integrated intensities) for PVD and electrodeposited (ED) CdTe films in as-deposited and annealed states. Intensities from the JCPDS file and high-purity CdTe powder are included.

(hkl)	PVD#112393 (as-deposited)	PVD#113093 (annealed)	ED#062393 (as-deposited)	ED#062393 (annealed)	Powder	JCPDS
(111)	100%	100%	100%	100%	100%	100%
(220)	0	10	<1	56 87		60
(311)	0	14	1	29 45		30
(400)	0	4	0	4 8		6
(331)	0	3	<1	12 16		10
(422)	0	7	<1	12 18		10
(333)	5	4	2	4 11		4

Fig. 6.e.1(a) SAXS pattern obtained from ZnO/Si substrate and with CdS overlying film ($h = 4\pi \sin\theta / \lambda$; $2\theta =$ scattering angle, $\lambda = 0.154 \text{ nm}$). (b) Size distribution of scattering centers as obtained from SAXS measurements on as-deposited CdS and after anneal.

Fig. 6.e.2 Comparison between the SAXS patterns obtained from ZnO/Si substrate and with CdS overlying film which was deposited by physical vapor deposition.

Fig. 6.e.3 SAXS data obtained from two PVD-grown films deposited on SiO₂/Si substrates. K112393 is as-deposited and K113093 was annealed in-situ.

Fig. 6.e.4 XRD pattern of the two different PVD-CdTe films used for SAXS measurements: as-deposited (K112393) and annealed in-situ (K113093).

Fig. 6.e.5 Comparison of the XRD CdTe (111) peaks from the two different PVD-CdTe films: as-deposited (K112393) and annealed in-situ (K113093).

Fig. 6.e.6 Comparison of the XRD CdTe (333) peaks from the two different PVD-CdTe films: as-deposited (K112393) and annealed in-situ (K113093).

Fig. 6.e.7 Comparison of the lattice constants of PVD-CdTe films: as deposited and annealed in situ.

Fig. 6.e.8 Comparison of the lattice constants between bulk CdTe powder and an annealed film made by electrodeposition. Lattice constants calculated from the values listed in JCPDS handbook are also plotted. θ is the Bragg angle.

f. Modeling of CdS/CdTe Junctions Using the ADEPT Program

The ADEPT (A Device Emulation Program & Tools) program developed by Purdue University is being used in this study. ADEPT has been previously applied to the study of CdS/CdTe and CdS/CuInSe₂ junctions [15]. A description of ADEPT is given by Gray and Lee [16].

ADEPT solves a set of three coupled nonlinear partial differential equations commonly referred to as the semiconductor equations. This set of equations consists of Poisson's equation and the hole and electron continuity equations. Simple drift-diffusion transport of carriers is assumed. This set of partial differential equations is discretized on a 1D (one dimensional) mesh. The resulting set of nonlinear difference equations is solved using a generalization of Newton's method.

Figures 6.f.1 (a), (b), and (c) are the band diagrams of a CdS/CdTe junction at equilibrium, at zero bias under light, and under the open-circuit condition. The doping density and the thicknesses of CdS and CdTe are:

$$\text{CdS:N}_d = 1 \times 10^{17} \text{ cm}^{-3}, \text{ thickness} = 0.1 \text{ } \mu\text{m}$$

$$\text{CdTe:N}_a = 1 \times 10^{13} \text{ cm}^{-3}, \text{ thickness} = 2.0 \text{ } \mu\text{m}.$$

The doping density of CdS corresponds to a reported value of the electron density of dip-coated CdS after annealing [17]. The doping density of CdTe is estimated from a reported resistivity value for electrodeposited CdTe after annealing assuming $\mu_p = 1 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$.¹⁵ We chose to investigate only the CdS/CdTe structure instead of the CdS/CdTe/ZnTe structure because, since the ADEPT program does not include tunneling current and assumes an ideal back ohmic contact, these will produce the same results.

Fig. 6.f.1(a) shows that the whole CdTe layer is depleted under equilibrium conditions as discussed in reference 18. Because of the built-in electric field in the CdTe, an improved carrier-collection efficiency is expected. It should be noted that there is a spike in the conduction band at the CdS/CdTe interface which should partially block the electron flow from the CdTe to the CdS side and increase the interface recombination. Figures 6.f.1(b) and (c) show quasi-Fermi levels for both electrons and holes (E_{fn} and E_{fp} , respectively). The effect of back surface recombination on electron density in CdTe is shown by E_{fn} and the effect of front surface recombination of holes in the CdS layer is shown by E_{fp} .

Fig. 6.f.2 is a light current-voltage (LJV) curve of the CdS/CdTe junction produced by the ADEPT program under the given conditions. It was assumed that there is no surface reflection, no interface recombination, no external R_s , and infinite R_p .

Figs. 6.f.3 (a) and (b) show cell performances with different CdTe thicknesses. The highest efficiency is predicted to occur at 1.5 - 2 μm which coincides well with the report of Ametek [12].

Further increase of the thickness results in the decrease of FF and J_{sc} due to the bulk R_s . However, when the doping density is increased to $1 \times 10^{16} \text{ cm}^{-3}$, the thickness of CdTe has virtually no effect on cell performance beyond $2 \text{ } \mu\text{m}$, as is shown in Fig. 6.f.4(a) and (b). A lower J_{sc} is predicted because of the smaller depletion region and a higher V_{oc} because of higher built-in potential at the junction.

Figs. 6.f.5 (a) and (b) show cell performances with different doping densities in the CdTe layer. As mentioned above, J_{sc} decreases and V_{oc} increases with CdTe doping. Control of hole density (p) up to $1 \times 10^{16} \text{ cm}^{-3}$ in the CdTe layer is reported to be achieved by changing the substrate temperature in close-spaced sublimation (CSS) without extrinsic doping [19]. This may be one of the reasons why the USF group must use high growth temperatures (up to 625°C) to produce cells with the highest V_{oc} 's [20]. In general, vacuum deposited CdTe shows hole densities between 1×10^{14} - $1 \times 10^{15} \text{ cm}^{-3}$ [21]. This may be one of the reasons why the V_{oc} 's of CdTe/CdS deposited by vacuum evaporation and CSS show higher V_{oc} 's than those of CdTe/CdS (Ametek, 767 mV and University of Queensland, 720 mV) made by electrodeposition ($p \leq 1 \times 10^{13} \text{ cm}^{-3}$, typically) [10]. The V_{oc} reported by the British Petroleum (BP) group is much higher even though they use electrodeposition. They report that their cell has a p-n structure rather than p-i-n implying higher hole density in the CdTe [22].

This model predicts a decrease of J_{sc} with an increase of hole density. This is only true if the minority carrier lifetimes (τ) are the same regardless of the hole density. However, vacuum-deposited CdTe films may have higher τ which should compensate the adverse effect of high hole density for carrier collection due to decreased depletion width. This may explain why the J_{sc} 's of some vacuum deposited cells are higher than those of electrodeposited cells.

Figs. 6.f.6(a) and (b), and Figs. 6.f.7(a) and (b) show model cell performances as a function of electron densities (n) in the CdS layer when $p=1 \times 10^{13} \text{ cm}^{-3}$ and $1 \times 10^{15} \text{ cm}^{-3}$ in CdTe, respectively. According to the model of Anderson, increasing n in CdS must increase the built-in potential [23] and thus the V_{oc} of the cell and also depletion width in CdTe layer which should increase J_{sc} . However, the model predicts the opposite for $p=1 \times 10^{13} \text{ cm}^{-3}$. As for $p=1 \times 10^{15} \text{ cm}^{-3}$, J_{sc} decreases and V_{oc} increases only after $n > 1 \times 10^{16} \text{ cm}^{-3}$. For both cases, the highest cell efficiency can be obtained when $n=1 \times 10^{16} \text{ cm}^{-3}$. This result suggests that the electron density in CdS needs to be optimized, e.g., by annealing as is reported in reference 17.

Fig. 6.f.8 shows the effect of CdS thickness. In general, the model predicts better performances for thinner CdS because the model does not take into account problems such as shunt paths which occur when the CdS is too thin. It does account for the surface recombination at the CdS front surface, though. The cause for the increase of V_{oc} for thickness larger than $0.3 \text{ } \mu\text{m}$ is not yet understood.

We will continue the modeling study using ADEPT including parameters such as surface reflection and interface recombination velocities. It is believed that using the ADEPT program will enlarge our understanding of how CdS/CdTe cells operate and enable us to better analyze and predict cell performances. It will also provide guidance on which parameters might most profitably be optimized for improved cell quality.

Fig. 6.f.1 Energy band diagram of CdS/CdTe junctions constructed by ADEPT program: (a) at equilibrium, (b) at zero bias under illumination (AM 1.5), and (c) near open-circuit condition (at 0.8 V). The parameters were: $N_d = 1 \times 10^{17} \text{ cm}^{-3}$ and thickness = $0.1 \text{ } \mu\text{m}$ for CdS, and $N_a = 10^{13} \text{ cm}^{-3}$ and thickness = $2 \text{ } \mu\text{m}$ for CdTe.

Fig. 6.f.2 Light current-voltage curve for junction illustrated in Fig. 6.f.1.

Fig. 6.f.3 (a) (b) Cell performance data with different CdTe thicknesses. CdS has $N_d=1 \times 10^{17} \text{ cm}^{-3}$ and $t=0.1 \mu\text{m}$. For CdTe, $N_a=1 \times 10^{13} \text{ cm}^{-3}$ (simulations are from ADEPT modeling program).

Fig. 6.f.4 (a) (b) Cell performance data with different CdTe thicknesses. Parameters are the same as Fig. 6.f.3 except that $N_a=1 \times 10^{16} \text{ cm}^{-3}$ (simulations are from ADEPT modeling program).

Fig. 6.f.5 (a) (b) Cell performance data for different doping density in CdTe layer. For CdS, $N_d=1 \times 10^{17}$ cm⁻³ and $t=0.1$ μ m. The thickness of CdTe is 2.0 μ m (simulations are from ADEPT modeling program).

Fig. 6.f.6 (a) (b) Cell performance data with different doping density in CdS layer. For CdTe, $N_a=1 \times 10^{13} \text{ cm}^{-3}$ and $t=1.5 \text{ } \mu\text{m}$. The thickness of CdS layer is $0.1 \text{ } \mu\text{m}$ (simulations are from ADEPT modeling program).

Fig. 6.f.7 (a) (b) Cell performance data with different doping density in CdS layer. Same condition were used as in Fig. 6.f.6 except that $N_s=1 \times 10^{15} \text{ cm}^{-3}$ (simulations are from ADEPT modeling program).

Fig. 6.f.8 Cell performance data with different CdS thicknesses. For CdTe, $N_a=1 \times 10^{13} \text{ cm}^{-3}$ and $t=1.5 \mu\text{m}$. For CdS, $N_d=1 \times 10^{17} \text{ cm}^{-3}$ (simulations are from ADEPT modeling program).

7. Summary and Plans

We have made substantial progress on many of the "Phase II" tasks as listed in Section 5 of this report. Regarding film growth techniques, dip-coating is established as a viable process for the deposition of the n-type CdS layer. In the case of the CdTe layer, we have continued to gain a significant understanding of the basic electrochemistry of this material and have established a foundation for further improvements. We are continuing to work on an electrochemical process to deposit thin films of ZnTe.

With regard to device fabrication, dot cells of regularly increasing efficiency have been fabricated in the past two years of the project. We have developed a proprietary photoresist technique for blocking pinholes in the CdTe layer and expect to demonstrate high-efficiency 1 cm^2 cells in the near future.

In view of the results of Phases I and II of this project, a revised list of Phase III tasks and goals is given on the following page. This includes the original list of Phase III tasks as well as several tasks which were not completed on schedule in Phase II. Among the latter, photoenhancement will be considered as we continue to optimize the procedures for high quality film growth. We have developed a test apparatus for rapid thermal processing and will employ it for various studies in Phase III. A group of students is currently working on the preliminary design of a large-scale process for the production of CdTe modules. Their report will be available early in the Phase III period. Finally, we will pursue the development of microscopic probes such as STM for characterizing grain boundaries and interfaces.

8. Phase Three Tasks (Revised)

High Quality Film Growth Techniques

1. Continue to optimize the procedures of preference for the fabrication of CdS, CdTe, and ZnTe layers.
2. Conduct experiments with rapid thermal annealing.
3. Combine the selected processes for individual layers into a single procedure for the fabrication of entire cells.
3. Determine the most effective processing steps for the mitigation of electronic traps.
4. Publish results in open literature.

Device Fabrication

1. Demonstrate a 13%, 1 cm² cell.
2. Develop the preliminary design of a large-scale process suitable for the production of CdTe modules.
3. Develop a manufacturable module which incorporates the technologies described above, including appropriate encapsulation.

Material Analysis and Device Characterization

1. Demonstrate the use of STM or other techniques to characterize the electrical potential distribution near grain boundaries and interfaces as it relates to the depression of V_{oc} .

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10. Appendices

a) Personnel

Fifteen individuals contributed to this work during the current reporting period. Their names, titles, and representative responsibilities are summarized below. Those who have been involved during just a portion of the project period are noted.

Permanent Faculty

1. Thomas E. Furtak, Professor of Physics: electrochemistry, optical properties
2. John U. Trefny, Professor of Physics: project coordinator
3. Noboru Wada, Associate Professor of Physics: Raman spectroscopy (left CSM, June, 1993)
4. Don L. Williamson, Professor of Physics: XRD, SAXS
5. Donghwan Kim, Research Associate: materials processing and characterization (promoted to Research Assistant Professor, November, 1993).

Research Associate; Temporary Faculty

6. Lianghuan Feng, Visiting Professor (since February, 1994)

Students

7. Esam Al-Kaoud, Graduate Research Assistant; electrochemical processing (January, 1994-present)
8. Dahong Du, Graduate Research Assistant: CdS processing
9. Andrew Johnson, Graduate Research Assistant; TCO coatings at NREL (May, 1993-present)
10. Jeanne McGraw, Graduate Research Assistant: employed part-time by Golden Photon (November, 1993-present)
11. Scott Pozder, Graduate Research Assistant: electrochemical processing
12. Bin Qi, Graduate Research Assistant: materials characterization (August, 1993 - present)

13. Yi Qu, Graduate Research Assistant: TCO coatings (left CSM, December, 1993)
14. Jason Selby, Graduate Research Assistant: four-point probe and electrodeposition of ZnTe (January, 1993 - present)
15. Yuming Zhu, Graduate Research Assistant: I-V measurements (January, 1993 - present)

b) Laboratory Improvements

Since the inception of this project, Colorado School of Mines has spent or committed more than \$100,000 for laboratory improvements and equipment upgrades. The majority of these funds has been used to provide the processing laboratory with modern, filtered fume hoods and other hardware related to the safety of staff members and students working on the project. These installations were completed in the spring of 1993. Plans to enlarge the facilities are currently being developed.

c) Publications

1. D. Kim, S. Pozder, B. Qi, Y. Zhu, T.E. Furtak, D.L. Williamson, and J.U. Trefny, Proc. 12th NREL Review Meeting, Denver, Colorado, October 1993, to be published.
2. "Electrical and optical properties of ion beam sputtered ZnO:Al films as a function of film thickness," Qu, Y. , Gessert, T.A., Ramanathan, K., Dhere, R.G., Noufi, R., Coutts, T.J., J. Vac. Sci. & Technol. 11 996 (1993).
3. "Electrical and optical properties of Al-doped ZnO films as a function of Al doping level," Yi Qu, T.A. Gessert, and T.J. Coutts, to be published in Thin Solid Films.
4. "A study of ion-beam-sputtered ZnO films as a function of deposition temperature," Y. Qu, T.A. Gessert, T.J. Coutts, and R. Noufi, to be published in Journal of Vacuum Science and Technology.

REPORT DOCUMENTATION PAGE

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OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE July 1994		3. REPORT TYPE AND DATES COVERED Subcontract Report, 20 March 1993 - 19 March 1994	
4. TITLE AND SUBTITLE Polycrystalline Thin Film Cadmium Telluride Solar Cells Fabricated by Electrodeposition				5. FUNDING NUMBERS C: XG-2-11036-4 TA: PV431101	
6. AUTHOR(S) J.U. Trefny, T.E. Furtak, D.L. Williamson, D. Kim					
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Colorado School of Mines Department of Physics Golden, CO 80401				8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393				10. SPONSORING/MONITORING AGENCY REPORT NUMBER TP-451-7046 DE94011848	
11. SUPPLEMENTARY NOTES NREL Technical Monitor: B. von Roedern					
12a. DISTRIBUTION/AVAILABILITY STATEMENT				12b. DISTRIBUTION CODE UC-273	
13. ABSTRACT (Maximum 200 words) This report describes the principal results of work performed during the second year of a 3-year program at the Colorado School of Mines (CSM). The work on transparent conducting oxides was carried out primarily by CSM students at NREL and is described in three publications listed in Appendix C. The high-quality ZnO produced from the work was incorporated into a copper indium diselenide cell that exhibited a world-record efficiency of 16.4%. Much of the time was devoted to the improvement of cadmium sulfide films deposited by chemical bath deposition methods and annealed with or without a cadmium chloride treatment. Progress was also made in the electrochemical deposition of cadmium telluride. High-quality films yielding CdS/CdTe/Au cells of greater than 10% efficiency are now being produced on a regular basis. We explored the use of zinc telluride back contacts to form an n-i-p cell structure as previously used by Ametek. We began small-angle x-ray scattering (SAXS) studies to characterize crystal structures, residual stresses, and microstructures of both CdTe and CdS. Large SAXS signals were observed in CdS, most likely because of scattering from grain boundaries. The signals observed to date from CdTe are much weaker, indicating a more homogeneous microstructure. We began to use the ADEPT modeling program, developed at Purdue University, to guide our understanding of the CdS/CdTe cell physics and the improvements that will most likely lead to significantly enhanced efficiencies.					
14. SUBJECT TERMS polycrystalline thin films ; cadmium telluride ; electrodeposition ; photovoltaics ; solar cells				15. NUMBER OF PAGES 58	
				16. PRICE CODE A04	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL		