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Elimination of Internal Contamination on Semiconductor Devices (Protective Coatings)

Kansas City Division

T. Castillo

KCP-613-5433

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Final Report

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**ELIMINATION OF INTERNAL CONTAMINATION
ON SEMICONDUCTOR DEVICES
(PROTECTIVE COATINGS)**

T. Castillo

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Final Report
T. Castillo, Project Leader

Technical Communications
Kansas City Division

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Abstract

Characterization results are described of epoxy and gel coatings that were applied to leadless chip carriers (LCC) and TO-46 semiconductor packages. Samples included silicon dioxide, liquid epoxy, epoxy, RTV silicon, and silicon gel; and a standard test sequence was followed. Test results and coating application feasibility for semiconductor packages and military applications are discussed.

Summary

Several epoxy and gel coatings were applied to leadless chip carriers (LCCs) and TO-46 semiconductor packages in an effort to eliminate potential internal shorts. Most of the electrical and mechanical characterization was performed using only the TO-46 package. The coatings were applied on LCC packages to determine coating application feasibility. A standard test sequence was followed for all devices.

Coatings included silicon dioxide, liquid epoxy, epoxy, RTV silicon, and silicon gel. No satisfactory results were achieved. All coatings failed to withstand minimum testing requirements of a high-reliability device.

Discussion

Scope and Purpose

A study was performed using epoxy and gel coatings on TO-46 and LCC package prototypes. The prototypes were assembled at AlliedSignal Inc., Kansas City Division (KCD), using industry standard TO-46 and LCC packages and a 2C222AHV Motorola die. The bulk of the electrical and mechanical characterization was performed using only the TO-46 package. The coatings were applied on LCC packages to determine coating application feasibility.

Prior Work

In the past conformal coatings were used to protect the die and to reduce the chance of internal package shorts. Today most semiconductor manufacturers do not apply coatings to their die. Lessons learned from coatings have caused manufacturers to eliminate the coating process. Coatings were believed to cause detached wires and to outgas contaminants internal to the package. Most recently it was believed that coatings have improved and that new materials would not outgas.

Activity

Silicon Dioxide

Devices were coated using a silicon dioxide clear coating. The vendor applied the coating to the packages by spin coating. In the process of applying the coating, the vendor could not control the

process to avoid placing SiO₂ around the seal perimeter of the packages, thus creating hermetic seal failures. Typical yields after the coating application for the TO-46 package were 89% and 15% for the LCC package.

A group of SiO₂-coated devices underwent the test sequence defined in Figure 1. Test results are shown in Table 1. The groups contained 21- and 42-piece group samples. The 21-piece group had already been exposed to some temperature cycling. Failure analysis was performed on rejects which had undergone electrical and mechanical test sequence. Failure modes ranged from handling damage (damaged wires--shorts) to electrical overstress.

Failure analysis provided good visual data on nonadherence of SiO₂ to gold plating and die. Failure analysis also indicated that this coating will craze/crack (Figure 2). Residual gas analysis (RGA) was performed on some samples which provided readings from 202 to 9049 ppm. A second group of samples was pulled for RGA which provided readings which ranged from 187 to 9304 ppm. The second test was performed to verify validity of the first sample group. RGA results are summarized in Table 2.

Liquid Epoxy

A group of devices was coated with a liquid epoxy (glob type) coating. Figure 3 shows examples. The coating was applied using a manual syringe process. The devices underwent the test sequence described

NO.	TEST ACTIVITY
1	FINE LEAK
2	GROSS LEAK
3	AMBIENT ELEC
4	-55°C ELEC
5	150° ELEC
6	HIGH TEMP STORAGE
7	POST STORAGE ELEC
8	TEMP CYCLING
9	POST CYCLING ELEC
10	PRE B/I ELEC
11	BURN-IN
12	PRE B/I ELEC
13	OP LIFE
14	POST OP LIFE ELEC
15	HTRB
16	POST HTRB ELEC
17	CONSTANT ACC.
18	POST ELECTRICAL
19	MECHANICAL SHOCK
20	POST ELECTRICAL
21	VIBRATION
22	POST ELECTRICAL

Figure 1. Test Sequence for Coated Devices

in Figure 1. Test results are shown in Table 1. The failures obtained as a result of the test sequence were submitted to failure analysis for evaluation, but the evaluation was hindered because of the dark coating. The dark coating made

internal visual analysis impossible to perform. The package could not be internally visually analyzed to determine if there were any burnt spots on the die or detached wire bonds. Attempts to perform failure analysis were made by trying to remove the coating with a reactive ion etching process. Using this process it was concluded that some of the failures obtained were due to a disconnected wire at the die, probably caused by the thermal expansion property of the coating. Some of the failures were inconclusive because the etch process had etched away the wires.

Other attempts were made to perform a failure analysis with a step-by-step cross section on those devices which had been verified as opens. The cross section would progress across the emitter and base leads first in an attempt to determine if either the base or emitter wire had become detached. Then the cross section would progress to the die area to determine if the thermal expansion stresses of the epoxy had dislodged the die from the header. Finally the cross section would progress towards the wire/die interface to determine if the wires had become detached from the die. On one failure it was discovered that the emitter wire had become detached from the die.

It would have been ideal if devices had been fabricated with gold wires. The gold wires would have allowed for X-rays which may have determined whether or not the wires had become detached from the post or the die due to thermal expansions of the coating material. The fabricated devices had aluminum wire.

Table 1. Test Results for Coated Devices

Sequence	Silicon Gel	RTV Silicon	SiO ₂		Liquid Epoxy
			42-Piece Group	21-Piece Group	
Fine Leak	0/20	0/23	0/42		0/23
Gross Leak	0/20	0/23	0/42		0/23
Ambient Elec	1/20	0/23	10/41		6/23
-55°C Elec	0/19	0/23	0/31		1/17
150°C Elec	0/19	0/23	0/31		0/16
High Temp Storage					
Post Storage Elec	0/19	5/23	0/31		0/16
Temp Cycling			31		
Post Cycling Elec	0/19	0/18	0/31		1/16
Pre B/I Elec				1/20	0/15
Burn-in		18		19	
Post B/I Elec	0/19	12/18		1/19	0/15
OP Life				18	
Post Op Life Elec	0/19	0/6		0/18	0/15
HTRB				18	
Post HTRB Elec	0/19	1/6		0/18	0/15
Constant Acc			10		7
Post Electrical	4/18	5/5	0/10		0/7
Mechanical Shock	14		10		7
Post Electrical	0/14		0/10		0/7
Vibration	14		10		7
Post Electrical	0/14		2/10		0/7

Figure 2. SiO_2 Coating Showing Cracked Condition

Table 2. Test Results for Residual Gas Analysis (H₂O)

Sample		Liquid Epoxy	RTV Silicon	Silicon Gel	SiO ₂	
Coated	1	No Pressure*	No Pressure	No Pressure	9049**	9304**
	2	No Pressure	No Pressure	No Pressure	6680**	187
	3	10,728	No Pressure	No Pressure	202	4414
	4				2105	474
Control	1	No Samples	3128	6515**	No Samples	
	2	No Samples	2880	4893	No Samples	
	3	No Samples	5330**	8335**	No Samples	
	4	No Samples		5916**	No Samples	

*"No Pressure" implies that the probe was not able to draw detectable pressure from the cavity to obtain a reliable reading. The probe probably punctured coating material.

**Failed 5000 ppm maximum limit.

Additional temperature cycling (50 cycles) was performed on some of the remaining electrically functional devices. The additional temperature cycling was performed to determine if the temperature extremes would induce any thermal expansion failures. The test resulted with one reject after 45 cycles and another after 50 cycles. The failure had failed lcbo 10 nanoamps maximum limit with readings of 10.24 nanoamps and 128 nanoamps. Failure analysis of the rejects was not conclusive since previous attempts to remove coating had not been effective.

Epoxy

Another glob type epoxy was also evaluated. Early attempts to apply the epoxy to the TO-46 packages were unsuccessful. The application process was difficult to control. The epoxy height after curing was higher than the lid height, which created a dome lid after welding the lid onto the header. Again, the coating was a dark coating which would have made failure analysis difficult to perform.

It is impossible to completely conclude that the failures were attributed to the environmental conditions that the package was exposed to during the test sequence, because some of the failures may have been induced by handling damage caused by the coating process.

RTV Silicon

A clear RTV semiconductor protective coating was applied using a syringe process. With continuous progression of this experiment it was decided that control samples were necessary for residual gas analysis. Therefore, control samples were sealed without the coating at the same time the devices with the coating were sealed.

An initial visual examination was performed on both LCC and TO-46 packages. The LCC packages did exhibit some coating overflow onto the seal perimeter. Examples are shown in Figure 4. The LCC packages submitted for seal obtained 21 gross leak failures and two fine leak

Figure 3. Devices Coated With Liquid Epoxy

Figure 4. Devices Coated With RTV Silicon

failures, which would verify that RTV material was on the seal perimeter. The TO-46 packages did not obtain any hermetic seal failures, as shown in Table 1.

It was also discovered that the material was contaminating the sealer. Only the TO-46 packaged devices underwent the test sequence defined in Figure 1. The entire test sequence was not completed because all samples had failed prior to completing the test sequence (Table 1). Failure analysis performed on the rejects revealed that the majority of the devices had failed because the majority of the wires (base/emitter) had become detached either at the die or the post. The failures occurred after having completed some type of temperature effects test (that is, high-temperature storage, burn-in). It appears as if the high-temperature conditions may have caused the coating's thermal expansion characteristic to either expand or contract, resulting in detached wires.

The last group of failures had failed post-constant acceleration. The failure analysis performed on these failures provided the same results as preceding failures, detached wires. It is believed that these failures occurred as a result of the coating material shifting internally (poor adhesion) to the package during the constant acceleration test process which applied forces on the wires, thus causing the wires to become detached at their weakest point. This is the heel of the wire where the wire was compressed to make attachment to either the die or post. RGA results are summarized in Table 2.

Silicon Gel

A transparent silicon gel protective coating was applied using a syringe process. The coating sample underwent the test sequence described in Figure 1. The completed test results are shown in Table 1. The failure analysis results provided a detached wire and bent wires touching the can. Figure 5 shows an example. The bent wires were probably induced by handling at either the coating application or sealing process. RGA results are summarized in Table 2.

Accomplishments

The coating evaluation verified that of the coatings studied none would have met or withstood the necessary high-reliability requirements for military applications. The test sequence performed can best be described as a typical minimum test sequence for device characterization. The coatings would not have been capable of withstanding even far adverse conditions.

All coatings would have made the failure analysis process difficult to perform on critical applications. It was learned that without the proper controls or methodology the coatings cannot be removed effectively without overetching the wires or the die. Dark coatings such as liquid epoxy would not be applicable for hi-rel devices where preliminary failure analysis usually commences with an internal visual examination of the active areas on the die before progressing into an in-depth failure analysis.

Figure 5. Device Coated With Silicon Gel

Future Work

Consideration for a follow-on evaluation would be to evenly distribute a thin layer (spin process similar to SiO_2 process) of coating over the die and wires instead of a glob type (syringe process) as used in this evaluation. The syringe coating process used in this evaluation would have been difficult to apply in an actual assembly process without reducing yields and increasing cost.

The use of coatings for elimination of potential internal shorts will require a more extensive coating evaluation and feasibility study than was applied in this evaluation. It would be ideal, in an effort to minimize the possibility of internal shorts, for a

manufacturing facility to maintain a controlled clean environment before adopting a coating process that would require an immense process of qualifications. One can say that manufacturers' early fears and concerns still exist. It can be concluded that none of these coatings will withstand the minimum testing requirements of a hi-rel device.

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