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Development of Concentrator Cells: Technical Status Report Phase 1 Report

Applied Solar Energy Corporation
15251 East Don Julian Road
City of Industry, CA 91746

Prepared by Sandia National Laboratories Albuquerque, New Mexico 87185
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Technical Status Report

Phase 1 Report

Applied Solar Energy Corporation
15251 East Don Julian Road
City of Industry, CA 91746

Contract 54-2191B

ABSTRACT

The microgrooved passivated emitter solar cell approach combines a thin diffused top junction layer of approximately $0.2\mu\text{m}$ depth and $120\text{-}180\Omega/\square$ sheet resistance with a thin (100-200Å) silicon dioxide surface passivation layer. The front gridlines sit on top of a heavily diffused N++ region to reduce contact resistance between front gridlines and the N surface. High-quality float zone silicon with nominal resistivity of $0.20\Omega\text{-cm}$ or $0.15\Omega\text{-cm}$ is used for this work. To achieve the highest possible concentration performance and lower system cost, the cell area was reduced to 1 square centimeter from 1.58 square centimeters used at the University of New South Wales. The gridline spacing is 127 microns designed to match the available prismatic cover. The baseline process requires four lithographic masking steps. A single lift-off process for evaporated gridlines is used to provide 8-microns-thick metallization to avoid the non-uniform metal plating and disposal of hazardous plating solutions. The front and back contact materials are space-qualified, vacuum-deposited layers of titanium-palladium and silver. A double-layer antireflection coating of TiO_2 and Al_2O_3 is used to reduce surface reflection from the cells; this antireflection coating is designed to match with the SiO_2 passivation layer. Four different gridline widths (20, 16, 8, and 2 microns) were tested and evaluated for the best performance at high intensities. A three-level lithographic masking process was evaluated for reduced costs and a five-level lithographic masking process was evaluated for increased yield.

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1.0 Objectives of Contract

2.0 PESC Technology

The microgrooved PESC structure (Figure 1) developed at UNSW has been transferred to ASEC. The PESC approach combines a thin diffused top junction layer of approximately $0.2\mu\text{m}$ depth and $120\text{-}180\ \Omega/\square$ sheet resistance with a thin ($100\text{-}200\text{\AA}$) silicon dioxide surface passivation layer. The front gridlines sit on top of a heavily diffused N^{++} region to reduce contact resistance between front gridlines and the N surface. High quality float zone silicon with nominal resistivity of $0.20\ \Omega\text{-cm}$ or $0.15\ \Omega\text{-cm}$ is used for this work.

Figure 1. Schematic Diagram of a Microgrooved Passivated Emitter Solar Cell (PESC). AR Coating is not shown.

To achieve the highest possible concentration performance and lower system cost, the cell area was reduced to 1 square centimeter from 1.58 square centimeter used at UNSW. The gridline spacing is 127 microns designed to match the available prismatic cover. The baseline process requires four lithographic masking steps. A single lift-off process for evaporated gridlines is used to provide 8-microns-thick metallization. This process is used

to avoid the non-uniform metal plating and disposal of hazardous plating solutions. The front and back contact materials are space qualified, vacuum deposited layers of titanium-palladium and silver. A double-layer antireflection coating of TiO_x and Al_2O_3 is used to reduce surface reflection from the cells; this antireflection coating is designed to match with the SiO_2 passivation layer. Four (4) different gridline widths (20, 16, 8 and 2 microns) were tested. These gridline widths were evaluated for best performance at high intensities, (see 3.2).

A three-level lithographic masking process was also evaluated for reduced costs. In addition, a five-level lithographic masking process was evaluated for increased yield.

Cell processing utilizes an existing silicon production facility under production conditions. No new equipment was required but some equipment was modified and dedicated for this project.

2.1 Process Sequence

Table 1 lists the baseline processing sequence used to fabricate PESC cells at ASEC. This process sequence is the four-mask process developed at UNSW.

2.2 Modifications

Two optional process sequences were added to the baseline process to further evaluate cost/efficiency trade offs. The first modified process sequence involves the elimination of the masking step prior to the N^{++} diffusion. This is accomplished by performing the diffusion step before the microgrooves are etched in the front surface. Following the diffusion step, the microgroove patterning and etching is performed which removes the heavily diffused N^{++} regions inside the microgrooves. The N^{++} regions under the contact finger areas and the peaks between the microgrooves however remain. The revised process sequence is outlined in Table 2.

Table 1. Standard processing sequence of PESC concentrator cells.

STEP	PARAMETERS
1. Wafer selection	0.2 Ω -cm, (100), FZ, p-Si, 280 μ m thick, 3 inch
2. Oxide growth	1000°C, 1 hr, in TCA, $\sim$ 1000Å SiO ₂
3. 1st masking, etch	Microgrooves on the active area
4. μ -Groove etching	KOH(8%, w/v), 70°C, 8 min
5. Oxide Removal	Buffered HF, 3 min
6. Oxide growth	1070°C, 5 hr, in TCA, $\sim$ 3000Å SiO ₂
7. 2nd masking, etch	N ⁺⁺ region
8. Phosphorus diffuse	Solid source, 930°C, 30 min, 15 Ω /■
9. Oxide growth	1000°C, 40 min, in TCA, $\sim$ 1500Å SiO ₂
10. 3rd masking, etch	Cell front junction, planar
11. Phosphorus diffuse	Solid source, 830°C, 20 min, 150 Ω /■
12. Back Al deposition	Vacuum evaporation, 1 μ m
13. Dry oxidation	950°C, O ₂ : 3 min, N ₂ : 3 hr, $\sim$ 100Å SiO ₂
14. 4th masking, etch	Metallization
15. Top metallization	Ti-Pd-Ag: 1200Å-500Å-8 μ m
16. Lift off	Ultrasonic in acetone
17. Back metallization	Al-Ti-Pd-Ag: 5000Å-1200Å-500Å-9 μ m
18. Sinter	410°C, 15 min, in forming gas
19. AR coating	500Å TiO _x , 820Å Al ₂ O ₃

Table 2. Simplified processing sequence of PESC concentrator cells.

STEP	PARAMETERS
1. Wafer selection	0.2 Ω -cm, (100), FZ, p-Si, 280 μ m thick, 3 inch Wacker wa
2. Phosphorus diffuse	Solid source, 930°C, 30 min, 15 $\Omega/\square$
3. Oxide growth	1000°C, 1 hr, in TCA, $\sim$ 1800Å SiO ₂
4. 1st masking, etch	Microgrooves on the active area
5. μ -Groove etching	KOH(8%, w/v), 70°C, 8 min
6. Oxide Removal	Buffered HF, 3 min
7. Oxide growth	1070°C, 5 hr, in TCA, $\sim$ 3000Å SiO ₂
8. 2nd masking, etch	Cell front junction, planar
9. Phosphorus diffuse	Solid source, 830°C, 20 min, 150 $\Omega/\square$
10. Back Al deposition	Vacuum evaporation, 1 μ m
11. Dry oxidation	950°C, O ₂ : 3 min, N ₂ : 3 hr, $\sim$ 100Å SiO ₂
12. 3rd masking, etch	Metallization
13. Top metallization	Ti-Pd-Ag: 1200Å-500Å-8 μ m
14. Lift off	Ultrasonic in acetone
15. Back metallization	Al-Ti-Pd-Ag: 5000Å-1200Å-500Å-9 μ m
16. Sinter	410°C, 15min, in forming gas
17. AR coating	500Å TiO _x , 820Å Al ₂ O ₃

The second modified process sequence includes the addition of a masking step immediately prior to the contact finger pattern definition. The purpose of this extra mask step is to open up a 3 micron wide slot in the oxide above the heavily doped N+ + region which will limit the contact-finger to silicon interface region to the active area. This reduces the risk of creating pinholes through the oxide in the busbar region during the oxide etch step. This oxide etch slot is then exposed and developed and the oxide is etched. The contact finger pattern is then exposed onto the remaining resist and developed using the baseline parameters. The process sequence is outlined in Table 3.

Table 3. Improved processing sequence of PESC concentrator cells.

STEP	PARAMETERS
1. Wafer selection	0.2 Ω -cm, (100), FZ, p-Si, 280 μ m thick, 3 inch Wacker wafer
2. Oxide growth	1000°C, 1 hr, in TCA, $\sim$ 1000Å SiO ₂
3. 1st masking	Microgrooves on the active area
4. μ -Groove etching	KOH(8%, w/v), 70°C, 8 min
5. Oxide Removal	Buffered HF, 3 min
6. Oxide growth	1070°C, 3 hr, in TCA, $\sim$ 3000Å SiO ₂
7. 2nd masking, etch	N ⁺⁺ region
8. Phosphorus diffuse	Solid source, 930°C, 30 min, 15 $\Omega/\square$
9. Oxide growth	1000°C, 70 min, in TCA, $\sim$ 1400Å SiO ₂
10. 3rd masking, etch	Cell front junction, planar
11. Phosphorus diffuse	Solid source, 830°C, 20 min, 150 $\Omega/\square$
12. Back Al deposition	Vacuum evaporation, 1 μ m
13. Dry oxidation	950°C, O ₂ : 3 min, N ₂ : 3 hr, $\sim$ 100Å SiO ₂
14. 4th masking, etch	Metal contact windows
15. 5th masking	Metallization
16. Top metallization	Ti-Pd-Ag: 1200Å-500Å-8 μ m
17. Lift off	Ultrasonic in acetone
18. Back metallization	Al-Ti-Pd-Ag: 5000Å-1200Å-500Å-5 μ m
19. Sinter	410°C, 15min, in forming gas
20. AR coating	500Å TiO _x , 820Å Al ₂ O ₃

3.0 Technology Transfer

Transfer of the PESC technology from UNSW to ASEC was accomplished with the assistance of UNSW personnel working side by side with ASEC personnel during the first seven months of the contract period. During this period, Dr. Jianhua Zhao and Aihua Wang provided the necessary modeling, documentation, and process detail to allow ASEC personnel to closely duplicate the process used at UNSW. Slight modifications to the UNSW process were made which allowed high volume production equipment and processes to be utilized for future mass production requirements.

3.1 Overall Transfer

The transfer of the PESC technology occurred in three phases. The first phase of the technology transfer involved device modeling and mask design which are discussed in detail in Section 4. The second phase of the transfer involved demonstration of the cell design and process by UNSW personnel using ASEC production equipment. This provided the necessary baseline 4-mask process demonstration for duplication by ASEC personnel. The third phase of the transfer involved demonstration of the four-mask process by ASEC personnel.

3.2 Adapted ASEC Processes

The PESC cell technology developed in the University of New South Wales is used for the concentrator cell design. The technology has demonstrated 25.2% efficiency on a 1.58-square-centimeter cell.

Figure 2 shows the newly designed cell in the current ASEC program. To achieve the highest possible concentration performance and lower system cost, the cell area is reduced to 1 square centimeter from 1.58 square centimeter used at UNSW. The metal finger spacing is 127 microns to fit the available prismatic cover design. The cell surface between

metal fingers is microgrooved to reduce the cell reflectance. The microgrooves also reduce the emitter lateral resistance by a factor of square root 3. An inverted-pyramid mask has also been designed for future experiments.

Figure 2: Top View of ASEC Silicon Concentrator Cell

To avoid problems in using plating to provide thick Ag contacts, (non-uniform metal thickness and disposal procedures for plating solutions), a single-step lift-off process was used to provide 8-micron-thick metalization. This metalization will also improve the solderability of the cells. As detailed above, the baseline process requires four lithographic masking steps.

A double-layer antireflection coating of TiO_x and Al_2O_3 is used to further reduce the surface reflection from the cells. The TiO_x and Al_2O_3 double-layer anti-reflection coating is more reliable than the ZnS and MgF_2 coating. It has better optical match for the adhesive and prismatic cover, which have a refractive index around 1.43. This coating is calculated to have a reflection 0.6% lower than cells with ZnS and MgF_2 coating after the cover is applied.

3.3 Yield Issues

The three process sequences shown in Tables 1, 2 and 3 showed that even the simplest process sequence (Table 2) needs to have high yields at each of several key steps to produce high overall yield.

In the first phase of the work, effort was directed at consolidating the various steps. Working at "pilot-level" rates, very high overall yields (over 90% overall for some lots) were obtained and these yields are promising for the next stages of the work. The discussion below indicates that there is still some improvement needed in the cell performance at high concentrations, but recent yields indicate that the masking sequence which gives best results can be completed with good yields.

3.4 Cost Issues

The cost reduction needed to meet the contract goals will depend largely on the process yields, when the processes are optimized for high concentration efficiency. At this stage, the throughput will be scaled-up, while maintaining good yields, and the separate process costs will be analyzed and reduced. Most starting wafers will have a 4 inch diameter, but 5-inch-diameter wafers will be evaluated later.

3.4.1 Other Factors

Two changes in the original specification for cost efficiency have made these goals more difficult.

3.4.2 Recalibration of Simulators

SANDIA's standard cells have been recalibrated and were set 4.8% lower than when the contract started. This means that higher cell efficiencies than originally assumed will be needed to achieve the cost goals.

3.4.3 Re-assessment of Prismatic Covers

Work completed at SANDIA showed that initial estimates of the effectiveness of prismatic covers were higher than achieved. Ten of the cells made at ASEC had prismatic covers applied by ENTECH. Three grid line widths (shading 18.4%, 14.5% and 8.2%) were included. Figure 3 shows the results with % Isc gain plotted versus % shading. The 100%, 75% and 50% gain lines are indicated. For these ten cells, the average Isc gain - to - shadow ratio was 67%. The percent gain in Isc ranged from 3.7% for the narrowest lines to 16% for the widest lines.

Figure 3. Plot of Percent Isc-Gain versus Percent Shading for Cells with Prismatic Covers

Although the contract may ultimately include use of prismatic covers; for the next phase, ASEC has collaborated with UNSW to re-optimize the grid pattern on the current cell design to provide highest output without benefit of the prismatic covers.

This also serves to reduce the efficiency available in the next phase, yet another conversion efficiency point below that used originally to establish the contract yield and cost data.

In the long term, if prismatic covers with greater effectiveness are available, the cell design can be suitably modified because the main change will be in the grid pattern design and formation.

Work in the next phase of the contract will adjust to these two modifications.

4.0 Cell Design

In this section, we describe results obtained from tests in which the starting cell design was modified. In a later section (6.0), we discuss work resulting from analyzing the experimental results.

4.1 Resistivity

There is an obvious trade-off in the choice of resistivity, based on results obtained in earlier UNSW work. High Voc can be obtained for low and medium resistivity ($<5 \Omega\text{-cm}$) and even increasing the resistivity to $100 \Omega\text{-cm}$ does not significantly reduce Voc. Voc is controlled predominantly by the quality of the surface passivation, and as a result, resistivity over a wide range can be used.

In the tests below, ASEC has equalled (or even slightly exceeded) Voc values obtained at UNSW for PESC cells and this is taken as confirmation that the passivation procedures used are satisfactory.

Jsc depends on several factors - the minority carrier lifetime after processing, and low reflectance resulting from surface texturing and good AR coatings. The carrier lifetime depends on the bulk and surface passivation, but is mostly determined by the quality of the starting silicon. Float zone refined silicon has shown higher lifetime than Czochralski-grown silicon. For either growth method, the dopant concentration (which determines the resistivity) can affect lifetime - lower doping (higher resistivity) gives higher Jsc.

The cell fill factor (Cff) when the cell is operating at high concentrations is determined mostly by the series resistance, and generally lower series resistance values are obtained with lower resistivity silicon.

Table 4 shows that insignificant differences in performance are observed at one-sun operation for slices from ingots with resistivity 0.15 and 0.2 ohm-cm. Overall, efficiencies are reduced by low Jsc, resulting from incomplete etching of the microgrooves, leaving a flat instead of a sharp edge. However at high concentrations, greater differences are seen, the lower resistivity giving slightly higher Cff.

Table 4 Cell Performance Data - Lot 36

Grid Width	.15 ohm-cm					.2 ohm-cm				
	Voc	Isc	Cff	Eff	n	Voc	Isc	Cff	Eff	n
2 micron	668.82	33.12	82.70	18.32	11	666.55	32.85	83.25	18.23	11
8 micron	665.19	31.70	82.19	17.33	12	662.95	31.42	82.29	17.16	10
16 micron	662.92	30.65	82.92	16.85	20	661.31	30.76	82.90	16.86	25
20 micron	660.73	29.87	83.33	16.45	19	659.38	30.09	83.25	16.52	24

n : Sample Size

Figure 4 shows calculated cell performance at different concentrations as a function of substrate resistivity. The cell area was 1 cm², the cell thickness 280μm, sheet resistance of the emitter = 100 ohm/□, gridlines spaced 127μm, 16μm wide and 9μm thick. For concentrations up to 200 suns, the 0.2 ohm-cm cells appear best, however for the required concentrations approaching 400 suns, slightly lower resistivities should be better.

Figure 4. Calculated Efficiencies of PESC Cells with Different Substrate Resistivities for 280 μ m thick cells.

In practice, it has been difficult to obtain good quality Si with resistivity around 0.1 ohm-cm, but as indicated above, 0.15 ohm-cm is promising.

4.2 Cell Area

As indicated in Figure 2, for this work the UNSW PESC design for high concentration was modified to give cell area = 1 cm². The reduced cell area gives 21 cells/3-inch wafer and 40 cells/4-inch wafer, a possible 30% reduction in manufacturing cost.

4.3 Grid Dimensions

The trade-off factors are: closer grid spacing reduces series resistance but increases shading; trade-off involves using narrower and fuller lines to maintain the required low series resistance. In 3.4.3, prismatic covering for different grid coverage was reported.

Several tests of performance for various gridline widths (and also for increased thickness) are presented in section 5.0.

5.0 Test Results

5.1 Group 4

Group 4 was the first group of concentrator cells tested at SANDIA. Four different grid finger widths were used as shown. Table 5 shows the one-sun performance for typical cells with different grid widths.

Table 5. The one-sun performance of the first lot of concentrator cells tested at Sandia under AM1.5 at 25°C.

Cell No	Voc (mV)	Jsc (mA/cm ²)	FF (%)	Eff (%)	Finger width (μm)
4841	659	34.61	83.4	19.03	2
4831	656.3	33.49	83.0	18.28	8
4621	656.0	31.14	83.5	17.10	16
4614	651.3	30.18	83.4	16.46	20

Jsc was slightly lower because of residual flats on the top of the grooves.

Figure 5 shows the good spectral response at both short and long wavelengths.

Figure 5. Spectral Response for Cell #4831 (Sandia Measurement)

The CFF values were high indicating good dark performance of the P/N junction. These cells had good performance at concentrations around 150X (Figure 6).

Figure 6. Efficiency Versus Concentration (Sandia Measurement)

The performance of this group with prismatic covers was given in 3.4.3.

5.2 Group 9

This group performed like Group 4 and the test results are presented in Table 6 along with results from groups 24, 25 (in section 5.3).

Table 6 One Sun Electrical Data

Lot No.	Cell No.	Voc (mV)	Jsc (ma/cm ²)	CFF (%)	EFF (%)	Finger Width (microns)
↑ 4 ↓	4841	659.0	34.61	83.4	19.03	2
	4831	656.3	33.49	83.0	18.28	8
	4621	656.0	31.14	83.5	17.10	16
	4614	651.3	30.18	83.4	16.46	20
↑ 9 ↓	9611	659.0	35.12	82.4	19.06	2
	9623	651.0	33.53	83.1	18.14	8
	9234	656.0	31.64	82.7	17.17	16
	9243	651.0	30.01	83.0	16.21	20
↑ 24 ↓	24913	667.0	35.7	83.8	19.92	2
	24923	662.0	34.0	83.8	18.87	8
	24534	659.0	31.8	83.6	17.53	16
	24542	658.0	30.7	83.7	16.93	20
↑ 25 ↓	25111	667.0	35.6	79.8	18.94	2
	25322	660.0	33.8	78.9	17.59	8
	25633	661.0	31.8	82.5	17.34	16
	25545	658.0	31.1	81.9	16.75	20

Note: Data based on new reference cell MK-25

5.3 Groups 24, 25

These lots also included four different gridline widths and the results are shown in Table 6.

The tested efficiencies (without prismatic covers) for Lot 25 cells with different grid widths is given in Figure 7. The peak efficiency is 21.8% at 50X. The Voc values in these groups are among the highest values measured for PESC cells.

**Figure 7. Achieved Efficiency (without prismatic covers)
for Cells With Different Gridline Widths for Lot No. 25.**

The fall off in efficiency at high concentrations in Figure 7 is the result of higher series resistance than expected. Figure 8 shows series resistance measurements for lots 24 and 25. These are measurements made from gridline to gridline, after isolating the grids from the busbar region. Also included in this figure are sample data from groups 4, 9 and 27, the latter discussed below.

Figure 8. Front Contact Series Resistance Measurements

Some cells from lot 27 were included in the front contact series resistance measurements reported in Figure 8 and showed reasonably low resistance.

One advantage to the five-mask process is the localized etching of the oxide prior to contact evaporation. This avoids exposing the busbar region to the etchant and minimizes pinhole formation in the oxide. The etch time can be extended to assure complete removal of the oxide, a factor in reducing series resistance.

The 5-mask process adds complexity and cost. However, the electrical yields for 5-mask lots 27, 32 was over 93%. This was at the expense of adding 4 minutes/wafer (0.25 minutes/cell) for small 10-wafer lots. In volume production, lot sizes 50-100 would be used, and would significantly reduce the labor costs for the added step. This area of cost tradeoff (high yield vs small added cost) will be explored further.

5.4 Test Results on Thinner Cells

Lot 25 included some cells made from starting silicon which had been thinned from 280 μ m to either 150 or 200 μ m. The mechanical yields were 17.5% (150 μ m) and 60% (200 μ m). Two 150 μ m cells and seven 200 μ m cells were tested at SANDIA.

Table 7 shows the one-sun test results.

Table 7 Cell Performance Data (One-Sun)
Lot 25

Thickness	n	Grid Type (μ m)	Voc (mV)	Isc (mA)	Cff (%)	Eff (%)
150 micron	2	2	655	33.2	80.2	17.4
200 micron	4	2	665	34.5	79.2	18.5
	3	8	658	32.3	78.3	16.7
	8	16	658	31.1	78.0	16.0
	5	20	655	29.4	79.3	15.2
280 micron	6	2	666	35.0	76.1	17.7
	4	8	662	33.0	78.2	17.3
	9	16	660	31.3	80.0	16.7
	6	20	659	30.0	81.0	16.0

The thinner cells had reduced performance and when the mechanical yield is considered, thin cells may not be cost effective.

The high concentration tests results on Lot 25 cells are shown in Figures 9 and 10.

Figure 9 Average Efficiency vs Thickness, Lot 25 Two Micron Grids

Figure 10 Average Efficiency vs Thickness, Lot 25, 8, 16, 20 Micron Grids

The thicker cells showed better performance. However, when the present series resistance problems are solved (possibly also using 5-mask processing), the thinner cells may show some advantages.

5.5 Groups 27, 32

These groups were made with the 5-mask process (Table 3) to determine if the more detailed process could improve the performance. Some 4-mask control wafers were included for comparison.

The 5-mask process adds an extra exposure/development step during the photolithography processing for the front contacts. This step opens up a narrow $3\mu\text{m}$ wide slot above the heavily doped N^{++} region which is confined inside the lightly diffused N^{+} region at the

sequence gave high yield of "good cells". For lot 27, 57 out of 64 cells reached electrical test, and 54 cells had Voc > 658mV, with good Jsc and CFF at one- sun. The control cells in lot 27 had low Voc and CFF probably caused by shunting at pinholes in the oxide.

Lot 32 was the second lot processed using a 5-mask process and was similar to lot 27. The one-sun test results are shown in Table 8.

**Table 8 Five Mask Process
Cell Performance Data Lots 27 and 32**

Grid Type (μm)	*n	Lot 27				*n	Lot 32			
		Voc (mV)	Isc (mA)	Cff (%)	Eff (%)		Voc (mV)	Isc (mA)	Cff (%)	Eff (%)
2	11	665	35.1	82.3	19.2	8	663	34.2	83.1	18.8
8	11	665	34.0	82.9	18.7	8	664	32.9	83.4	18.2
16	14	663	33.0	82.7	18.1	14	661	31.5	82.9	17.3
20	18	662	31.8	81.6	16.3	14	658	30.5	82.8	16.6

*n is the number of samples tested

5.6 Lot 36

A small lot (10 wafers) was processed using the 5-mask process sequence to compare the effect of Si of resistivity 0.15 and 0.2 ohm-cm. The cells were all processed together.

Table 9 shows the one-sun test results.

Table 9 Cell Performance Data - Lot 36

Grid Width	.15 Ohm-cm					.2 Ohm-cm				
	Voc	Isc	Cff	Eff	n	Voc	Isc	Cff	Eff	n
2 micron	668.82	33.12	82.70	18.32	11	666.55	32.85	83.25	18.23	11
8 micron	665.19	31.70	82.19	17.33	12	662.95	31.42	82.29	17.16	10
16 micron	662.92	30.65	82.92	16.85	20	661.31	30.76	82.90	16.86	25
20 micron	660.73	29.87	83.33	16.45	19	659.38	30.09	83.25	16.52	24

n : Sample Size

The efficiencies in each group are identical as expected for low concentration. The I_{sc} values are lower than previous run, because front surface reflectance was increased by the residual flat areas along the top of the microgrooves.

Sixteen 0.15 ohm-cm cells and four 0.2 ohm-cm cells were tested at high concentrations at SANDIA. The results are shown in Figures 11 and 12. Note that Figure 11 contains grid finger widths 2 μm and 16 μm ; Figure 12 contains 8 μm and 20 μm finger widths.

The results were not as expected. The 2 μm and 8 μm grid widths gave similar results for both resistivities. For the wider grids, the 0.2 ohm-cm cells had higher peak efficiency, at higher concentrations, and in addition, fell-off significantly less as the concentration increased. This behavior probably resulted from differences in series resistance, but the slight different in resistivity (and the revised dependence of series resistance on resistivity) could not account for the differences observed.

**Figure 11. Efficiency vs. Concentration
(Different Resistivities, Grid Width)**

**Figure 12 Efficiency vs. Concentration
(Different Resistivities, Grid Width)**

5.7 Overall Comments

In this period, progress has been made in establishing the processes in a production setting. Several minor (and correctable) problems (flat areas on microgrooves, reduced minority carrier lifetime, etc.) were found.

The surface passivation processing has been most effective.

Good efficiency values have been achieved. However, the efficiencies at high concentration levels are low. The major cause is high series resistance and more discussion is given in Section 6.0 of the tests to determine the sources of the increased resistance.

The adjustment to the "increased" goal efficiencies (assume no prismatic cover, decreased standard simulator setting) is promising. In the next phase, the prismatic cover option will be re-assessed because of the severe tradeoffs required to ensure high efficiency at high concentrations, approaching 400 suns.

Sufficient understanding has been gained of the subtleties of the various process steps to predict achievable efficiencies at high concentrations. These efficiency values can be used to define the yield and cost issues.

6.0 Development Issues

6.1 Analysis of Series Resistance

The major problem is obtaining high efficiency at high concentrations. Above it was observed that series resistance must be reduced to very low values. A simple calculation shows that at 350 suns, the matched load resistance is around 60 milliohms; a series resistance of 6 milliohms causes about 10% loss in CFF. These very low values of series resistance make it difficult to isolate the sources of parasitic resistance.

The two major resistive losses are in the front contacts. The first loss involves the gridline resistance which is usually a function of the gridline spacing, the gridline width, and the thickness of metal deposited. The second loss is contact resistance, particularly when the metal to diffused layer contact area is seriously restricted, to reduce the recombination current generated at the metal-Si contacts.

The next few sections describe some tests intended to identify these resistive losses.

6.1.1 Tests of Heavily Doped N++ Layer

In the phosphorus diffusion process used to form the n++ region, the time at 930°C was increased from 30 to 40 minutes. This reduced the sheet resistance from 12 ohms/square to 8 ohms/square. The emitter depth increased from 1.2 μ m to 1.3 μ m.

Table 10 shows the one-sun I-V data for groups of cells diffused for 30 minutes (control group) and for 40 minutes (experimental group).

Table 10 One-Sun I-V Data for Different Diffusion Time

	Control Group Sample Size: 14 Cells				Experimental Group Sample Size: 14 Cells			
	Voc	Isc	Cff	Eff	Voc	Isc	Cff	Eff
Average	657.1	30.8	83.2	16.8	658.2	31.3	83.6	17.2
Standard Deviation	4.5	1.2	0.85	0.83	2.9	0.67	0.16	0.44

The average values for the I-V parameters were similar, but the standard deviation is reduced for the slightly deeper emitter group, in particular for the CFF values. These

results led to a test matrix to optimize emitter diffusion. Table 11 shows the details of this matrix. The cells made in this matrix will be tested at one-sun and also at high concentrations.

**Table 11 Solid Source Phosphorus Diffusion
Optimization Test Plan
930°C**

Time (Minutes)	10	20	Baseline 30	40	50	60
Sheet Resistance (Ohms/Square) (Target)	17	15	12	9	8	7
Junction Depth (Target)	0.9	1.1	1.2	1.3	1.35	1.4
Sample Size (Wafers) (Cells)	2 32	2 32	2 32	2 32	2 32	2 32

6.1.2 Measurement of Contact Resistance

Figure 8 (in Section 5.3) showed the results obtained when resistance values between successive grid lines was tested for several lots, after isolating the grids from the busbar.

In Figure 8, the slope gives the emitter sheet resistance and the intercept (extrapolated to line 0) is a measure of the contact resistance.

Note: These measurements give qualitative results, and the resistance values correlate with the cell performance at high concentrations. In Section 8, in the work planned, we describe the use of resistance test patterns.

6.1.3 Variations in Grid Line Dimensions

6.1.3.1 Width

In Sections 5.2 and 5.3, the effect of various gridline widths on cell performance was discussed.

6.1.3.2 Thickness

Normally gridline thicknesses around $7\mu\text{m}$ were used. Some tests were made of a double photoresist process to provide thicker gridlines with a rectangular profile rather than a trapezoidal profile.

These tests were promising (gridline thickness up to $10\mu\text{m}$) and will be continued. In Section 8, plans for image reversal tests are presented.

6.1.4 Processing Effects on Contact Resistance

Section 6.1.1 described a test to vary the emitter sheet resistance. Also the procedures used to stabilize the solid sources will be optimized. In Section 5.5, it was noted that the 5-mask process improves the chance that thin residual oxide layers are fully removed in the contact slots.

6.1.5 Back Contact Resistance Measurements

Most of the resistance sources are traced to the front contacts. However, some tests of the resistance between pads formed in the back contacts showed the back contact resistance could be reduced.

The non-uniform values obtained from pads formed at different areas of the back contact suggested that, as was the case for the front contacts, the diffusion processes and the back surface cleaning procedures could be improved.

The measured back contact resistance values decreased when successive sintering cycles (at 600°C) were used.

In Section 8.0, the use of series resistance test patterns for the back surface is proposed.

7.0 Mounting & Environmental Tests

These tests were preliminary, but indicate that the array performance of these cells is promising.

7.1 Solder Tests

Solder screens were designed and used to print front and rear patterns on cells before the dicing process.

Some cells with screen printed, melted and reformed solder patterns were sent to SANDIA.

7.2 Ultraviolet Exposure

SANDIA exposed several typical ASEC cells to UV radiation. No noticeable degradation was observed. It can be projected that the surface passivation oxides produced at ASEC on PESC-design cells should not be unstable under prolonged exposure to concentrated sunlight.

8.0 Work Planned

The first phase has demonstrated effective technology transfer. Most current process steps can be performed effectively using low-cost, high-throughput methods.

Several areas have been identified to provide cost effective optimization of efficiency, and effort is now directed towards yield improvement and cost reduction.

The technical tasks planned are well suited to use of design-of-experiments approaches and these will be used.

The main areas for Phase 2 include:

8.1 Optimized Diffusion Procedures

For front and back contacts, optimum doping and surface preparation procedures will be found for the N++ or P++ region for metal contacts.

8.2 Optimized Process Sequence

The tradeoff between complexity (number of masks) and high yield will be resolved.

8.3 Improved Process Monitoring

In-line process checks are planned.

8.3.1 Resistance Test Patterns

Contact resistance patterns (which provide data on both sheet resistance and contact resistance) will be included at the edges of the photomask used for the front contact

patterning and also on the back contact. The test pads in the patterns will undergo the same process sequence as the main contacts and the resistance can be sampled before and after sintering.

8.3.2 Minority Carrier Lifetime Monitoring

In addition to an evaluation of alternate sources of high quality silicon, ASEC plans to install a contactless minority carrier lifetime tester. Two pieces of equipment were available, one from SEMITEX (Lifetime 88) and the other from MAREUBLENI (Leo Giken). The former is more readily available. However, the Leo Giken equipment has been used by both UNSW and SANDIA. SANDIA has made significant improvements in the Leo Giken method and these advances can be incorporated, by choice of suitable modules, or by addition of hardware items. ASEC prefers to use the Leo Giken equipment, to facilitate correlation with SANDIA and UNSW.

8.3.3 Evaluation of Alternate Si Suppliers

ASEC will test other sources of Si which can meet the contract goals. Five-inch and four-inch ingots will be used.

8.4 Design for No Prismatic Cover

UNSW has already provided an updated analysis of a grid pattern which will provide high efficiency without recourse to a prismatic cover. This design will be implemented in Phase 2.

8.5 Prismatic Cover

ASEC is considering re-evaluation of prismatic covers using current standard covers and application methods. In addition, ASEC would assess the chance of providing improved covers. The efforts in 8.4 and 8.5 will be included in updated cost estimates.

8.6 Gridline Formation

Image reversal methods will be evaluated. If possible, one of ASEC's engineers will visit SANDIA's Photovoltaic Device Fabrication Laboratory to observe their current technology.

8.7 Yield Improvement

More intensive lot control will be included as the process methods become more "fixed".

8.8 Cost Estimates

With the narrowing down of the process steps, it is possible to obtain input for ASEC's cost model. Quantitative sensitivity studies can now be made to determine process performance trade offs.

In Phase 2, increased effort will be placed on the cost goals.

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