Development of Large-Area Monolithically Integrated Silicon- FilmTM Photovoltaic Modules

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Abstract

The objective of this program is to develop Silicon-Film™ Product III into a low-cost, stable solar cell for large-scale terrestrial power applications. The Product III structure is a thin ($<100\mu\text{m}$) polycrystalline layer of silicon on a durable, insulating, ceramic substrate. The insulating substrate allows the silicon layer to be isolated and metallized to form a monolithically interconnected array of solar cells. High efficiency is achievable with the use of light trapping and a passivated back surface. The long term goal for the product is a 1200 cm^2 , 18% efficient solar cell array.

During the past year, material quality has improved throughout the use of new metallurgical barrier technologies. The barrier is essential preventing impurity interaction between the silicon film and the low-cost substrate. Minority carrier diffusion lengths have improved from $5 - 7\text{ }\mu\text{m}$ to $45\text{ }\mu\text{m}$ by the use of the new metallurgical barrier layer. Also, control of the PV layer thickness has improved with the incorporation of the barrier layer. The barrier technology has made a reduction in film thickness from $100\text{ }\mu\text{m}$ to $50\text{ }\mu\text{m}$ possible. Also, during the Phase III program a new filament-based fabric substrate material was investigated. Efficiencies over 10% were achieved on 1.0 cm^2 devices made on these substrates.

The Phase III program also demonstrated the monolithic fabrication sequence by the fabrication of a prototype array using the device processing sequences developed during the Phase II program. Arrays of with 15 array elements have been fabricated on 50 cm^2 silicon films. A 12 cm^2 , 7-element, monolithically-interconnected sub-array was fabricated with an open circuit voltage of 3.9 volts (561 mV/element), short circuit current of 35.2 mA, fill factor of 0.63 and an overall efficiency of 7.3%.

Figure 1. *Silicon-Film™ Product III device structure.*

1. Introduction

The key advancement of the Phase III program was the invention of a new, conformal metallurgical barrier technology. The barrier has benefited this program by allowing:

- an improvement in the minority carrier diffusion length from less than 10 μm to 45 μm , and
- a reduction in the minimum silicon layer thickness from greater than 100 μm to 50 μm .

The new barrier technology has exhibited excellent wetting properties and good survivability during the Silicon-Film™ growth process. Also, the barrier layer has the potential to provide back surface reflection and texturing and electrical conduction to the substrate. During the past year, we have investigated a number of techniques for the deposition of the conformal metallurgical barrier, however the technology is still far from being optimized. The key issue is how well the barrier prevents impurities from the ceramic substrate from contaminating the PV layer.

The Phase III program investigated a new substrate material on filament-based fabrics. 10.7% efficient, 1.0 cm^2 devices have been verified at the National Renewable Energy Laboratory. This substrate was introduced during the Phase III program and will be included during the Phase IV effort.

The Phase III program also demonstrated the monolithic fabrication sequence by constructing a prototype array using the device processing sequences developed during the Phase II program. Arrays with 15 array elements have been fabricated on 50 cm^2 silicon films. A 12 cm^2 , 7-element, monolithically-interconnected sub-array was fabricated with an open circuit voltage of 3.9 volts (561 mV/element), short circuit current of 35.2 mA, fill factor of 0.63 and an overall efficiency of 7.3%.

This report will review progress in the development of the Product III device, including the conformal barrier layer, ceramic and alternate substrates, thin (50 μm) PV layers, and fully interconnected array devices.

1.1 Materials Development - Metallurgical Barrier Layer

Material quality has been the key issue in the development of Product III for the last year. During the Phase III program, a considerable amount of effort was devoted to understanding the major factors limiting the performance of silicon-on-ceramic devices. Minority carrier diffusion

lengths had been limited to 5 - 7 μm despite all efforts to improve the material by processing enhancements such as diffusion gettering or hydrogenation.

A variety of analytical techniques were applied in order to determine which major factor was limiting material quality. A number of chemical techniques, including EDS (energy dispersion spectroscopy) and ICP-MS (inductively-coupled plasma - mass spectroscopy), and a number of electrical/optical techniques, including EPD (etch pit density) counting, EBIC (electron beam induced current) and LBIC (light beam induced current) were applied during the Phase II effort. The conclusions of the Phase II program were that the ceramic substrate was a major source of metallic impurities and these impurities were being introduced into the PV layer during the growth process. The Phase II annual report contains more details of this investigation.

The Phase III effort focused on methods of reducing the ceramic-silicon layer impurity interaction. Two approaches were developed in order to prevent contamination of the PV layer. The first involved selecting expensive, high-purity materials for the ceramic fabrication process. This approach met with little success. Films grown on these ceramics showed no improvement in minority carrier diffusion length. The second approach involved the development of a barrier layer between the ceramic and silicon PV layer. The key issues for the selection of a metallurgical barrier include:

- good wettability of the silicon film during the growth process,
- good survivability of the barrier during the growth process,
- low contamination of the PV layer by the barrier materials,
- good electrical conduction through the barrier layer,
- good electrical passivation provided by the barrier layer, and
- good optical reflectivity and scattering by texturing.

The Phase III program investigated a number of materials and deposition techniques for the formation of the barrier layer. One approach utilized high purity dielectric materials. The dielectric, in powder form, was dispersed in a colloidal solution, then sprayed (atomized) onto the ceramic substrate at 100°C (substrate temperature). The substrate was fired at over 1000°C in an argon atmosphere and is then ready for silicon growth. Barriers fabricated by this technique are typically 35 - 45 μm thick after being fired (see **Figure 2**). This barrier technique yields a barrier that is compatible with the insulating substrate and is suitable for the fabrication of the Product III device.

Figure 2. *Cross-sectional photomicrograph of a colloidal-sprayed metallurgical barrier. Wetting to these types of barriers is not reproducible.*

One of the major difficulties in selecting a barrier material for colloidal-spray deposition is finding one that allows wetting of the silicon during the growth process. Typically, dielectric materials, which consist primarily of metal oxides and nitrides, are difficult to wet with molten metal solutions. Although we were able to fabricate devices on these barrier layers, wetting has not been reproducible and depends on factors such as powder particle size and surface texturing.

A second barrier approach, which was discovered during the Phase III program, is radically different compared to the colloidal-spray deposition method. This barrier exhibits many of the properties missing in the dielectric powder-based layer, such as good wettability and survivability. During the Phase III effort, we investigated an number of growth and deposition techniques based on this new technology.

The new, conformal barrier has been beneficial in greatly reducing the physical interaction between the ceramic and the silicon PV layer. **Figure 3(a)** shows the silicon-ceramic interface for a structure formed without a barrier layer. Note that a high level of interaction between the ceramic and silicon has taken place. **Figure 3(b)** shows a similar silicon-ceramic interface with a barrier layer present. Note the clear delineation between the silicon film region and the porous ceramic. This photomicrograph illustrates our early development work with this type of barrier layer. This particular barrier resulted in an increase in the diffusion length from 5 - 7 μm to over 20 μm .

(b)

(a)

Figure 3. *Silicon-ceramic interaction (a) without a conformal barrier layer and (b) with a conformal barrier layer. Note the lack of interaction between the silicon and ceramic in (b).*

Subsequent work improved the minority carrier diffusion length substantially. In all of the work, a correlation was observed between how effective the barrier was at preventing physical interaction of the silicon with the barrier and the material quality as measured by minority carrier diffusion length. Diffusion lengths as high as 45 μm have been measured on samples that exhibited a clear delineation between the silicon PV layer and the ceramic substrate. A quantum efficiency curve (see **Figure 4**) illustrates the improvement in film quality.

Figure 4. *QE curves of a typical cell fabricated before and after the conformal barrier process was discovered.*

Single crystal substrates are currently being used to further develop the metallurgical barrier process. The silicon substrate eliminates any possibility of contamination being caused by a ceramic substrate. Barrier layers deposited onto single crystal substrates are being analyzed for their survivability in the Silicon-Film™ process, and as to whether the barrier itself will contaminate the silicon PV layer. **Figure 5** illustrates a barrier layer deposited on a single crystal substrate which has survived the growth of a silicon PV layer. **Figure 6** shows a barrier layer deposited by a different technique which has been destroyed by the silicon PV layer growth process. The extent of contamination is not clear at this point, however, the electrical quality of the PV layers grown on conformal barriers will be extensively studied during the Phase IV program.

Figure 5. *A metallurgical barrier on a single crystal substrate which has survived the Silicon-FilmTM process.*

Figure 6. *Barrier destroyed by the PV layer growth process.*

1.2 Materials Development -- Ceramic Development

The ceramic technology has remained basically unchanged from the Phase II technology. Several attempts were made to upgrade the purity of the ceramic by utilizing more pure materials, however this approach met with little success. The present ceramic process is summarized below.

The ceramic is fabricated from low-cost materials using conventional ceramic fabrication methods. Ceramic powders of the appropriate size and purity are batch mixed with a water-based organic binder, then sieved to remove agglomerates. The resulting slurry is then tape-cast onto polyethylene coated aluminum setters using a laboratory scale tape casting unit with an adjustable doctor blade assembly. Tape casting is a continuous process which is currently being done at the rate of 30 cm/min based on the viscosity of the slurry. The tape cast substrates are dried in air at 100°C to remove volatile materials, and then delaminated. The dried substrates, which are 45 cm x 13 cm x 0.12 cm thick, are then trimmed and cut to the appropriate size. Ceramic substrates up to 582 cm² have been fabricated with existing equipment.

The sintering process is done in an electric furnace that utilizes silicon carbide heating elements in an argon atmosphere. In the first stage of the furnace binder burn-out occurs at 850°C, and in the second stage sintering occurs at over 1200°C. Ceramic thickness is reduced by 40% due to shrinkage during firing; linear and cross dimensional shrinkage are negligible. The sintering process is a unique step that we are able to suitably densify our ceramic very rapidly. The sample moves through the furnace, which is 160 cm long, on a refractory setter at a rate of 15 cm/min. We are able to sinter at this rate because of the combination of materials used, and the fact that we do not need to achieve mass densities comparable to conventionally fired ceramics.

Ceramic resistivity can be controlled by varying the composition of the ceramic, without sacrificing any of the mechanical strength. Resistivity of the Product II substrate is designed to be 0.5 to 2.0 Ωcm to provide back surface conduction for that single junction device. Resistivity, flatness, and mechanical strength of the ceramic substrate are critical issues for the monolithic integration process. With a suitable variation in the composition, Product III substrates can be reproducibly fabricated with resistivities over 50KΩcm, resulting in a base-to-base shunt resistance through the ceramic of over 10 kΩ. Flatness is required for the photolithography and dicing in the present laboratory scale process. Mechanical strength of the ceramic is important to assure the durability of the finished array. These issues were resolved during the Phase II program.

1.3 Materials Development -- Alternate Substrates

The silicon-on-ceramic growth process has been extended to fabric substrates. Devices are fabricated by growing thin silicon layers directly on high temperature fabric substrates (see

Figure 7). The use of a filament-based fabric substrate offers the possibility of direct silicon growth to a readily available substrate material. It also offers a method of silicon layer evaluation independent of the ceramic and barrier layer. The initial fabrics investigated were relatively high cost (\$70 /m²), however recent efforts have shown that high cost fabrics may not be required to support the growth of high quality silicon films.

The fabric-based effort was initiated in 1990 in an effort to fabricate lightweight arrays. That work expanded to investigate low-cost versions for terrestrial applications. Some initial efforts took place in Phase III. Investigation of low cost fabric substrates has been incorporated into the Phase IV of this contract. The work plan focuses on the demonstration of lightweight, high-efficiency solar cells.

Figure 7. *Schematic of the proposed device. The structure is based on a filament based fabric. The silicon is grown on the fabric in a high temperature process, then a conventional solar cell structure is fabricated.*

Thin silicon films on lightweight fabric substrates offer many commercial and military applications. Powering lightweight unmanned planes is one application of the proposed solar cells in both commercial and military sectors. Lightweight arrays can also be used to power infantry telecommunications. Commercial applications for lightweight arrays grows daily. These include remote power, where equipment has to be carried or flown in, and powering vehicles of all types.

Figure 8. *Cross section of a silicon-on-fabric structure.*

Progress with the use of low-cost fabrics (\$17.5/m²) has indicated that direct competition with conventional crystalline silicon wafer fabrication processes are possible. This would make this new product a contender for all terrestrial PV applications including utility scale power.

Once basic material issues were settled, solar cell conversion efficiency has steadily increased. **Figure 9** indicates how the program has been successful in increasing conversion efficiency. The data in **Figure 9** is for 1.0 cm² cells, tested under 1000 mW/cm², AM1.5G spectrum at 25°C. The testing laboratory is indicated for each test (either Sandia National Laboratory, or the National Renewable Energy Laboratory). Considerable increases in efficiency are expected through solar cell device optimization. Increases in material quality are expected as well, which will lead to further efficiency enhancements.

Figure 9. *Solar cell conversion efficiency increases over the program life to date.*

The dependence on high purity material initiated an investigation into a preliminary cleaning process. This cleaning process was developed and utilized for the substrates that later became the solar cells tested in October 1993. These cells used a fiber substrate that earlier was found to be too impure to support high quality material. It has not yet been determined to what extent the cleaning process will be able to purify material, or how loose the purity specification on the fiber can be, however all reductions in purity specification will result in a lower cost product. Presently, all existing fabric manufacturers are fabricating material for applications very unlike the one being pursued here. It is expected that further refinements in the specification need for this application will result reduced fabric cost.

This program has demonstrated that solar cell conversion efficiencies over 10% can be achieved with silicon grown on a filament-based fabric substrate. The efficiency potential of this material approaches 15% in an optimized device structure. The path to a low-cost device has been developed through the use of low-cost substrate materials and thin layers of silicon. The applicability of this technology to the utility-scale PV applications will be further investigated in Phase IV of this contract.

2. Silicon Layer Growth Development

Near the end of the Phase III program, we began a development effort designed to achieve thin (50 μm) films grown at high sheet speeds over large areas. Equipment previously used to generate Product I material was modified for the growth of thin silicon films which incorporate a metallurgical barrier layer. The new, conformal barrier has been a significant

factor allowing 50 μm films with long elongated grains to be grown. Work on high-speed, large-area silicon layers will require significant effort during the Phase IV program.

2.1 High-Speed Film Growth

The controlled growth of crystalline silicon from a liquid generally requires the following conditions:

1. relatively pure starting material,
2. a technique for seeding,
3. temperature gradient in liquid at interface approaches zero.

The absence of any of these conditions will result in polycrystalline and/or dendritic growth. All low cost silicon substrate approaches are presumed to start with material suitably pure to avoid the growth defects due to constitutional supercooling. Other than the dendritic web process the low cost substrate approaches generally do not employ a preferential seeding procedure. As a consequence these substrates are polycrystalline.

The temperature gradient in the liquid at the interface determines the rate at which the silicon growth front proceeds (growth speed). If the temperature gradient is negative in the liquid (heat flow from interface to liquid), then the conditions for supercooling exist and dendritic growth occurs. If the temperature gradient in the liquid at the interface is positive (heat flow from liquid to the interface), then the growth speed is diminished from its maximum.

The maximum growth occurs when the only heat to be removed from the liquid-solid interface is the heat of solidification, and is determined by the details of heat transfer in the grown solid. Ciszek [CISZEK, 1976] has calculated this maximum growth velocity for silicon growth by CZ and for conventional sheet technologies. He calculates a velocity of 0.5 cm/min for a 13 cm diameter cylindrical CZ growth, 6.7 cm/min for a 500 micron thick silicon sheet, and 10.4 cm/min for a 200 micron thick silicon sheet. Observed maximum nondendritic growth rates are approximately 30% of the calculated values [CISZEK and SCHWUTKE, 1975]. Thus, for CZ growth the observed maximum is in the range of 0.17 cm/min. The configuration of heat removal for the silicon brick technologies [GESSERT *et al.*, 1985] is similar, and comparable maximum growth speed are observed. However, this latter approach generates polycrystalline material since no preferential seeding is employed. For the conventional sheet technologies the observed maximum is in the range of 2 to 3 cm/min.

For the conventional sheet technologies [HOPKINS, 1987; ETTOUNEY and KALEJS, 1987; GURTLE, 1980] to achieve these maximum growth rates it is necessary to employ very steep temperature gradients in the solid at the liquid-solid interface. The presence of these temperature gradients can lead to the introduction of thermal-induced stresses [CHALMERS, 1985]. In the

extreme, these stresses can lead to sheet deformation [DILLON and TSAI, 1987], making solar cell fabrication untenable. Even in the absence of deformation, stress induced structural defects, most notably dislocations, lead to a diminution of the electrical properties necessary for the efficient operation of a photovoltaic device. As a consequence, a great deal of attention has been expended by these conventional sheet technologies to accomplish temperature profiles which simultaneously assure maximum growth rate and minimum stress introduction.

(a)

(b)

Figure 10. Schematic of growth habit for (a) conventional sheet processes, and (b) the high areal throughput sheet processes.

A further consequence of the process employed by conventional sheet technologies is growth habit. The surface of these grown materials are typically characterized by elongated grains as illustrated in **Figure 10(a)**. These grains can be many millimeters wide, and several centimeters long. The direction of the long dimension of these grains is coincident with the direction of sheet motion. For these processes the direction of growth is collinear with the pulling direction; and the growth speed is equal to the pulling speed.

A drawback to the conventional sheet technologies is the solar cell areal generation rate. The areal generation rate (dA/dt) is proportional to the product of the growth velocity (dx/dt) and area of the liquid-solid interface (represented as w times l , where w and l are the width and length of the liquid-solid interface area, respectively), and inversely proportional to the effective thickness (s) of the solar cell as given in equation (1).

$$\frac{dA}{dt} = \frac{wl}{s} \frac{dx}{dt} \quad (1)$$

For example, for a sheet technology with $w = 10$ cm, $s = 1$, and $dx/dt = 2.5$ cm/min (corresponding to a thickness, s , of 0.03 cm), the solar cell areal generation rate is 25 cm²/min. For comparison, a polycrystalline silicon brick growth process with $w = l = 10$ cm, $s = 0.08$ cm (s is equal to 0.04 cm of actual thickness, and 0.04 cm worth of kerf loss due to sawing) and $dx/dt = 0.17$ cm/min, achieves a solar cell areal generation rate of 210 cm²/min. Thus, in this comparison of machines generating 10 cm wide material for solar cells, the sheet technology machine utilizes 62.5% less silicon per solar cell, but generates solar cells at one eighth the production rate. Clearly, the material utilization savings in silicon is worthwhile, and the elimination of the costly sawing of large silicon areas per wafer is a major benefit, however, there is a rather severe penalty in areal throughput that can be expected.

There is a path to improving the areal throughput for sheet material; **Figure 11** illustrates the essential features of the approach. The approach is to de-couple the growth speed from the sheet pulling speed. In this figure the terms dx/dt , l , w and s are as defined above and V_p is the sheet pulling velocity. The sheet pulling speed is related to growth speed according to equation (2).

$$V_p = \frac{1}{s} \frac{dx}{dt} \quad (2)$$

By substituting equation (2) into (1) it is seen that the areal generation rate for a sheet process operating in this mode is just the product of the pulling speed and sheet width, w . For example, a 20 cm wide sheet pulled at 50 cm/min would yield 1000 cm²/min. Thus, with this approach, the silicon utilization is greatly improved, the costly and cumbersome sawing of large areas of silicon per wafer is eliminated, and the areal generation per machine is much greater than the ingot/brick technologies.

Figure 11. *Diagram of a high areal throughput sheet growth process.*

There are three significant features about the higher speed (>10 cm/min) approaches. First, these materials are comprised of columnar grains (typically in the size range of 100 to 1000 microns) as generically illustrated in **Figure 10(b)**. Generally, the grains sizes are comparable to the sheet thickness. Second, in all the higher speed approaches the heat of solidification is removed in a direction nominally perpendicular to the plane of the growing sheet, and the actual growth rates are reduced. Consequently, the thermal stress-induced material defects seen in conventional sheet technologies employing the very large temperature gradients necessary to achieve practical growth rates, are greatly reduced. Third, the observed effective minority carrier diffusion lengths do not seem to be limited by the grain size. It is expected that this approach to the recrystallization of the deposited silicon layer is compatible with manufacturing processes achieving areal production rates in excess of $1000 \text{ cm}^2/\text{min}$.

2.2 Film Thickness Control

The Silicon-Film™ growth process has been limited to a minimum film thickness of $100 \mu\text{m}$. This has been primarily due to difficulty in controlling amount of interaction between the ceramic and the silicon. Without a barrier layer a large amount of the silicon grown can be "soaked" into the ceramic. The amount of soaking is not controllable. To prevent the PV layer from being too thin or completely soaking into the ceramic, a thicker silicon layer has been necessary. The new, conformal barrier process is a key element in solving this problem. The conformal barrier prevents a large degree interaction without preventing wetting of the silicon layer to the substrate during the growth process. This has allowed an improvement in the control of the thickness of the PV layer.

Figure 12. 50 micron silicon layer grown on a conformal barrier layer (100X).

With the new conformal barrier technology, we have been able to achieve 50 μm films over small area. **Figure 12** depicts a 50 μm film of silicon grown onto the conformal barrier which has been deposited on a single crystal silicon wafer. This work was initiated near the end of the Phase III program and will be continued during the Phase IV program.

3. Device Development

3.1 Device Fabrication

The Product III structure has a high potential for significant optical and electrical losses due to grid shading, isolation groove kerf loss, and series resistance losses from lateral current flow. The Phase II program developed a mathematical model of the significant loss mechanisms. The model accounted for the physical parameters of the solar cells (i.e. base and emitter sheet resistivities, grid line widths and thicknesses, etc.), as well as the array configuration (i.e. the inclusion or exclusion of emitter or base grid lines). Optimization led to an array design that utilized 100 μm wide emitter grids spaced 0.33 cm apart and 400 μm bus lines spaced 0.6 cm apart. A photolithography mask set was made, and this design was used for all device processing during the Phase III

The Product III fabrication sequence utilizes standard fabrication sequences, with the exception of the base contact formation, the array element isolation process and the array re-interconnection step. The Product III fabrication sequence is shown in **Figure 13**. This sequence was used for device fabrication during the Phase III program.

The as-grown samples were prepared for diffusion using standard silicon chemical cleaning sequences. The emitter was diffused to a sheet resistivity of 15 - 20 ohm/sq., and a weak HF:HNO₃ (1:100) etch was used to thin the emitter so that the final sheet resistivity was 40 ohm/sq. The diffusion sequence is designed to getter impurities from the silicon layer. After surface preparation and diffusion, the base layer was exposed in a stripe pattern by using photolithography (**Figure 13a**). This process allowed the base contact to be made to the base layer from the top of the device. Photolithography, evaporation and metal liftoff were used to define the contact pattern, with the base bus line aligned in the etched stripes and the emitter grid lines perpendicular to the base grid lines (**Figure 13b**). The sample was then diced to isolate the individual array elements, and mechanical saw damage was removed with a Freon-based plasma etch (**Figure 13c**). Finally, the re-interconnection metallization was applied to connect the cells as a series-connected array (**Figure 13d**). In some cases an additional dicing step was required to isolate the base contact from the adjacent emitter and emitter contacts.

The details of the key fabrication steps are described in more detail in the 1992 annual report.

Figure 13. Product III device fabrication sequence: (a) surface preparation, diffusion and base contact area definition, (b) contact metal evaporation and liftoff, (c) cell isolation, and (d) re-interconnection.

3.3 Device Results

This sequence was used in the fabrication of a 12 cm², 7-element, monolithically-interconnected sub-array was fabricated. The device had an open circuit voltage of 3.9 volts (561 mV/element), short circuit current of 35.2 mA, fill factor of 0.63 and an overall efficiency of 7.3%. An I-V curve of this cell is shown in **Figure 14**. The device is pictured in **Figure 15**.

Figure 14. *I-V curve of a 7-element Silicon-Film™ on ceramic sub-module.*

Figure 15. *Photomicrograph of a completed 9-element array showing emitter grid pattern (vertical) and bus bars (horizontal). This array consists of 9 elements connected in series. The open circuit voltage of this device is 4.84 volts.*

4. Conclusions

The significant advancement of the Phase III program was the invention of a new, conformal metallurgical barrier process. The process has dramatically improved the quality of the silicon PV layers. Minority carrier diffusion lengths have improved from 5 - 7 μm to 45 μm by the use of the barrier layer. The barrier has also enabled much thinner silicon layers to be grown. The barrier exhibits the characteristics necessary to grow thin films: good wettability and survivability during the Silicon-Film™ process, and no interaction between the ceramic and silicon layer. Films as thin as 50 μm have been demonstrated.

The Phase III program also investigated the growth of silicon films on filament-based fabric substrates. 10.7% efficient, 1.0 cm^2 devices were demonstrated. The feasibility of the monolithically interconnected solar cell array was demonstrated. A 7-element array was fabricated with an open circuit voltage of 3.9 volts (561 mV per array element). The array had a fill factor of 0.63 and an efficiency of 7.3% (AM1.5G).

The Phase IV will continue to develop the new, conformal barrier with the objective of improving the electrical quality of the layer, as well as improve the thickness control of the growth process. We also plan to further develop the speed and area capabilities of the growth equipment to achieve 100 cm^2 samples.

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