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An RS-170 to 700 frame per second CCD camera

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ABSTRACT

A versatile new camera, the Los Alamos National Laboratory (LANL) model GY6, is described. It operates at a wide variety of frame rates, from RS-170 to 700 frames per second. The camera operates as an NTSC compatible black and white camera when operating at RS-170 rates. When used for variable high-frame rates, a simple substitution is made of the RS-170 sync/clock generator circuit card with a high speed emitter-coupled logic (ECL) circuit card.

1. INTRODUCTION

The LANL model GY6 camera and its predecessor the GY5 camera were designed to explore the speed limits of the Loral Fairchild CCD222 area sensor. The CCD222 is organized into 380 pixels horizontally by 244 rows (when operated noninterlaced), with a single readout port. Although designed for RS-170 operation, the CCD222 is one of the few available sensors we have found that can be clocked very fast, due in part to using two phase clocking, a floating gate sense node (which can be reset once per line or even once per frame), and an excellent package layout (short lines for low inductance). The major limitation of this sensor is the on-chip video amplifier, which has a bandwidth of only 25 MHz. Even with the limitation of the amplifier, useful video is produced as seen in the CTF patterns in Fig. 1, taken from line scans at pixel rates of 60 to 77.5 MHz. High speed operation, from 50 to 80 MHz pixel rates, benefits from analog signal processing. A self-clocked track and hold (T/H) circuit used to enhance A/D capture will be described separately.¹

The camera consists of four detachable parts as seen in the GY5 photograph, Fig.2. The first is the CCD, second is the video circuit, and the third is the high-speed logic (ECL) circuit card, or alternatively for the GY6 an RS-170 sync/clock generator circuit (not seen in photograph, but in block diagram of the system, Fig. 3). The fourth is the low-speed logic circuit card.

2. DESIGN CONSIDERATIONS FOR HIGH SPEED CCD OPERATION

To achieve high-frame rate video with a single output port CCD sensor, two basic criteria must be met. First, the sensor design must allow high-speed clocking of the horizontal register. This is due to the

fact that the active line time, where the pixels are contributing to video generation, dominates the total line time (which includes the vertical shift and any other overhead such as sync pulses and front/back porches). The Loral Fairchild CCD222 device is designed with a two-phase serial register that is capable of being clocked at 80 MHz or even higher.²

A second fundamental concern involves the ability of high-speed driving of clock lines for moving photocharge. The drive circuitry must have the ability to quickly charge and discharge the CCD clock line capacitance and adjust for proper timing of the two phases to ensure that maximum charge transfer efficiency (CTE) is maintained. The level shifting clock drivers used in the GY6 are charge pump drivers, which allow very high-speed control of large currents for charging of the horizontal and vertical clock lines. Coupled with the high-speed logic circuit's independent control of the leading and trailing edge timing of the horizontal clock phases, H1 and H2, this provides precise control for optimizing CTE at high clocking rates. That is, at least to the maximum extent possible given the inherent nonuniformity of voltage distribution along resistive polysilicon clock lines. The operation of this level shifter circuit was previously described for its use in the more general purpose LANL High Speed Solid State Imager Test Station.³

3. VIDEO CIRCUIT CARD

The card consists of a single layer surface mount technology (SMT) component side, with the opposite side where the CCD is inserted forming a ground plane. The video card block diagram, Fig. 4, shows the high-speed level shifting clock drivers connected to the CCD inputs for horizontal clocks H1 and H2, vertical clocks V1 and V2, and the photosite transfer clock P. The CCD video output is buffered by a single transistor stage, and then dc shifted for input to a clamping preamplifier.

The preamplifier output may be sent off the video circuit card to the self-clocked T/H circuit for high-speed operation,¹ or continue on to the peak stretcher and a synchronously clocked T/H for forming RS-170 video. The synchronously clocked T/H output is then sent off the video circuit card to an analog multiplexer on the RS-170 sync/clock generator card, where the NTSC sync is mixed with the video.

4. HIGH-SPEED LOGIC (ECL) CIRCUIT CARD

The high-speed logic block diagram is seen in Fig. 5. The card can be fitted with an on board crystal oscillator or can be driven with an external source, at a frequency of 2x the desired pixel rate (up to a maximum of 160 MHz.)

The logic has timing adjustments to allow independent control of the leading and trailing edges of each horizontal clock phase, H1 and H2. By carefully adjusting the overlap and duty cycle of these phases, optimum performance of CTE can be achieved.

5. RS-170 SYNC/CLOCK GENERATOR CIRCUIT CARD

To operate the camera as a standard RS-170 black and white (noninterlaced) video source, one has only to replace the high-speed logic card with this card, Fig. 6. The Philips SAA 1101 Universal Sync

Generator becomes the system controller, providing vertical timing initiation, composite blanking, and a gated horizontal clock phase generator (U4, U5, U6, and U7). Composite sync is multiplexed with the video coming from the synchronously clocked T/H on the video card. The NTSC compatible video is then available through a BNC connector on the back panel. A future version of the GY6 switchable camera may include interlaced video and not require the card swap, using paralleled solid-state switches instead for selecting the operating mode (RS-170 or high speed).

6. SLOW LOGIC TRANSISTOR-TRANSISTOR LOGIC (TTL) CIRCUIT CARD

The slow logic block diagram is seen in Fig. 7. It functions almost identically whether one is clocking it from the high-speed logic (ECL circuit card) or the RS-170 circuit card. This circuit generates the timing for the vertical clocks (V1 and V2) and photosite transfer clock (P clock) and sends them to the level shifter drivers on the video circuit card. When used with the high-speed ECL circuit card, back panel inputs also support instant reset, and image dump capabilities. Integration time is also controlled by this circuit. A future version of the GY6 will allow instant frame reset and image dump for the RS-170 mode, making synchronization to external events an easier task.

7. APPLICATIONS

The primary mission of LANL Group P-15 involves fast transient neutron imaging in the underground nuclear testing program. Here the camera disintegrates within milliseconds of frame start. The maximum data rate is called for in this application. The camera has also been proposed for high-speed image capture of several military applications, requiring variable frame rate capability. It has also been used to collect data for underwater mine detection (currently in RS-170 mode). Lastly, it will soon be used in real time image capture in a high speed medical imaging application.⁴

8. CONCLUSIONS

This camera is an upgrade of a series of LANL high-speed model GY area cameras based upon the Loral Fairchild CCD222 sensor. The horizontal phase split clocks with independent control of leading and trailing edges ensure proper timing overlap for clocking of photocharge along the horizontal register, even at fast rates. The use of a unique level shifting clock driver provides sufficient current drive to clock the horizontal register clock lines (200 pF) to rates exceeding 80 MHz and to drive the vertical clock lines (12,000 pF) to rates exceeding 2 MHz. The main limiting factor to optimal high-speed performance seems to be the on-chip amplifier. Options for modifying the amplifier have been proposed and may be implemented in the future. Modification of the camera operational mode is simple, requiring a change of a circuit card.

9. REFERENCES

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Fig. 1a. Line scan of video at 60 Mpixels/s.

Fig. 1b. Line scan of video at 77.5 Mpixels/s.

Fig. 2 GY5/6 High speed camera components.

Fig. 3 Block diagram of GY6 with optional RS-170 card.

Fig. 4 Video card block diagram.

Fig. 5 High-speed (ECL) logic card block diagram.

Fig. 6 RS-170 sync/clock generator card block diagram.

Fig. 7 Low-speed (TTL) card block diagram.

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