**TOTAL IONIZING DOSE EFFECTS ON MOS AND BIPOLAR DEVICES
IN THE NATURAL SPACE RADIATION ENVIRONMENT**

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OSTI**Abstract**

Mechanisms that control the response of MOS and bipolar devices to ionizing radiation in the natural space environment are briefly reviewed. Standard tests based on room-temperature irradiation and elevated temperature annealing are described for MOS devices to bound the effects of oxide and interface-trap charge in space. For bipolar devices that exhibit enhanced low-dose-rate sensitivity, a standard test equivalent to that developed for MOS devices is not available. However, screening techniques based on room temperature and/or elevated temperature irradiations are described which can minimize the risk to spacecraft and satellite electronics from this phenomenon.

1. Introduction

MOS (metal oxide semiconductor) and bipolar electronics are mission critical elements for spacecraft and satellites. In space, their response to ionizing radiation from high-energy electrons and protons can limit the performance and lifetime of a space system. Components used in these systems may or may not have been designed specifically for survival in this harsh environment. Thus, it is important to understand what controls the response of MOS and bipolar electronics to ionizing radiation exposure, and how one can perform economical ground testing that will ensure that devices and integrated circuits (ICs) will function as intended for the lifetime of a mission. In this paper, we briefly review the basic mechanisms of MOS and bipolar radiation response, and discuss test methods that have been developed on the basis of this knowledge.

2. MOS Radiation Response

When a MOS device or IC is exposed to ionizing radiation, electron-hole pairs are created in the transistor gate oxide, and in parasitic insulating layers of the devices. This process is illustrated schematically in Fig. 1. Under positive gate bias, electrons rapidly transport to the gate and leave the oxide, while holes transport slowly toward the Si. A fraction of these holes are trapped near the Si/SiO₂ interface at O vacancies, leading to a shift in the threshold voltage of the transistor [1]. During the hole transport and trapping processes, hydrogen is released within the oxide, and may transport to the interface and react with Si dangling bonds, forming interface traps [2-4]. Some holes trapped near the interface induce compensating electron traps, which are often called border traps [5,6]. The effects of faster border traps are similar to those of interface traps [7], and slower border traps serve primarily to mitigate the effects of trapped positive charge in the SiO₂ [8,9]. While border traps are quite important to MOS radiation response, and must be considered when attempting to optimize device processing, hardness assurance tests can be developed without explicitly including their effects in the test design. Thus, the goal of a radiation hardness assurance program for MOS components is to develop ground tests that provide conservative estimates of the impact of trapped holes and interface traps in gate and parasitic transistor structures on device and IC performance in the space environment [10,11].

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Fig. 1. Schematic illustration of ionizing radiation effects on a MOS transistor.

3. MOS Hardness Assurance

Present standard methods for MOS radiation hardness assurance are based on the need to provide tests for potential failures due to oxide-trap charge and interface traps. In device-quality thermal oxides, MOS net oxide-trap charge is positive, and dominated by trapped holes [1]. The percentage of radiation-induced holes trapped near the Si/SiO₂ interface varies greatly with device processing, as does the rate at which holes are neutralized via annealing or electron compensation processes [1,10,12]. Thus, for some devices a large density of slow annealing trapped holes can lead to device failure even in the low-dose-rate environment of space. For others, annealing or charge neutralization effects can mitigate the effects of trapped-hole buildup. Interface traps affect *n* and *p* channel MOS transistors differently. For *n* channel transistors, interface traps tend to be charged negatively, which leads to positive threshold voltage (V_{th}) shifts. For *p* channel transistors, on the other hand, interface traps are charged positively, leading to negative V_{th} shifts. In both cases, interface traps also cause mobility degradation. During irradiation, *n* channel MOS transistors are at positive or zero bias, in contrast to *p* channel transistors which are at negative or zero bias. Because MOS radiation response at positive electric field is nearly always worse than the response at negative electric field, *n* channel MOS transistor response tends to dominate CMOS IC radiation response, as reflected in the design of standard test methods.

Figure 2 is a schematic illustration of the present MOS standard test incorporated in US MIL-STD (military standard) 883, test method 1019, and which will also be incorporated in the upcoming release of ASTM (American Society for Testing of Materials) standard F-1872. The first step is to irradiate the device to the desired dose, using Co-60 irradiation. As long as the dose rate of this exposure is higher than that in space, this portion of the test procedure provides a conservative test of the effects of oxide-trap charge (e.g., high leakage currents) on MOS response in space [10,12]. There is a provision in the test method that allows parts which fail parametrically to be annealed at room temperature, to see whether annealing processes enable them to recover quickly enough that the devices would be acceptable for space use. This is the (optional) second step of the test in Fig. 2. The room temperature anneal may not be performed on devices that fail the first test functionally, because of the risk that debiasing effects may lead to radiation-enhanced recovery of the device [13] which could lead to an overly optimistic estimate of its hardness in space. Thus, for parts that fail the initial Co-60 irradiation in Fig. 1, the only options are to (1) test a second group at a still lower dose rate, or (2) find a substitute part.

Fig. 2. Schematic illustration of US MIL-STD 883, Test Method 1019 for MOS devices and ICs.

For most parts that pass testing after either the Co-60 irradiation or room temperature anneal, there is still a need for further testing to ensure that devices will not fail due to interface trap effects in space (e.g., reduced output current drive, timing degradation, reduced noise margin). In standard test methods, this is accomplished by irradiating the same group of devices to an additional dose, so that they have received 150% of the dose expected in the environment. The devices are then given a 1-week anneal at 100°C before being tested again. The purpose of this anneal is to accelerate the neutralization of trapped holes and the buildup of interface traps sufficiently as to induce a more positive shift in n channel MOS transistor V_{th} than will occur in space [12,14]. The additional 50% "overstress" in dose that is given the devices before the 100°C anneal is to offset (1) annealing of damage in p channel transistors, (2) the potential that switched-bias irradiation can lead to greater interface-trap buildup than static bias irradiation, and (3) that a small amount of interface-trap annealing can occur in some devices at 100°C [14]. There are provisions in the test method that permit the additional irradiation and elevated temperature anneal in Fig. 2 to be modified or even omitted for cases in which it can be shown that interface trap effects are sufficiently small or well controlled that they do not cause failure. This can potentially reduce the time and expense involved in MOS IC qualification. However, in the absence of such knowledge, one must successfully complete the entire sequence in Fig. 2 to qualify a MOS process lot for use in the space environment.

Finally, we note that some MOS devices show a change in radiation response when subjected to burn-in [15-17]. This phenomenon is not well understood, though it is thought potentially to be related to the movement of hydrogen. Thus, unless it has been demonstrated that devices are not sensitive to this effect, the tests of Fig. 2 should be performed on devices that have been exposed to all elevated temperature screen that they will experience before system insertion [15,17]. Note this may include board level as well as package level temperature cycles.

4. Future Trends in MOS Radiation Response

The test method illustrated in Fig. 2 was developed as a generic screen for the effects of oxide and interface trap charge in MOS technologies, and can still be used successfully to do so in the future. However, scaling trends in advanced MOS technologies make the additional 50% overstress and elevated temperature anneal less important for devices with thin gate oxides (e.g., less than ~ 100 Å) intended for use in relatively low-dose space applications (e.g., less than ~ 30 krad(SiO_2)). In these cases, the oxide is simply too thin to support enough interface-trap buildup to cause device failure [12]. Still, oxide-trap charge related failures in parasitic oxides of the device remain a concern for all MOS technologies, even with the most advanced processing. So, for all MOS devices, the first half of the procedure in Fig. 2 must still be performed, and the second half of the procedure may only be omitted for devices which are known to show negligible interface-trap buildup.

Recently, it has also been shown that high doses of ionizing radiation (> 1 Mrad(SiO_2)) can lead to enhanced leakage in thin MOS gate oxides [18]. This phenomenon is known as radiation induced leakage current, and is analogous to the stress induced leakage current shown by MOS devices exposed to high-field stress [19]. Hence, in the future, it may not only be necessary to test MOS devices for failures due to the buildup of radiation-induced charge, but it may also be necessary to understand the effects of ionizing radiation on MOS long-term reliability.

5. Bipolar Radiation Response

Bipolar devices can also be quite sensitive to ionizing radiation effects in space. The chief concern for these devices are (1) gain degradation, and (2) leakage due to parasitic MOS elements. The second of these concerns is primarily an issue for digital bipolar devices [20], which are rarely used in space due to their high power dissipation relative to digital MOS devices and ICs. Moreover, enhanced leakage in bipolar devices and ICs is easily screened with tests analogous to those used for MOS oxide-trap charge in Fig. 2. Therefore, the primary concern for bipolar devices in space is gain degradation in linear bipolar devices and ICs.

Figure 3 is a schematic illustration of the primary ionizing radiation effects in linear bipolar devices. The damage to the device is a consequence of the low-quality oxide that often overlies the emitter-base junction in a linear bipolar IC [21,22]. If there were high electric fields (like those in MOS gate or field oxides) across these insulators, these linear bipolar devices would fail at low total doses at any radiation dose rate [21,23]. However, only the small fringing field from the emitter-base junction is typically present in these oxides. At such low electric fields, the base oxide is subject to space-charge effects that can alter the transport of radiation-induced positive charge, leading to less net oxide-trap charge near the base-emitter junction and fewer interface traps at the surface of the active base [23,24]. Net positive charge in the oxide that overlies the base of an NPN bipolar transistor [22,25] or a lightly doped emitter of a PNP transistor [26] increases the carrier surface recombination rate and decreases the device gain. The same effect results from interface-trap generation along the surface of the active base of either device type [22,25-28]. At low dose rates, the gain degradation of bipolar transistors can be up to 5-10 times worse than that observed at higher rates [29-31], with greater gain degradation typically observed at lower total doses for lateral and substrate PNP transistors than for NPN or vertical PNP transistors [25-32].

Fig. 3. Illustration of radiation induced charge at or near the emitter-base junction of a bipolar transistor.

6. Bipolar Hardness Assurance

In contrast to MOS devices, there is no simple testing sequence analogous to Fig. 2 that can be employed to easily predict bipolar response in space. This is because there is no series of higher-rate irradiations and/or anneals that can simulate the charge distributions one obtains at low dose rates in bipolar base oxides. To date, the most promising approaches to screening linear bipolar devices for enhanced low-dose-rate gain degradation are (1) low-dose-rate irradiation, and (2) elevated temperature irradiation. The obvious disadvantage of method (1) is that dose rates in space are typically 1-2 orders of magnitude lower than those which can be easily or practically achieved in the laboratory. One cannot perform a seven-year ground test to determine whether parts will survive seven years in space! Thus, with low-dose-rate irradiation, one always risks that the gain degradation in space will exceed that observed during a higher rate exposure on the ground. A few device types even show enhanced gain degradation or increased offset voltages at $\sim 1 \text{ mrad}(\text{SiO}_2)/\text{s}$ than at $\sim 10 \text{ mrad}(\text{SiO}_2)/\text{s}$ [30,33,34], making it very difficult to identify a low-dose-rate testing sequence that can be used to predict bipolar response in space. ASTM F-1872 suggests that one may reasonably expect that tests at $10 \text{ mrad}(\text{SiO}_2)/\text{s}$ to a dose that is twice that expected in space [34] should approximate or bound bipolar response in space; however, this is based on limited experience, and is not guaranteed to be conservative.

A second alternative is elevated temperature irradiation. This is based on the idea that one can speed up the charge transport that occurs in the bipolar base oxides at low electric fields by heating the device during irradiation [21,23,31-35]. Typically, devices are irradiated at $\sim 100^\circ\text{C}$ at a dose rate of $\sim 10\text{-}50 \text{ rad}(\text{SiO}_2)/\text{s}$ [31-35]. For many device types this approach has been successfully applied, as long as a design margin of ~ 3 is applied in parametric degradation [34]. For example, if one can tolerate a shift in offset voltage of no more than 30 mV for a linear bipolar device, one would need the change to be less than 10 mV after the elevated temperature irradiation. Once again, these recommendations are based on the results of only a few dozen tests, and are subject to revision on the basis of future experience.

Because there is no fully validated test for bipolar radiation response in space, one should view the testing recommendations in ASTM F-1872 [34] as somewhat preliminary, and should be very careful to apply the design margins specified in the test method. At Sandia National Laboratories, our approach for screening bipolar devices for use in a low-dose-rate radiation environment is to combine both low-dose-rate and elevated temperature irradiation methods in an initial screen, as illustrated in Fig. 4. The first group of devices is irradiated at $\sim 50 \text{ rad}(\text{SiO}_2)/\text{s}$, and serves as a control against which groups 2 and 3 will be compared. Group 2 is irradiated at the same dose rate, but at higher temperature during irradiation. This is a quick way to check to

possible enhanced low-dose-rate sensitivity (ELDRS) effects, which is especially useful if one is trying to choose among more than one device type. Group 3 is an actual low-dose rate irradiation, but is limited to at most 2-4 weeks in duration for practicality. For all groups, the total dose should be delivered in steps up to at least 2-3 times the dose expected in space. If the degradation of the parts in either Groups 2 or 3 is significantly greater than that of the devices in Group 1 at equivalent doses, then one should either try to find an equivalent device type that does not show the ELDRS effect, or more detailed characterization may be required [34].

Fig. 4. Screening technique to identify linear bipolar devices showing enhanced gain degradation in space.

An especially vexing problem in applying the screen of Fig. 4 to linear bipolar ICs is that, *a priori*, it is usually not possible to know which bias condition is likely to reflect worst-case device response. For some types of bipolar ICs, worst case response is obtained for devices with all pins grounded; for others, worst case response is observed for bias applied to the inputs [34,36]. This not only means that more than one bias condition may need to be checked for the screen of Fig. 4, but is also a problem for using unpowered backup parts in the satellite. For some device types, the unpowered spares are likely to fail [36] before their powered counterparts! Thus, while screening techniques are available to assist in the effort, qualifying linear bipolar parts for space applications remains a challenging task for ELDRS devices.

7. A Few Words on COTS

There is a desire to use less costly commercial off-the-shelf (COTS) devices wherever possible in space systems, as opposed to more expensive radiation-hardened parts. At the same time, there is a desire to reduce design margins and safety factors in testing. In the author's opinion, this combination is a recipe for future disasters. Only those systems that (1) understand their radiation environment very well, (2) incorporate hardness assurance testing early in the system design cycle, and (3) manage the overall risk to the system will avoid premature failure of their system. This is due to (1) the well-known variability of the radiation response of COTS parts, from lot-to-lot, and within lots [37,38], and (2) the difficulty in testing an IC that is not specifically designed for use in a radiation environment sufficiently well to ensure that an unexpected early failure mode is not overlooked. Thus, the overall cost to a system may be higher if less expensive commercial parts are selected, than if more expensive radiation-tolerant devices are selected. Still, there is no doubt that COTS devices will play an increasingly important role in future space systems, and the most successful and highest performing systems will be those that manage the risk of COTS devices the most successfully.

8. Conclusions

The space radiation environment is challenging for both MOS and bipolar technologies. Standard tests are available to provide a conservative bound on MOS response in space, but testing linear bipolar devices for space applications is more challenging. With the release of ASTM F-1872, screening techniques will be available to assist this task, but there is more risk inherent in the outcome of tests of bipolar devices for space than for testing MOS devices. Because of these inherent risks, there is a premium in identifying linear bipolar devices that do not show enhanced gain degradation at low dose rates. For both MOS and bipolar devices, the use of COTS parts will certainly increase in the future, and the most successful space programs will likely be those that select, screen, and shield these COTS devices the most carefully.

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