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A SIMPLE SINGLE-PHOTOMASK PROCESS FOR FABRICATION OF HIGH-EFFICIENCY MULTICRYSTALLINE SILICON SOLAR CELLS

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We have developed a simplified process sequence for fabrication of high-efficiency multicrystalline silicon (mc-Si) solar cells. Photolithography is required only to define the evaporated metal gridlines. We use this fast turn-around, high-yield baseline process to evaluate different mc-Si materials and new processing procedures. The process uses a one-step emitter diffusion/drive-in and an aluminum-alloyed back surface field to provide a well-passivated cell with excellent blue and red response. Laser-scribed cell-isolation grooves are used to define both moderate-area (4 cm^2) and large-area (42 cm^2) cells. We have been able to achieve minority-carrier diffusion lengths well over $300 \text{ }\mu\text{m}$ in $2\text{-}\Omega\text{cm}$ mc-Si material and have achieved efficiencies of 16.2% in 4-cm^2 cells. This was accomplished without hydrogenation to passivate bulk defects or texturing to reduce reflectance. By using the same fabrication process for both small-area and large-area cells, we intend to determine and minimize the effect of areal inhomogeneities on large-area mc-Si cell performance.

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Multicrystalline silicon (mc-Si) shows good promise as a cost-effective material for high-efficiency. Efficiencies have reached 17.7% in 1-cm² mc-Si cells [1], and 17.2% [2] in specially processed large-area mc-Si cells. A distinguishing feature of the above cells is the complex processing used to produce them. The small-area cell used multiple photolithography steps and evaporated metals [1]. The large-area cell utilized sophisticated screen printing and a mechanically textured substrate [2]. Our work has retained essential high-efficiency aspects with a simpler protocol, and achieved over 16% efficiency using commercial mc-Si material. The process, similar to one developed previously at the University of New South Wales [3], is especially useful as a baseline for experimental evaluation of different mc-Si materials and new cell processes. Another goal of this work is to produce both moderate- and large-area cells [4] with the same process, providing a way to determine the effect of small regions of defective material on the performance of large-area cells.

Table I. High-Efficiency One-Photomask Process for mc-Si Solar Cells

Damage removal etch and clean
APCVD-oxide - Back, 400°C (Optional)
POCl ₃ One-step emitter diffusion/drive-in (80-100 Ω/□, 875°C)
APCVD-oxide - Front, 400°C
Shallow laser-isolation scribe (front of moderate-area cells only)
Groove etching/cleaning
Deglaze front and back
Aluminum deposition (back, 1 μm)
Aluminum alloy, ≤ 900°C (also grows 10 nm passivation oxide on the front)
Photolithographic definition of front grid
Contact oxide etch
TiPdAg deposition (front)
Aluminum deposition (back)
Lift-off
Forming Gas Anneal/ Metal Sintering (400°C)
Antireflection coating deposition
Separation laser scribe (backs of large-area cells only)

The baseline process developed at Sandia is outlined in Table I. The damage removal etch is specific to the material being processed. The one-step POCl_3 emitter diffusion results in an 80 to $100 \text{ } \Omega/\square$ emitter with a peak doping concentration below $6 \times 10^{19} \text{ cm}^{-3}$ to ensure low emitter recombination. Oxide is deposited on the front side using an atmospheric pressure chemical vapor deposition (APCVD) process. A Nd:YAG laser ($1.06 \text{ } \mu\text{m}$) is then used to scribe grooves through the emitter diffusion, thus defining the cell area when in-wafer isolation is required. The damaged region surrounding the isolation grooves is removed by etching in KOH solution at 70°C . The APCVD-oxide mentioned above provides additional protection for the emitter from the KOH etch. We found that the minimum laser pulse energy required to continuously penetrate the emitter junction gave the best performance. Higher energy laser scribing decreased the fill factor and increased the non-ideal recombination current in the dark current-voltage curve. After an HCl clean and an HF etch, aluminum is deposited on the backs. We have found that it is not necessary to protect the fronts during the aluminum deposition. The aluminum is alloyed at temperatures between 800 and 900°C , depending on the substrate material. The samples are pushed in oxygen and experience a short oxidation stage at the beginning of the alloy process. This procedure prevents the aluminum from balling up on the back side and also grows a thermal passivation oxide on the front side about 10-nm thick. This combination of emitter diffusion and aluminum alloy processes provides a well-passivated cell with excellent blue and red response. An internal quantum efficiency plot for a typical mc-Si cell produced using this process is shown in Figure 1.

Figure 1. External and internal quantum efficiency (EQE and IQE respectively) for an “average” cell on Solarex $2 \text{ } \Omega\text{-cm}$ material using the process in Table I. This particular cell had an efficiency of 15.4% , and a minority-carrier diffusion length of $260 \text{ } \mu\text{m}$.

A key feature of our baseline process is the use of laser-scribed grooves for cell isolation and/or separation. We investigated sequences other than the one outlined in Table I. Laser cutting the cell-isolation grooves after the alloy process resulted in lower current, voltage, and fill factor. Scribing the grooves after the AR coating resulted in electrically isolated gridlines. Although the evaporated TiO_2 acts as an etch mask for the groove cleaning etch, discontinuities in TiO_2 coverage at the edges of the gridlines allowed the KOH to etch a trench in the silicon outlining the grids. We also investigated the effect of varying the duration of the KOH etch on cell performance and found that excessive etching caused problems with the lift-off process; TiPdAg metallization sometimes remained in the grooves, interfering with cell isolation and causing shunting around the edges of the cells.

Our best cell results to date for two different types of mc-Si material are shown in Table II. In both cases the cell thickness was about 270 μm . Also, the solar-weighted average reflectance (R_w) was greater than 8% for both of these cells, leaving considerable room for improvement. In the case of the higher resistivity Solarex material, the cell lost considerable current due to recombination at the back surface. We either need to improve our back surface field treatment or use thicker substrates to obtain better performance with this material.

Table II. Best mc-Si Cell Results to Date with the One-Mask Process

Material	Bulk Res. ($\Omega\text{-cm}$)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	L_n (μm)
HEM	0.9	620	32.6	78.9	15.9	150
Solarex	2.0	602	34.6	77.4	16.2	> 300

Area = 4 cm^2 , 25°C, AM1.5G Spectrum

We intend to fabricate both small- and large-area cells on adjacent wafers cut from the same mc-Si ingot to correlate the performance of the large-area cells with any small regions of defective material that are detected by the small-area cells. This is important because the performance of large-area cells may be limited by defects in a small portion of the cell area. We can then investigate variations in the process sequence, such as gettering or defect passivation, to determine whether any improvement can be made to those regions which critically limit cell performance. This work is part of a larger effort to produce a 15%-efficient mc-Si module, which will require a high-yield fabrication process for 16%-efficient large-area mc-Si cells.

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