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Conf-940678-2

INFLUENCE OF ELECTRODE GEOMETRY ON THE HIGH-FIELD CHARACTERISTICS OF PHOTOCONDUCTIVE SILICON WAFERS

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Abstract : A series of experiments were conducted to study the influence of electrode geometry on the prebreakdown (and breakdown) characteristics of high resistivity ($\rho > 30 \text{ k}\Omega\text{-cm}$), p-type Si wafers under quasi-uniform and non-uniform electric field configurations. In the quasi-uniform field configuration, the 1mm thick Si wafer was mounted between the slots of two plane parallel stainless steel disc electrodes (parallel), while the non-uniform field was obtained by mounting the wafer between two pillar-type electrodes with a hemispherical tip (pillar). The main objective of the above investigation was to verify if the uniform field configuration under a parallel system has a positive influence by reducing the field enhancement at the contact region, as opposed to the definite field enhancement present in the case of the non-uniform pillar system. Also, it was proposed to study the effect of the contact profile on the field distribution over the wafer surface and hence its influence on the high-field performance of the Si wafers.

1. INTRODUCTION

The high-field characteristics of Si wafers used in Photoconductive Power Switch (PCPS) applications is of considerable importance for reliable and efficient high-power operations. The maximum voltage that can be switched by a PCPS is determined by the high-field limitations of the semiconductor - dielectric system, specifically the surface flashover field and more fundamentally by the high-field limit of the quasi-ohmic response of the semiconductor wafer [1]. It is observed that beyond a limit of voltage application, when the high-field conditions for a non-ohmic current response is established, the voltage (V) - current (I) characteristics of the semiconductor departs from the ohmic response. In this context, it would be advantageous to operate the PCPS under a uniform field configuration, with no apparent field enhancement effects due to electrode geometry. Such a configuration would theoretically enhance the maximum voltage that can be applied to the semiconductor. Also, a uniform field configuration would force a more uniform current distribution through the bulk of the wafer, perhaps reducing the chance of current filamentation because of local field enhancements. On the other hand, complex arrangements required to mount the Si wafer between a parallel plane electrode configuration will have to be weighed against the actual advantages that can be realized by such a system. Also, the effect of triple junction emitted electrons from the large area parallel plane electrodes could enhance the pre-breakdown currents.

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This work was supported by the United States Department of Energy under Contract DE-AC04-74AL85000.

These aspects need to be studied experimentally to determine the suitability of the electrode geometry that can be adopted for high-field PCPS applications.

2. EXPERIMENTAL PROCEDURE

The experimental arrangement for conducting high-field studies on Si wafers has been described in detail elsewhere [2]. The notable features of the test system are : a vacuum test chamber with provision for introducing different dielectric gases (air, N₂, SF₆ etc.); a continuously variable (2 - 100 kV) double exponential (0.39 / 3.0 μ s) impulse voltage generator; an E-dot probe for voltage measurement; a 50 Ω Current Viewing Resistor for pre-breakdown current measurement; a Rogowski coil for measuring high currents (during breakdown); ultra-violet - visible (UV-VIS : 220 - 400nm) and infrared (IR : 760-1100 nm) photomultiplier tubes, and an intensified 2D array computer controlled charge coupled device (CCD) camera. For the present series of experiments, two sets of plane parallel electrode structures (one fabricated at the University of South Carolina (USC), and the other from Sandia National Laboratories) and a "pillar electrode" structure were used (see Fig.1). As mentioned before, the quasi-uniform field configuration is obtained by mounting the wafers between two plane parallel electrodes (Fig.1[a, b]), while the non-uniform field was obtained using the pillar-type electrode system with a hemispherical tip (Fig.1[c]). In order to improve the electrical contact in the parallel system (considering the generally poor contacts obtained by limited mechanical pressure between the electrode and the contact metallization), the USC parallel system (Fig.1[a]) involved soldering of Ag strips on to the Au metallization using indium solder and obtaining a pressed mechanical contact between the Ag strip and the solid electrodes.

Fig.1[a]: USC Plane Parallel Electrode Configuration ; [b]: Sandia Plane Parallel Electrode Configuration ; [c]: Pillar Hemispherical Electrodes

Experiments were carried out on Si wafers with two different types of contact profiles: viz., one with a sharp contact corners (Fig.2[a]) and the other with rounded contact corners (Fig.2[b]). The

sharp contact corner samples (with contacts on both sides of the wafer) were deposited at the Sandia National Laboratories, while the rounded contact samples were made at the USC.

Fig. 2[a]: Two-side sharp cornered contact (Cr/Cr/Mo/Au) Si sample (Sandia)
 2[b]: One-side rounded corner contact (NiCr/Au) Si sample (USC)

The experimental procedure consisted of the following steps :

- Step 1: RCA cleaning of the wafers
- Step 2: Contact deposition on RCA cleaned wafers
- Step 3: The applied electric field (E) vs current (I) characterization of contact deposited samples using pillar electrode system:
 - (i) Vacuum : up to 16 - 25 kV/cm or until first surface flashover
 - (ii) SF_6 (1.5 atm.) : up to 35 - 55 kV/cm (depending on appearance of non-ohmic current)
- Step 4: $E - I$ characterization of above tested samples in Sandia parallel system, before soldering
 - (i) Vacuum; (ii) SF_6 (1.5 atm.)
- Step 5: Soldering of Ag strip using indium solder
- Step 6: $E - I$ characterization, after soldering, using pillar and USC parallel electrode systems, both in vacuum and SF_6 ambients.

The $E - I$ characterization during each stage of experiment was limited to the ohmic-regime of response of the semiconductor wafer to prevent any permanent change in the $I - V$ behavior of the wafer because of filamentation. For the same reason, care was taken not to subject the wafer to any surface flashover event in SF_6 , which could result in the damage of the contacts.

3. RESULTS

The experimental results emphasize the role of the electrode configuration and the contour of the metallized contacts on the high field performance of the Si wafers. It has to be noted that, due to the complexity of the mounting requirements in the parallel electrode system, the contact between the metallization on the Si wafer and the main electrode is not always perfect and hence the high field performance under such situations is determined by the local field enhancement effects at

the contact imperfections, rather than the main electric field distribution. This was especially noticeable in the case of the USC parallel system, when the Si wafers were mounted without appropriate soldered contacts, and also when the rounded contact contour samples were tested using the Sandia parallel system. In the pillar system, since the contact is made at a single point, the problem of contact imperfections does not arise. Because of the different variants involved, the E - I characteristics of the Si wafers under the parallel system is not as reproducible as that under the pillar system.

(A) Effect of contact imperfections on high-field characteristics in the parallel electrode system

The problem of partial-discharges at contact microvoids has been addressed in detail in our 1993 annual report to the SDIO / IST [2]. During experiments with Si wafers mounted in the USC parallel system with pressed mechanical contacts, when the contact was imperfect, strong partial discharge activity at the contacts, with short current bursts and associated light emission was observed. A typical current and light emission characteristics during a partial discharge process under the parallel system is depicted Fig.3 .

Fig.3: Typical characteristics during a partial discharge process in USC parallel electrode system
V: 1.9 kV / div; I: 70 mA / div; IR: 20 mV / div; VIS: 20 mV / div

The reason for the above partial discharge activity is evidently the presence of microvoids at the contact region between the Au metallization and the main electrodes, since it is difficult to obtain a perfect contact over a large area of the electrode by pure mechanical contacts. Hence, we

have adopted the new technique of soldered contacts, which provides much better contacts than that by pressed mechanical contacts. The Sandia parallel system, with a narrow electrode edge does not have the problem of partial discharges at contacts, when wafers with straight contact edges [Fig.2(a)] is appropriately mounted. On the other hand when the samples with rounded contacts are mounted in the Sandia parallel system, as shown in Fig.4, because of the natural void created at the rounded region of contact with dimensions close to thickness of the metallization ($< 1\mu\text{m}$), there is indication of strong partial discharge activity starting at very low voltages.

Fig.4: Rounded contact Si samples mounted in Sandia parallel electrode system: origin of voids at contacts

(B) Comparison of Pre-breakdown currents under pillar and parallel electrode systems

The comparison of the pre-breakdown currents of the same Si wafer under pillar and parallel electrode systems indicate significant influence of the electrode geometry and the contact contour on the wafer.

The sharp cornered contact Sandia samples (Fig.2[a]) with a contact gap spacing of 1.5cm, was at first measured using the pillar system (note: even though the metallized contacts were present on both sides of the wafer, the electrode contact was made only one side) in vacuum and SF_6 ambients. Under the pillar system, the Sandia samples suffered failure by surface flashover at fairly low fields (5 - 10 kV/cm) in vacuum ambient, and indicated very high pre-breakdown currents, at fields in the range of 10 to 20 kV/cm in 1.5 atm. pressure SF_6 ambient. There was clear indication of light emission, associated with the large current, from the sharp contact corners which are exposed under the pillar system. The voltage, current and light characteristics of a sharp cornered contact Sandia sample in SF_6 ambient under the pillar system is shown in Fig.5, and Fig.6 shows the CCD image of the light emission from the contact corners, associated with the large current. Note that, this light emission is not due to a partial discharge at any contact microvoid, rather it is due to the high current density at the contact corners because of high field concentration at those regions.

Fig.5: Voltage, current and light characteristics of a sharp cornered contact Sandia sample in pillar electrode system

Fig.6: CCD image of light emission from the sharp contact corners, associated with characteristics shown in Fig.5

When the Sandia samples [Fig.2(a)] are tested using the Sandia parallel system, there was significant improvement in the performance of the wafers, with perfect ohmic behavior observed well beyond 20 kV/cm, in SF₆ ambient. In fact, one of the samples withstood more than 72 kV (i.e., ≈ 48 kV/cm, assuming a uniform field for the 1.5 cm gap distance) in 1.5 atm. SF₆, without any indication of light emission from contact corners. A comparison of the applied electric field (average value, obtained by assuming no field enhancement) vs current characteristics in 1.5 atm. SF₆, for a typical sharp cornered contact Sandia sample under the pillar and Sandia parallel electrode systems, shown in Fig.7, clearly indicates that the current through the sample is more than a factor of 10 smaller under the parallel system, as compared to that under the pillar system.

Note that the current values under the Sandia parallel system has been multiplied by 10 to bring it into scale, for comparison with the currents under the pillar system.

Fig.7: Comparison of applied electric field vs current characteristics for a sharp cornered Sandia sample under pillar and parallel electrode systems in 1.5 atm. SF_6 ambient

Considering the situation of a rounded cornered contact sample (generally with a 0.5 cm gap spacing), with good semiconductor bulk and surface qualities, under the pillar system the wafer will withstand up to more than 25 kV/cm in vacuum and greater than 65 kV/cm in 1.5 atm. SF_6 without any departure from ohmic behavior. These very high withstand fields (average values, without considering field enhancement) under the pillar system for the rounded cornered contact samples, compared to the much poorer performance of the sharp cornered samples under the same electrode configuration, emphasizes the strong influence of the contact contour in determining the surface electric field distribution and the pre-breakdown current variation through the device. To have a comparison of the influence of the contact contour on the pre-breakdown current variation of Si wafers, experiments were performed on identically deposited (NiCr / Au contacts on one side) samples with sharp and rounded cornered contacts. The pre-breakdown current variation of two samples with different contact profiles, in 1.5 atm. SF_6 ambient under the pillar system, is shown in Fig.8.

Fig.8: Comparison of the pre-breakdown current variation of a sharp cornered contact and rounded cornered contact sample in 1.5 atm. SF_6 under pillar electrode system.

A computation of the field distribution along the contact edge of the Si wafer, for the sharp cornered and rounded cornered contact samples predicts a factor of ≈ 1.5 times smaller field enhancement factor for the rounded corner contacts than that for the sharp cornered contacts. Thus the significantly smaller pre-breakdown currents observed for the rounded cornered contact sample, is as expected from the theoretical prediction of the lower field enhancement of the rounded corner contour, compared to the sharp cornered contacts.

When the rounded corner contact samples are measured under the USC parallel system before any soldering, generally it shows a very poor response with strong current burst activity because of imperfect contacts between the Au metallization and the main electrodes. The evidence of imperfect contacts is observed when the pre-breakdown current shows frequent current spikes with associated light emission. More reproducible results are obtained from measurements under the USC parallel system when contact is made between the solid electrodes and a Ag strip soldered onto the Au metallization.

Measurements on the wafer after soldering Ag strips on the contacts, under the USC parallel system indicates clear pre-breakdown current variation with progressively increasing voltage application, with rare occurrences of current bursts in vacuum ambient. Comparing the voltage - current characteristics of a sample with soldered contacts, it is observed that the currents for the same applied fields are noticeably lower under parallel electrode system as compared to that in pillar electrode system (see Fig.9).

Fig.9 : Comparison of pre-breakdown currents of a rounded cornered contact sample under PHE and USC PPE systems (SF_6 ambient)

The above situation is reproducible for samples with fairly good bulk and surface properties, with minor variations in the current magnitudes, depending on the extent of heating performed for the soldering operation.

4. DISCUSSION

The complexity of the parallel electrode system makes handling of the Si wafer for effective mounting a serious problem. Because of the difficulty in making a perfect contact between the metallization and the main electrodes, the voltage - current characteristics of the Si wafers under the uniform field configuration is more difficult to reproduce than that under pillar system. As mentioned before, when the contacts are imperfect, the high - field performance of the Si wafer under the parallel system is determined by the local field enhancement effects at the contact imperfections, rather than the main electric field distribution between the large area electrodes. On the other hand, the high - field characteristics under the pillar electrode system is mostly determined by the semiconductor wafer properties and is more reproducible than the results obtained under the parallel electrode system. We analyze the significant results obtained from the present series of experiments, based on our knowledge of the influence of the semiconductor and the ambient dielectric properties on the high - field behavior of semiconductor - dielectric systems [3], as well as on the basis of the theoretical computation of the electric field distribution under the different electrode configurations.

(A) Field enhancement at contact imperfections and their effect on high-field performance of Si wafers under the parallel electrode system:

Contact imperfections, such as microvoids between the Au metallization on the Si wafer and the main electrodes of the USC parallel system (when the wafers are mounted without any soldering), as well as the void created at the rounded contact corner of a Si wafer when mounted in the Sandia parallel system (see Fig.4), are regions where the electric field distribution can be distorted because of the presence of the ambient medium (with a completely different dielectric constant) in the void region. More significantly, if the dimensions of the void is in the range of a micron, even a small potential difference (say, as small as 1V) would result in an high local electric field of 10 kV/cm. Considering, the large gap distance between the Au contacts on the Si wafer, the average field on the Si wafer itself would be generally much smaller than the local field because of the field enhancement at the contact imperfection. Hence, the high local fields at contact imperfections causes the failure of the ambient medium in the void region through partial discharges, at fairly low average applied electric fields. The partial discharge at the contact imperfections, in turn, introduces a sharp increase in the current through the semiconductor - ambient dielectric system, as well as creates enough light emission to be detected by the PMTs. An increase in the applied electric field, in the presence of partial discharges, can cause the failure of the Si wafer, through a premature surface flashover event triggered by the violent discharge activity at the contacts.

(B) Effect of field distribution on pre-breakdown currents under the pillar and parallel electrode systems:

The lower pre-breakdown currents in the parallel system compared to that under the pillar system (Figs. 7 and 9), for both the Sandia sharp cornered contact samples and the USC rounded corner contact samples, suggests that for the same applied electric field, the field distribution under the parallel system is more uniform than that under the pillar system, so as to cause a reduction in the current magnitude through the Si samples. When the wafer is subjected to high fields under the pillar system, the electric field near the knife edges of the contact metallizations (maximum thickness of about 3500 Å) will be significantly enhanced because of the non-uniform field configuration. On the other hand the parallel system masks the knife edges of the contacts, which results in the reduction of the field enhancement. From a 2D field computation performed at Sandia Laboratories using the ELECTRO software, it is observed that the field enhancement factor close to the middle of the contact edge under the pillar electrode system is approximately 1.4 times higher than under the parallel electrode system.

RESULTS OF 2D FIELD COMPUTATION

Distance, mm (from contact)	Enhancement factor (pillar electrodes)	Enhancement factor (parallel electrodes)	Ratio of Enhancement Factors (pillar/parallel)
10^{-3}	22.2	14.7	1.5
10^{-2}	5.6	4.4	1.3

$$\text{Average Ratio} = (1.5 + 1.3) / 2 = 1.4$$

If we plot the I vs E characteristics shown in Fig. 9 with corrected field values (by multiplying the fields under pillar electrode by 1.4), it is observed that the I-E curves for the pillar and parallel electrode systems coincide, confirming the theoretical prediction of the ratio of the field enhancement factors.

Even though the reduction in the field enhancement, and the consequent reduction in the pre-breakdown currents is noticeable under the parallel electrode system, it has to be noted that such an improvement is not noticeable when Si wafers with inherently higher pre-breakdown currents (probably because of poor bulk / surface qualities) are measured under the two electrode structures.

5. CONCLUSIONS

The practical difficulties in making a perfect contact between the semiconductor wafer (used for PCPS device applications) and the solid electrodes of a plane parallel electrode system imposes restrictions on the effective usage of a uniform field configuration for better high field performance of the PCPS material. When the contacts are imperfect, the high - field performance of the Si wafer in a parallel system is determined by the local field field enhancement effects and consequent partial discharge activity at the contact imperfections, rather than the main electric field configuration between the large area electrodes or the semiconductor wafer properties. On the other hand, the characteristics under a pillar system is mostly determined by the semiconductor wafer properties and is more reproducible than the results obtained under a parallel system. But when the contact imperfections are remedied by better mounting techniques, the pre-breakdown currents under a parallel system for a good quality wafer indicates lower currents for the same applied voltage than that in a pillar system. Thus the ohmic to quasi-ohmic regime of safe operation limit for the Si wafer can be extended to higher average fields by using a parallel electrode system, provided the semiconductor quality as well as the contact conditions are favorable. Modifying the contact profile from sharp corners to one with rounded corners significantly improves the high field performance of the Si wafers as a result of the reduction in the field enhancement. In fact, it is observed that the highest field for the inception of non-ohmic

response for a Ni/Cr/Au contact Si wafer (≈ 75 kV/cm) is obtained with rounded contact corners under the pillar electrode system. Hence, even though the parallel electrode system seems to be the better suited geometry for high field operation of the PCPS, the practical difficulties for the system implementation outweigh the advantages due to the uniform field configuration.

Acknowledgments

The support to this work by the BMDO / ONR is gratefully acknowledged.

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OBSERVATIONS FROM FIELD PLOTS ON SILICON WAFERS

- [1] The E-fields given the plots must be in V/m and not in V/mm !
- [2] From #16, the local field enhancement at the contact edge under PHE, is present only upto about 0.5mm away from the contact, after which the field is approximately equal to the average field of 200 V/mm (or 200 kV/m). Considering a field enhancement factor of ≈ 20 at 10^{-3} mm away from the contact, the field at that point is ≈ 4000 V/mm (200×20).
- [3] For the PPE system, (from #27), the field drops down from ≈ 3000 V/mm [200×15 (enhancement factor)] at 10^{-3} mm away from contact, to the average field of 200 V/mm at ≈ 0.4 mm away from the contact.
- [4] The ratio between the field enhancement factors under PHE and PPE systems at two different locations:

Distance, mm (from contact)	Enhancement factor (PHE)	Enhancement factor (PPE)	Ratio of Enhancement Factors (PHE./ PPE)
10^{-3}	22.2	14.7	1.5
10^{-2}	5.6	4.4	1.3

$$\text{Average Ratio} = (1.5 + 1.3) / 2 = 1.4$$

- [5] The experimental applied electric field vs current characteristics of a Si wafer under PHE and PPE systems, can be corrected based on the above ratio; the effective applied electric field under PHE is assumed to be 1.4 times higher than that under PPE system. Hence the electric field under the PHE is multiplied by 1.4 for comparing with the current characteristics under the PPE system. As observed from the figure below, the currents corresponding to the corrected field under PHE system matches fairly closely with that under PPE system, indicating that the computed field enhancement factors agree with the experimental results.

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