Alternative Fabrication Techniques for High-Efficiency CuInSe_2 and CuInSe_2 -Alloy Films and Cells

Final Subcontract Report
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PREFACE

This is a final report of research carried out from March 1, 1990, through August 20, 1992, under subcontract XG-0-10017-1 to the University of Illinois at Urbana. The principle investigator is Angus Rockett. Much of the work during the course of this contract continued efforts begun under SERI contract XL-7-06031-9 and its predecessors. The focus of this project has been on development of improved solar cell performance and manufacturability. Parallel efforts supported by the Electric Power Research Institute and the Department of Energy Office of Basic Energy Sciences concerned development of the hybrid sputtering and evaporation process and the microstructural and microchemical characterization of epitaxial single crystals of CuInSe_2 , respectively. The program has continued after the termination of subcontract XG-0-10017-1 under support of the Electric Power Research Institute and with new support from the Universities Program of the National Renewable Energy Laboratory.

We are very grateful for the support of this program by all of the above mentioned agencies.

We further wish to acknowledge the Institute for Energy Conversion at the University of Delaware that fabricated the solar cells described herein.

SUMMARY

Work performed during the course of this subcontract has led to improved CuInSe₂ (CIS) processing techniques and materials resulting in improved solar cell performance (up to 10% active area efficiency) based on a thick conductive evaporated CdS window layer and an indium-tin-oxide transparent conductor. Modeling of the device performance has indicated that an optimal CdS thickness should exist if pinholes occur in the CIS layer (for example, due to adhesion failures) leading to shunts between the CdS and the back contact. Pinholes in the CIS layer have been dramatically reduced by the use of a Cu-Mo two-phase back contact metallization resulting from significant increases in adhesion between the CIS and the back contact. Controlled leaching of the Cu from the back contact apparently contributes to this improvement without degradation of the solar cells. Finally, CIS has been grown epitaxially on GaAs. Preliminary results suggest explanations for the morphology and defect structures of polycrystalline layers used in devices as well as indicating the general mechanism for growth of CIS by vapor phase methods.

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Introduction

The work described below concerned the fabrication of solar cells based on CuInSe_2 (CIS) deposited by a hybrid sputtering and evaporation method. In this method CIS was deposited from magnetron sputtered Cu and In fluxes and evaporated molecular Se. The depositions were conducted in a 40cm-diameter, stainless steel vacuum system described elsewhere.¹⁻⁴ The system is pumped with a 250 L/s turbomolecular pump backed by a mechanical pump. The base pressure of the system was 1×10^{-4} Pa (1×10^{-6} Torr). Polycrystalline CIS films were deposited on $25 \times 25 \times 1.2$ mm, Corning type 7059 borosilicate or common soda lime glass substrates which were typically coated with Mo or a Cu-Mo mixture by magnetron sputtering.

Glass substrate preparation consisted of spraying with a detergent solution followed by a 300 second deionized water rinse and 300 second spin dry cycle in a substrate rinser/dryer. Epitaxial layers were deposited on GaAs as described below. The initial GaAs substrate preparation consisted of solvent and deionized water rinses. The final preparation was carried out as described below.

The experimental results discussed here have been described in more detail in proceedings of the 21st², 22nd³, and 23rd⁴ IEEE Photovoltaic Specialists Conferences and in a patent application concerning the Cu-Mo contact metallization, which is currently under review by the US patent office.

The original proposal requesting funding for this project cited four tasks: 1) demonstration of repeatable high-performance solar cells by the hybrid process, 2) aspects of hybrid process scale up, 3) characterization of solar cells and materials, and 4) modeling of solar cells and materials. The

results presented below address these four issues. Solar cells were produced according to the performances specified in the deliverables of the contract. Process scale up issues addressed primarily concerned improvement of adhesion of the deposited layer to the substrate. This involved development of a novel back contact metallization consisting of a Cu-Mo mixture. (Achieving improved adhesion is essential to viable large scale production of CIS solar modules by the hybrid process or any other method, see Reference 5.) Epitaxial CIS was deposited on GaAs to assist in understanding the physical vapor deposition of CIS and the general aspects of CIS surface morphology evolution and bulk defect formation. The epitaxial and polycrystalline CIS films were characterized by various methods to determine the structural features underlying device performances. Finally, a computational simulation of CIS devices was developed to help understand how adhesion failures can lead to degraded device performances and how this can be improved by optimizing the thickness of the CdS window layer.

RESULTS

Solar Cell Results

While the bulk of the effort over the course of the current contract was directed at understanding fundamental issues in the production and operation of CIS-based solar cells, significant improvements in device performance using our CIS were achieved. The composition of CIS layers on which solar cells were fabricated ranged from Cu-rich to In-rich, although active devices were only produced on In-rich material. All layers used for devices were deposited as bilayers. The initial layers were strongly Cu-rich (>30% Cu) and were covered by strongly In-rich films

(>29% In). The content of the other components of the CIS was found to follow a tie-line on the ternary Cu-In-Se phase diagram connecting Cu_2Se with In_2Se_3 . The Cu-rich layers were deposited at 300-400°C. The In-rich layers were deposited at 350-450°C and both layers were completely intermixed after deposition as determined by SIMS depth profiling. Device quality layers were always deposited at substrate temperatures of at least 350°C for the Cu-rich layer and at least 400°C for the In-rich material. Deposition of bilayer films with net In-rich compositions at higher temperatures (>400°C) on Mo resulted in severe adhesion problems. The use of Cu-Mo metallizations to reduce adhesion failures and results comparing the adhesion of CIS on Mo and on Cu-Mo two-phase mixtures is described below. The performances of the best solar cells based on CIS deposited at the University of Illinois as a function of time are shown in Figure 1 and reflected an increase in all device parameters, as indicated in Table I. The development of the Cu-Mo metallization also led to an improvement in the uniformity of the resulting device performances as discussed below.

We feel that the final active area performance achieved (10%) is close to the maximum value expected for routine device production at the Institute for Energy Conversion at the University of Delaware (IEC) where all devices reported here were fabricated. Test cells were produced by evaporation of 1.7 μm of $\text{Cd}_{0.9}\text{Zn}_{0.1}\text{S}$ with a sheet resistance of 50 Ω/square . This was coated with 180 nm of sputtered indium tin oxide and finished with Ni bus-bar contacts. The device active areas were $\sim 0.08 \text{ cm}^2$. Furthermore, devices based on pure CIS (no Ga) tend to fall below 13% efficiency even with thin CdS window layers and ZnO transparent conductor top contacts. Further improvements can probably be achieved

using alloy materials and with an optimized window layer and transparent conductor structure. We wish to express our appreciation for the efforts of Robert Birkmire, William Schaffarman, and other collaborators at IEC for all of their efforts in producing the devices reported here.

Table I: Device Parameters for Some Devices Produced at IEC from CIS Deposited at the University of Illinois

V_{oc}	I_{sc}	FF	Efficiency
mV	mA/cm ²	%	%
348	32.9	55.0	7.7
392	33.9	63.1	8.4
426	35.3	66.5	10.0

To analyze the performance issues associated with the above solar cells, and in particular to determine the relationship among shunt areas due to adhesion failures and the CdS film thickness and resistivity, we developed a model of Mo/CIS/CdS devices using the SPICE computer program. The device model assumed two parallel top contacts to the edges of a 1cm x 1cm device containing regions shunted to a back contact underlying the entire device area. The shunt was assumed to connect the CdS window layer to the back contact. The active areas of the device were simulated as a current source in parallel with a diode. The window layer, back contact, and transparent conductor were assumed to act as simple resistors. The resistance of the window layer was assumed to scale with the CdS resistivity and the layer thickness. A schematic diagram of the simulated structure and the simulation results are shown in Figure 2.

Using the model, it was determined that there should be an optimum CdS thickness which would increase with increasing fraction of the surface shunted. Different spatial arrangements of shorted and non-shorter areas were compared. No difference in the optimization of the CdS thickness was found using small dispersed shunts as compared to large shunted regions as long as the total shunted area fraction was fixed. It was also not important that the shunt be far from one of the contact bars. The maximum output power showed a peak for all shunted areas studied. Only a modest decrease in performance was found for shunted areas up to ~2% of the total area if the CdS thickness was optimized for that shunted area. However, significant decreases in performance were observed when the window thickness was far from optimal. (Note: while the CdS resistivity used in these simulations was $1000\Omega\text{-cm}$, a new set of curves could be generated in a similar manner for other CdS resistivities.)

Cu-Mo Back Contact Structures

In previous experiments we had observed that optimal device performance was generally obtained under conditions leading to extreme adhesion failure rates (net slightly In-rich layers deposited at temperatures above 400°C). Furthermore, replacing the borosilicate glass substrates with soda lime glass did not improve the adhesion significantly. These problems forced consideration of alternate back contact materials. To achieve optimal adhesion there should be a strong chemical and mechanical bond between the substrate and the film. Because, for our deposition process, the CIS generally shows a dramatic loss of adhesion when it becomes In-rich, a concentration gradient should also be established between the front and back surfaces of the film. To achieve

these objectives a back contact consisting of cosputtered Cu and Mo was deposited at room temperature. The equilibrium phase diagram shows no miscibility between Cu and Mo. Hence, this contact should have met the above criteria if the Cu was confined to small regions interspersed among the Mo grains such that Cu was partially leached from the back contact as deposition proceeded. This should have kept the back surface of the film Cu-rich even in the presence of excess In at the surface. It also provided a material (Cu) to which a strong chemical bond was made. Mechanical stress in Mo films often contributes to adhesion failures. Hence, the soft Cu in the back contact may have contributed to the improved adhesion by plastically deforming to reduce stress in the metallization. Finally, the leached areas convoluted the interface between the contact and the CIS which should have increased the mechanical interlocking contribution to adhesion. (A detailed analysis of the process of improved adhesion has been completed since the completion of this subcontract and the results are described in reference 6.)

Cu-Mo contact metallizations for CIS solar cells were produced by magnetron sputtering of composite targets. For flexibility in process development, strips of Cu foil were soldered to a Mo target using In. Two target compositions were tested with different sizes of Cu strips to adjust the Cu content in the deposited film. Indium solder was used because unintentional incorporation of In into the contact metallization would not degrade the CIS layer deposited subsequently. The deposited Cu-Mo films had compositions of 0, 22, and 30% Cu when the fractional area of Cu on the target surfaces was 0, 33, and 46%, respectively. No In contamination was detected by SIMS in the metallizations. The deposited films were analyzed by SEM and EDX and had CIS layers deposited on top for adhesion

testing and device fabrication. Adhesion was studied by tape tests and by analysis of failures in completed device structures.

CIS deposited on Cu-Mo layers with 22% Cu showed no significant improvement in adhesion. However, a large improvement was observed for metallizations with 30% Cu. The surface morphology of the 30% Cu films was indistinguishable by SEM from the morphology of pure Mo deposited at the University of Illinois and elsewhere. Cross sectional fractograph studies showed identical columnar microstructures in both the Mo and Cu-Mo films suggesting that the Cu did not significantly affect either the grain size or shape of the predominant Mo. Furthermore, there were no large Cu grains visible on the as-metallized surfaces suggesting that the Cu was distributed in the metallization rather than precipitated in large chunks. For CIS deposited by the hybrid process, there was no detectable change in the Cu content of device layers deposited at a maximum temperature of 400°C, as measured by EDX. This indicated that the total amount of Cu leached out of the substrate was a small fraction of the amount in the back contact layer. A fracture cross section of CIS on pure Mo showed an exposed Mo region ~5 μm wide around the fracture edge where the CIS had failed to adhere and had flaked away during the fracture. On Cu-Mo samples the CIS fracture face was coincident with the Cu-Mo and glass fracture faces.

Tape adhesion tests were carried out for CIS films on pure Mo layers deposited on Corning 7059 and soda-lime glass as well as on Cu-Mo layers on 7059 and soda lime glass. The tape was common Scotch-brand tape applied with moderate finger pressure. Virtually complete failure of the interface adhesion was observed for CIS on pure Mo metallizations on both the Corning 7059 and soda lime substrates on the first tape applied. CIS

films deposited on Cu-Mo layers exhibited only minor failures around the edges of the metallization after two tape applications. Some of the test tapes are shown in Figure 3. Adhesion failures in completed solar cell device structures were similarly reduced.

The improved adhesion also strongly affected the uniformity of performance of solar cells. Figure 4 shows the relative performances of 12 cells fabricated on each of two 25 x 25 mm substrates, one coated with pure Mo and the other with a Cu-Mo metallization. To reduce questions of reproducibility the performances are for the best results obtained to date on each metallization (8.4% efficiency on Mo and 10.0% on Cu-Mo). The significant improvement in uniformity of the devices on the Cu-Mo substrate was not due to changes in compositional uniformity, which was ± 2 atomic % for Cu and In across the 25 mm substrate in both cases. The improved uniformity apparently resulted from a reduction in adhesion failures.

Epitaxial Growth of CIS

Single crystals of CIS were successfully deposited on GaAs substrates as demonstrated by electron channeling patterns. Growth defects were observed and characterized. These provided important insights into the growth mechanisms for both single crystal and polycrystalline CIS. The principal growth defects were pits in the surface of Cu-rich layers, small islands or ripples on the surface of most In-rich films, and voids at the interface between the CIS and the GaAs substrate. Second phase precipitates of Cu-containing phases and arsenides were found in the CIS layers near the interface.

The most critical step in controlling surface pit formation was the substrate cleaning and outgassing process in the hybrid chamber. It was found that heating GaAs samples in the presence of a Se flux led to irregular etching of the GaAs surface and pit formation. Residual Se was also observable on the GaAs surface after this procedure. Consequent roughening of the substrate surface led to a network of overlapping pits or islands in the epitaxial layers. Minimization of Se pressure in the substrate area prior to growth reduced pitting and improved the surface morphology of the CIS layers. To minimize exposure to Se, substrates were heated to the growth temperature over approximately 30 minutes with both the Se shutter and the main growth shutter closed. During heating the metal targets were sputter cleaned at a low current. As the substrate approached the growth temperature the Se source was heated. To initiate growth the target currents were raised to growth values for five minutes, the Se shutter was then opened, and finally the main shutter was opened. In-rich epitaxial layers grown on surfaces prepared in this way showed rectangular pits when grown on (001) GaAs and triangular islands when grown on (111)B GaAs, consistent with (112)-type facet planes. Cu-rich layers showed a network of interconnected pits in all cases. When the Cu-rich CIS surface was (112) oriented, the side walls of the networks were vertical suggesting (110)-type facets while (002)-oriented layers had networks of facets both normal to the surface and inclined at an angle of approximately 60°. This implies that pits in Cu-rich films include (110) and/or (112)-type facet faces.

It was found that the surface defect density was further reduced by prebaking the substrate holder for approximately 30 minutes at 500 °C prior to mounting the GaAs substrates. This probably removes residual Se

from the substrate holder. Although the pit density could be reduced by this preparation process, pits could not be eliminated from the Cu-rich films.

In-rich layers exhibited much more perfect surfaces when the initial substrate surface was smooth, as shown in Figure 5. Rather than pits, these In-rich films exhibit islands or ridges. The (112)-oriented films have very smooth surfaces with isolated triangular pyramidal islands. The island density was typically less than $\sim 70 \text{ cm}^{-2}$ with the islands roughly $3 \text{ }\mu\text{m}$ on a side. On GaAs (001) the surface exhibited small highly anisotropic ripples aligned along one of the (110) directions, with a spacing of roughly $0.33 \text{ }\mu\text{m}$.

The asymmetry of pits on the (002)-oriented surfaces and the structure of the pits on the Cu-rich (112)-oriented surfaces suggest that the facet faces are (112)-type and that a strong preference for either the metal-terminated (less likely) or Se-terminated (more likely) facets exists. Any rectangular pit on CIS (002) with (112) facets will have two sides terminated with metal atoms and two terminated with Se atoms. The elongation of the pit along one direction results from a preference for the type of surface termination on that side. It is striking that on the Cu-rich layers pits form while on the In-rich material islands result. Since all GaAs (111)B growth surfaces were As-terminated it is most likely that the CIS nucleates with the Se-terminated face. (Results post-dating this subcontract confirm that the Se-terminated face is favored.)

CIS was shown to affect the GaAs surface from fracture cross sections of the deposited layers after growth. These cross sections show pyramidal crystallographic pits in the GaAs near the interface although the lower CIS surface is flat. This can only occur if the GaAs surface on which the CIS

originally nucleates is flat and if the voids form at the interface during growth. Void formation can result from interdiffusion across the interface (Kirkendall voids). Voids were only found for CIS on GaAs (001). Second phases were found at the interface between CIS and GaAs (111). To examine the possibility of interdiffusion causing Kirkendall voids, SIMS profiles of the samples were obtained. Figure 6 shows a SIMS profile along with a fracture cross section of the substrate and epitaxial layer showing both the smooth CIS lower surface and the underlying voids in the GaAs. Substantial interdiffusion has occurred across the heterojunction. In particular, Ga is found in the CIS epitaxial layer while Cu, In, and Se are all found in the substrate.

Voids are common in a layer extending roughly 170 nm into the substrate. There is an abrupt decrease in indium concentration at the original heterointerface with both Cu and Se extending across the voided region at relatively unchanged levels. It is clear that Cu and Se and, to a lesser extent In, diffuse into the substrate. Simultaneously, Ga diffuses outward into the CIS layer during growth. Relatively little As outdiffusion was observed by SIMS. The presence of Cu, In and Se in the substrate stresses the GaAs. Substantial strain fields were observed in the substrate by TEM. These cause local changes in the fracture properties of the GaAs. A modified fracture zone is evident in fracture cross sections as much as 500 nm below the interface, as shown in Figure 6.

The diffusion of large amounts of Ga into the CIS layer at the growth temperature resulted in supersaturation as the film was cooled. Some of the Ga then precipitated out of solution with the small amount of As present to form occasional GaAs crystallites in the CIS near the heterojunction. Cu-rich second phases have also been identified within the

matrix of the epitaxial layers. Coherent precipitates were observed at the CIS/GaAs heterojunction. Preliminary cross-sectional TEM analyses indicated that these precipitates may have hindered the interdiffusion giving rise to the Kirkendal voids or may have formed as a result of interdiffusion upon cooling the sample to room temperature after growth. They can not have affected the initial phases of the epitaxial growth since the CIS is a high quality single crystal and the lattice planes of the CIS are aligned with the GaAs lattice planes across the precipitates. Kirkendal voids were only observed in the interfaces between GaAs (001) and CuInSe₂ (002). Interfaces with GaAs (111) did not show these voids.

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Figure 1. The maximum conversion efficiency of solar cells based on CIS deposited at the University of Illinois as a function of time.

Figure 2. A schematic diagram of the device structure simulated with SPICE and the simulation results for power output as a function of CdS thickness and shunted area.

Figure 3. The results of tape tests for films on Mo and Cu-Mo metallizations. (A): CIS on pure Mo on borosilicate glass, (B) CIS on pure Mo on soda lime (slide) glass, (C) CIS on $\text{Cu}_{0.3}\text{Mo}_{0.7}$ on borosilicate glass.

Figure 4. Comparison of the relative performances of solar cells on 25 x 25 mm substrates as a percentage of the efficiency of the best device on each substrate. The best performances are 8.4% on Mo and 10.0% on Cu-Mo.

Figure 5. SEM micrographs of the surface morphology of In-rich (left) and Cu-rich (right) epitaxial layers grown on GaAs (001) (top) and (111) (bottom).

Figure 6. A SIMS profile (lower section) of a (112)-oriented slightly In-rich CuInSe_2 film deposited on GaAs (111). A fracture cross section SEM image of a corresponding area of the sample is also shown (upper portion).

Figure 3

Uniformity on a 25mm x 25 mm sample:

Devices on pure Mo
(film 6711C)

Devices on Cu-Mo
(film 6801-B)

Figure 5.

Figure 6. A SIMS profile (lower section) of a (112)-oriented slightly In-rich CuInSe_2 film deposited on GaAs (111). A fracture cross section SEM image of a corresponding area of the sample is also shown (upper portion).

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13. ABSTRACT (Maximum 200 words) This report describes work performed during the course of a subcontract and which has led to improved CuInSe ₂ (CIS) processing techniques and materials resulting in improved solar cell performance (up to 10% active-area efficiency) based on a thick conductive evaporated CdS window layer and an indium-tin-oxide transparent conductor. Modeling of the device performance has indicated that an optimal CdS thickness should exist if pinholes occur in the CIS layer (for example, due to adhesion failures) leading to shunts between the CdS and the back contact. Pinholes in the CIS layer have been dramatically reduced by using a Cu-Mo two-phase back contact metallization resulting from significant increases in adhesion between the CIS and the back contact. Controlled leaching of the Cu from the back contact apparently contributes to this improvement without degrading the solar cells. Finally, CIS has been grown epitaxially on GaAs. Preliminary results may explain the morphology and defect structures of polycrystalline layers used in devices as well as indicating the general mechanism for growth of CIS by vapor phase methods.					
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