A MINIATURIZED ASIC-BASED MULTICHANNEL SCALER INSTRUMENT*

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Abstract

A miniaturized multichannel scaler instrument has been developed to address size and operational constraints for data acquisition in a portable laser-induced luminescence system. The multichannel scaling (MCS) function is implemented as a programmable application specific integrated circuit (ASIC) with standard interfaces for control and data acquisition. The instrument is microcontroller-based with sufficient computing power for data manipulation and algorithmic processing. The unit includes electronics for laser control, and amplification and pulse height discrimination of PMT pulses. Modification of the instrument should allow use in nuclear, chemical, and spectroscopy related applications including Mossbauer experiments[1,2]. Interfaces are incorporated allowing both computer-controlled and stand alone operation. Implementation of the MCS function as an ASIC and comparison with conventional implementations are discussed. Full characterization of the MCS is presented including differential non-linearity (DNL), bin dead time, and bandwidth measurements.

I. INTRODUCTION

Commercially available multichannel scaling instruments can be too costly or physically large for use in many stand-alone monitoring systems or for field operations requiring portability [3,4]. Additionally, many commercial instruments provide functions not required in specific applications that contribute to the cost and size of the units. A programmable but functionally reduced MCS instrument miniaturized to allow for portability and use in size-restricted environments has been developed to address these issues. The instrument was specifically designed for determining environmental uranium concentration levels in ground water monitoring applications, with sufficient sensitivity to analyze low-level process streams and effluent. The analysis method employed is based on phosphorescence decay techniques thoroughly covered in published literature [5].

The instrument is microcontroller-based allowing it to be used as either a PC-controlled or stand alone unit. A user interface is provided that allows the operator to scroll through

menus and select desired functions. Sufficient computational power exists to provide data manipulation including cycle accumulation (stacking) and algorithmic processing.

A key feature of the instrument is the implementation of a programmable high-performance multichannel scaler as an ASIC. The use of ASIC technology provides several key benefits including reduced physical size, increased reliability, and reduced manufacturing costs. Additionally, scaling characteristics including count rate, differential non-linearity, and bin dead time are optimized by using this technology and the architecture specific to this chip.

II. DESIGN METHODOLOGIES

The design of this instrument was approached with careful consideration of the primary design objectives: programmability, flexibility allowing adaptability to various experiments and measurement applications, and miniaturization. Use of a microcontroller unit for instrument control allows a variety of control and data manipulation functions and will accommodate software changes for future applications. Blocks of the instrument were designed with standard interfaces to allow reconfiguring with other modules. The use of ASIC technology has led to a miniaturized, reliable, cost-effective circuit implementation. Additionally, the incorporation of a programmable ASIC with standard interfaces for control and data acquisition allows a wider range of target applications.

III. INSTRUMENT DESCRIPTION

A block diagram demonstrating the instrument as used in a typical time-resolved luminescence experiment is shown in Fig 1. The unit contains a pulse conditioning front-end that interfaces directly to the PMT and provides amplification and pulse height discrimination of input pulses. A level translator circuit translates the ECL level pulses from the discriminator to CMOS levels for the MCS chip. Time-resolved counting is performed in the MCS ASIC, and time bin information is stored in FIFO memory for retrieval by the microcontroller. Interfaces for computer control and stand-alone operator control are provided.

The pulse conditioning module performs amplification and pulse height discrimination of PMT pulses, and translation of the pulses to CMOS levels for counting by the MCS ASIC. The PMT preamplifier was designed for 50 Ω input and

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Fig.1 Multichannel Scaler Instrument Block Diagram

output impedance, with a nominal gain of 40. Typical rise and fall times are 1ns, allowing operation frequencies in excess of 200 MHz. This circuit module was implemented using surface mount technology (SMT) for miniaturization and improved performance, and requires an area of only 1 in². Pulse height discrimination is accomplished using an AD96685 ECL comparator. A level shifting circuit, also implemented using SMT, converts the pulses to CMOS compatible levels for counting.

A single board microcontroller module acts as the control and data acquisition interface between the multichannel scaler ASIC and the host computer. This unit is composed of an Intel 80C51 family microcontroller, 32 Kbytes read only memory (EPROM) for program storage, 32 Kbytes of static random access memory (SRAM) for acquisition data storage and manipulation, an 8 Kbyte EEPROM for result storage, an LCD display interface and push-button interface to facilitate user control, and a hardware selectable RS232/422/485 interface for computer controlled operation.

IV. MCS ASIC

The MCS ASIC was designed to fully implement a set of multichannel scaling functions. The following programmable functions were incorporated: bin width (dwell time) of 250ns, 500ns, 1 μ s, 2 μ s, or 4 μ s; programmable number of bins: 8, 16, 32, 64, 128, 256, 512, or 1024; and trigger delay of 0 to 1024 μ s, programmable in 1 μ s increments. Other features including standardized interfaces were incorporated into the ASIC to further maximize the flexibility of the chip and to facilitate its use in other instruments and applications.

An architectural block diagram of the ASIC is demonstrated in Fig. 2. The chip is composed of three primary functional modules: control, timing, and counting.

The control block serves as the interface between the ASIC and the microcontroller and is used to transfer all programming and control information. This module is composed of three read and three write registers that are

memory-mapped into the microcontroller external data memory. During a write operation, all three registers appear as control registers. When a read command is performed, two registers allow reading of programmed parameters, and the third register allows the microcontroller to check the ASIC acquisition status.

Fig. 2 Multichannel Scaler ASIC Architectural Block Diagram

The timing block is composed of the timebase control, delay generator, state machine and bin depth counter modules. A timebase is fed into the timebase control which generates the proper frequencies for the delay generator and state machine. The delay generator implements the programmed delay and the resulting signal is used to enable the state machine. The state machine provides precise control signals to the rest of the ASIC, namely the counters and the FIFO module. The bin depth counter determines the number of time bins that have passed, and disables the timebase control when the preloaded number of time bins has passed.

The counting module performs the actual counting of input pulses and supplies the count result to the FIFO interface for storage. This module is based on three recirculating 8-bit counters that are precisely controlled to minimize bin dead time and DNL associated errors. While one counter is performing the counting function associated with one time bin, the other counters are emptying their contents and initializing for upcoming counting bins. The FIFO write control routes the proper latched counter result to the FIFO interface and supplies a clock signal for writing the result into the memory unit. Thus, the FIFO writing operation is performed 'on-the-fly' while the data acquisition is taking place, allowing for fast and efficient operation without microcontroller intervention.

A typical data acquisition cycle is performed by the microcontroller first programming all experiment specific parameters through the ASIC control registers. All control register contents are preserved from one acquisition cycle to

the next requiring only new setup parameters to be loaded after the initial programming of the ASIC. The ASIC is reset by toggling the master reset (MRS) bit in the ASIC control register 1, and the chip is armed by setting the arm (ARM) bit in the same register. At this point the ASIC is configured and ready for a trigger. The microcontroller issues laser trigger that fires and laser and is used by the ASIC to properly synchronize the data acquisition. This trigger enables the timebase to the chip and the programmable delay generator counts off the programmed time interval. Upon completion of the delay, the timebase is enabled to the ASIC state machine that generates the control signals for the recirculating counters and the FIFO interface. Synchronous with counting, bin data is available 'on-the-fly' at the FIFO interface and a clock signal is provided for writing data. The bin depth counter compares the number of bins that have passed to the previously programmed value, and generates a stop signal when the proper number of bins have passed. This signal is used to halt the chip after the correct number of bins have passed and associated data written to the FIFO memory. The microcontroller is provided with an end of conversion signal (EOC) that is asserted when a laser trigger is issued, and de-asserted when the last bin information is written to the FIFO memory. Thus, after setup and triggering the ASIC runs independently and notifies the microcontroller when the acquisition cycle has finished allowing the microcontroller to perform other functions while the multichannel scaling is taking place.

Use of a precisely controlled recirculating counter architecture implemented as a single monolithic system provides many important benefits. A noticeable improvement in scaling parameters such as bin dead time, differential non-linearity, and pulse counting rate over many recent designs are observed [3,7]. Errors caused by delay paths are minimized using entirely monolithic interfaces between circuit modules. An increase in counting speed will be noticed which will improve the dynamic range of the MCS unit and decrease statistical errors associated with dead time correction and pulse pair rejection. Additionally, some obvious physical benefits including reduced size and improved reliability are inherent to monolithic construction.

V. EXPERIMENTAL RESULTS

The MCS ASIC was fabricated in $2\ \mu\text{m}$ CMOS using MOSIS and is shown in Fig. 3. A complete characterization of this chip was performed using both commercial ASIC test equipment and a benchtop prototype of the MCS instrument. The results are summarized below.

- Input Count Rates Exceeding 200 MHz (ASIC only)
- Bin Width (250 ns, 500 ns, 1 μs , 2 μs , 4 μs)
- Bin Depth (8, 16, 32, 64, 128, 256, 512, 1024 bins)
- Trigger Delay (0 to 1024 μs in 1 μs increments)
- Standard Microcontroller Interface for Programming and Control

- Standard FIFO Interface for Data Storage 'on-the-fly'

Bin differential non-linearity (DNL) was measured as 1.34% for 250 ns bins with approximately 30,000 counts per bin. All chips tested counted properly for continuous input count rates over 200 MHz resulting in a pulse pair resolution $< 5\text{ns}$. Though the gating signals of the counters are precisely controlled to virtually eliminate dead time, an anomaly in the enabling scheme allows a pulse occurring during a transition of two time bins to fall into both bins. However, this situation will allow no more than one pulse to occur in two adjacent bins and in essence increases the effective width of each time bin slightly. A redesigned version of the ASIC that incorporates a corrected edge-triggered gating method will improve this performance.

Fig. 3 Multichannel Scaler ASIC ($4.8\mu\text{m} \times 4.8\mu\text{m}$)

A complete, portable multichannel scaler instrument that incorporates the MCS ASIC and support electronics, a nitrogen laser for sample excitation, 4 chamber cuvette holder, PMT, and battery supply packaged in a suitcase size enclosure was built and tested (refer to Fig. 4). A sample of data acquired using a 10 ppb uranium water sample with 1024 1 μs time bins stacked 5000 times is shown in Fig 5.

VI. CONCLUSIONS

An ASIC-based miniaturized multichannel scaler instrument designed for portability has been introduced. The multichannel scaling function has been implemented as a programmable ASIC with standard interfaces for control and data acquisition. Tests performed on the ASIC indicate full functionality including low DNL (1.34%) and high counting rates ($> 200\text{MHz}$). A complete instrument has been developed around the ASIC providing a portable instrument solution for laser induced luminescence decay experiments.

The incorporation of a programmable multi-function MCS ASIC and microcontroller, and standard interfaces for data

testing. We also thank Curtis Currie, Norma Hensley, and Teri Subich for assistance in preparing this paper.

Fig. 4 Portable Multichannel Scaler Instrument

acquisition and control, allow this instrument to be retrofitted for application in a number of different experiments. Modification of this unit should allow use as an airborne uranium monitor, remote surface and subsurface water monitor, dedicated urine analyzer, non-contact temperature measurement unit, and a variety of other spectroscopy-related applications including Mossbauer experiments.

Fig. 5 Phosphorescence Decay Curve for a 10 ppb Uranium Sample

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