Gallium Arsenide-Based Ternary Compounds and Multi-Band-Gap Solar Cell Research

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ABSTRACT

The aim of this contract is the achievement of a high-efficiency, low-cost solar cell. The basic approach to the problem is centered upon the heteroepitaxial growth of a III-V compound material onto a single-crystal silicon wafer. The growth technique employed through out this work is metalorganic chemical vapor deposition (MOCVD). The silicon wafer may serve as a mechanical substrate and ohmic contact for a single-junction device, or may contain a p-n junction of its own and form the bottom cell of a two junction tandem solar cell structure. The III-V material for the single-junction case is GaAs and for the two-junction case is either GaAlAs or GaAsP, either material having the proper composition to yield a band gap of approximately 1.7 eV. Results achieved in this contract include the following: (1) a 17.6% efficient GaAs-on-Si solar cell; (2) an 18.5% efficient GaAs-on-Si concentrator solar cell at 400 suns; (3) a 24.8% efficient GaAs-on-GaAs solar cell; (4) a 28.7% efficient GaAs-on-GaAs concentrator solar cell at 200 suns; (5) measurement of the effects of dislocation density and emitter doping on GaAs cells; and (6) improvements in the growth process to achieve reproducible thin AlGaAs window layers with low recombination velocities and environmental stability.

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SECTION 1.0 INTRODUCTION

1.1 PROGRAM GOAL

The aim of this contract is the achievement of a high-efficiency, low-cost solar cell. The basic approach to the problem is centered upon the heteroepitaxial growth of a III-V compound material onto a single-crystal silicon wafer. The growth technique employed throughout this work is metalorganic chemical vapor deposition (MOCVD) in a reactor which has been described previously [1]. The silicon wafer may serve as a mechanical substrate and ohmic contact for a single-junction device, or may contain a p-n junction of its own and form the bottom cell of a two-junction tandem solar cell structure. The III-V material for the single-junction case is GaAs and for the two-junction case is either GaAlAs or GaAsP, either material having the proper composition to yield a band gap of approximately 1.7 eV.

1.2 PROGRAM HISTORY

This work is a direct continuation of previous SERI-funded efforts which began in 1980. Under the previous contracts, the following achievements have been made:

- Startup and characterization of a new MOCVD reactor for the growth of GaAs, GaAlAs, and GaAsP on five two-inch diameter substrates with excellent uniformity.
- Optimization of the growth of Ge films on Si by a simple CVD technique.
- Production of a 9% efficient GaAs-on-Ge-on-Si solar cell.
- Much advancement in the understanding of the GaAs-on-Si growth process and in the quality of grown films.
- Production of a 15.2% efficient GaAs-on-Si solar cell.
- Characterization of atomic hydrogen passivation of GaAs-on-Si solar cells.
- Development of a GaAsP-on-GaAs growth technology.
- Production of a 17.8% efficient GaAsP (1.7 eV) solar cell on GaAs.
- Production of a 17.7% efficient GaAlAs (1.7 eV) solar cell on GaAs.
- Production of a 23.7% efficient GaAs-on-GaAs solar cell.

- Improvements in cell processing technology, including the use of a double-layer antireflection coating and a new liftoff process for formation of low-loss grid lines.
- Improved theoretical understanding of the loss mechanisms in GaAs-on-GaAs and GaAs-on-Si solar cells.
- Study of the reproducibility of solar cell production (GaAs, GaAlAs, and GaAsP cells) in a research laboratory environment.

1.3 SUMMARY OF RESULTS

Results achieved in this contract include the following:

- Production of a 17.6% efficient GaAs-on-Si solar cell.
- Production of a 18.5% efficient GaAs-on-Si concentrator solar cell at 400 suns.
- Production of a 24.8% efficient GaAs-on-GaAs solar cell.
- Production of a 28.7% efficient GaAs-on-GaAs concentrator solar cell at 200 suns.
- Determination of the effects of dislocation density on GaAs cell efficiency.
- Determination of the effects of emitter doping on GaAs cell efficiency.
- Improvements in the growth process to achieve reproducible thin AlGaAs window layers with low recombination velocities and environmental stability.

The results from the first year are detailed in Chapters 2-5.

SECTION 2.0

MATERIAL STUDIES

A number of experiments aimed at improving the material quality of our GaAs solar cell structures have been carried out. We have studied ways of increasing the cell efficiency of both our GaAs homoepitaxial cells and our GaAs-on-Si heteroepitaxial cell structures.

2.1 LIFETIME STUDY IN GaAs-on-GaAs STRUCTURES

In the case of GaAs-on-GaAs devices, MOCVD growth-parameter-optimization experiments were performed in an attempt to maximize the lifetime in the base as well as minimize the interface-recombination velocity at the emitter-window interface. In this study, time-resolved photoluminescence was used to assess the minority-carrier lifetime of GaAs-GaAlAs double heterostructures grown on GaAs substrates. The work was a collaborative effort among researchers at Spire Corporation (epitaxial growth), SERI (lifetime measurements, data analysis), and the University of Colorado (modelling). In the course of this project, very-high-lifetime GaAs layers and low-recombination-velocity interfaces were achieved. The details of this work are described in a paper submitted to Applied Physics Letters, and a copy of this manuscript is included here as Appendix A.

2.2 LIFETIME STUDY IN GaAs-on-Si STRUCTURES

Much effort has been directed toward improving the GaAs-on-Si minority-carrier lifetime by optimizing the structure and the growth parameters of the buffer region used as a defect-reduction zone placed between the Si substrate and the GaAs solar cell active layers. The results of our recent work in this area have been presented (April 1989) at the Spring Meeting of the Materials Research Society (MRS) and have been submitted for publication in the proceedings from that conference. The following sections present the details of our studies in a format which is a greatly expanded version of the MRS manuscript. The work discussed here is a joint effort between Spire and SERI, and major contributions from M.M. Al-Jassim, K.M. Jones, and R.K. Ahrenkiel are acknowledged.

2.2.1 Abstract

GaAs-on-Si structures have been grown by atmospheric-pressure metalorganic chemical vapor deposition (MOCVD); in some samples, the GaAs nucleation layer was deposited by atomic layer epitaxy (ALE). Material quality has been characterized by Nomarski microscopy, time-resolved photoluminescence, and transmission electron microscopy. The minority-carrier lifetime has been correlated with defect density and growth parameters. The use of a thermal-cycle-growth technique is seen to be a major factor in improving GaAs-on-Si material quality without resorting to the use of thick buffer layers.

2.2.2 Introduction

For many of the applications for which GaAs-on-Si structures are being considered, such as photovoltaic energy conversion and the monolithic integration of GaAs-based optoelectronic devices with Si integrated circuitry, the minority-carrier properties of the GaAs layers are critically important. While there have been numerous reports of the successful fabrication of majority-carrier devices (such as field-effect transistors) from GaAs-on-Si wafers [2], there are far fewer successes reported in the minority-carrier-device segment of the GaAs-on-Si field. This is due mainly to the fact that the presence of the high dislocation density typically found in GaAs-on-Si layers deleteriously affects the minority-carrier material properties (e.g., lifetime) much more severely than the majority-carrier properties (e.g., mobility).

2.2.3 Experimental Procedure

In the present work, we study a number of ways to reduce the dislocation density, and thus improve the minority-carrier lifetime, in MOCVD-grown GaAs-on-Si structures. The examined variables include buffer region thickness, first-layer nucleation process, in situ thermal anneal, and usage of a strained layer.

The test structures studied are shown schematically in Figure 2-1. The three top layers represent the GaAs-AlGaAs double heterostructure (DH) specifically designed for the measurement of lifetime by the photoluminescence (PL) technique described below. All samples are grown by atmospheric-pressure MOCVD in the SPI-MO CVDTM 450 reactor built by Spire. The GaAs-on-Si growth is accomplished by the now popular three-step method outlined here: The Si substrates (oriented 2° off (100) in the $\langle 011 \rangle$ direction) are heated in hydrogen to over 1000°C to remove the oxide, and then the temperature is lowered to approximately 400°C for nucleation and deposition of ~200 angstroms of GaAs; finally, a thick GaAs layer (≥ 1 micron) is deposited at typical MOCVD conditions using a 700°C growth temperature, a 4 micron/hour growth rate, and a V-III ratio of 15:1. In all growths, the source chemicals used are trimethylgallium and arsine, and the n-type dopant gas is silane diluted in hydrogen.

In some runs, the low-temperature layer growth (200 angstroms) is performed by an Atomic Layer Epitaxy (ALE) process described elsewhere [3]. The use of ALE to deposit the nucleation layer in a GaAs-on-Si structure is a new technique in our laboratory and has not yet been optimized. However, it is a very promising method for GaAs-on-Si growth due to its low substrate temperature and two-dimensional nucleation properties. The ALE-based results in this paper are therefore to be regarded as quite preliminary. Higher quality GaAs-on-Si films using the ALE nucleation process have recently been grown and are reported elsewhere [4].

The growth of the GaAs buffer region in some samples utilizes the thermal cycle growth (TCG) process, which involves several repetitions of a deposition-annealing-cooldown cycle as shown schematically in Figure 2-2. In other samples, a thermal cycle annealing (TCA) process is used in which the annealing-cooldown cycles are performed after the entire buffer thickness has been grown. Another buffer-region variable employed in some runs is the use of a single 1000 angstrom-thick layer of GaInAs. Finally, to complete the growth, the DH depicted in Figure 2-1 is deposited on top of the buffer region. In all test runs, the MOCVD chamber is opened and a GaAs control substrate is loaded onto the susceptor at an appropriate point before start of the DH growth.

0.3μm	Al _{.3} Ga _{.7} As	n=1E17cm ⁻³	} DH For Lifetime Tests
4μm	GaAs	n=1E17cm ⁻³	
0.3μm	Al _{.3} Ga _{.7} As	n=1E17cm ⁻³	
0.1μm or 0	(Ga _{.85} In _{.15} As)		Strained Layer or Anneal or None
Varies	Ga As		Std. Growth or TCG
1μm	Ga As		Std. Growth
0.02μm	Ga As		Std. Growth or ALE
25 mils	Silicon		2° Off (100) → (110)

Figure 2-1. MOCVD-grown Test Structures Studied

Figure 2-2. Typical Thermal Cycle Growth Schedule

Nomarski interference-contrast optical microscopy is used to study the surface morphology of the samples. The defect structure and density is analyzed by transmission electron microscopy (TEM) using both planview and cross section modes. Minority-carrier lifetime is measured by the photoluminescence (PL) technique using pulsed dye-laser excitation and time-correlated photon counting; the system is described in detail elsewhere [5], and is briefly outlined below.

The data are obtained using a pulsed dye laser to excite the PL of the device and photon counting [5] is used to analyze the results. A schematic of the experimental set-up is shown in Figure 2-3. Using a beam splitter and a photodiode, a part of the laser pulse is picked off to initiate a START trigger into the delayed coincidence electronics. The START trigger initiates a time-to-amplitude converter (TAC). When a photon-initiated signal is passed by the amplitude discriminator, the latter produces a STOP trigger at the TAC. The TAC output is a ramp with amplitude proportional to the time delay between the laser pulse and the arrival of the first photon. The TAC signal is fed to a multi-channel pulse-height analyzer (MCA). The MCA collects one count per detected photon which is stored in a channel appropriate to the time delay. Thus one count is recorded for every laser pulse. In this way, a profile of the PL decay is built up in terms of counts versus time.

Figure 2-3. Experimental Set-up Used to Measure Minority-Carrier Lifetimes in Double-Heterostructure Samples

2.2.4 Results

2.2.4.1 Surface Morphology

Nomarski microscopy has been used to characterize the GaAs-on-Si samples. Since, in most cases, several runs were used to grow the complete structures of Figure 2-1, the samples were removed and examined at several points in the growth sequence in order to evaluate the effects of the different recipes used in the construction of the buffer region.

Figure 2-4 shows the surface morphology of two 1-micron-thick GaAs-on-Si samples in which the nucleation layer was deposited by two different techniques. Both samples are quite smooth and shiny with no obvious problems at this stage, although the surface features on the two samples do appear to be quite different.

A. Standard nucleation
standard growth

B. ALE nucleation
standard growth

Figure 2-4. Surface Morphology of 1 micron-thick GaAs on Si

The surface morphologies of four samples, each two microns thick, are shown in Figures 2-5A-D. We can see that the TCG process leads to generally smoother surfaces; cross-hatch features, indicative of a reduction in the threading dislocation density, are apparent in the TCG samples, especially in Figure 2-5B. In Figure 2-5 it appears that the ALE-initiated films are slightly rougher than the conventional-growth samples.

A. Standard
nucleation

standard
growth

B. Standard
nucleation

TCG

C. ALE
nucleation

standard
growth

D. ALE
nucleation

TCG

Figure 2-5. Surface Morphology of 2 micron-thick GaAs on Si

Some wafers of the type shown in Figure 2-5 were subjected to the growth of a 1000 angstrom-thick layer of $\text{Ga}_{.85}\text{In}_{.15}\text{As}$; typical morphologies of these are displayed in Figure 2-6. Strong cross-hatch features appear on all these samples, including those with no prior annealing; this indicates that the cross-hatch is due to the lattice mismatch of the GaInAs to the GaAs . All these samples appear generally smooth and shiny to the eye.

Figure 2-6. Surface Morphology of $\text{Ga}_{.85}\text{In}_{.15}\text{As}$ on 2 micron-thick GaAs on Si

Subsequently, a number of samples with a variety of buffer-region designs were used as substrates for the growth of the 4.6 micron-thick DH for the purpose of measuring lifetimes. The surface morphologies of these 6.6 micron-thick structures are all similar to their respective buffer-layer-on-Si substrates except for the appearance of microcracks (see Figures 2-7 and 2-8). It is clear from these two sets of micrographs that the TCG process leads to a somewhat smoother surface morphology and to the presence of cross-hatch features as mentioned above. The ALE-nucleated films appear slightly rougher than those using our conventional low-temperature MOCVD first layer. Thicker DH samples, having a 5 micron GaAs buffer (and thus a 9.6 micron total thickness) have appearances nearly identical to those of the 6.6 micron samples, with strong cross-hatch features again being evident in the annealed samples, as shown in Figure 2-9. All these samples have microcracks at a linear density of 100 per cm. We have shown previously that the presence of such cracks need not be deleterious to the fabrication of solar cells [6].

total thickness = 6.6 μm

A. Standard nucleation
standard growth.

B. Standard nucleation
standard growth
InGaAs

C. ALE nucleation
standard growth

Figure 2-7. Surface Morphology of DH on GaAs on Si with no Buffer Anneals (total thickness = 6.6 microns)

A. Standard
nucleation

TCG

B. Standard
nucleation

TCG

InGaAs

C. ALE
nucleation

TCG

D. ALE
nucleation

TCG

InGaAs

Figure 2-8. Surface Morphology of DH on GaAs on Si with TCG Buffers (total thickness = 6.6 microns)

A. Standard nucleation
standard growth

B. Standard nucleation
TCA

C. Standard nucleation
TCG

Figure 2-9. Surface Morphology of DH on Thick GaAs-on-Si Buffers (total thickness = 9.6 microns)

2.2.4.2 Minority-Carrier Lifetime: Experiment 1

This experiment studies the effects of buffer thickness and annealing. Figure 2-10 shows the lifetime data measured on a number of GaAs-on-Si DH samples. The improvement of lifetime with increasing thickness is obvious; similar effects on other material properties have been previously reported [7]. Figure 2-10 also shows that improved lifetimes result from use of the TCG process as preliminary data has shown earlier [8]. One run in this batch employs the TCA process; this one datum implies that there may be a slight improvement over unannealed layers but more work is needed in this area.

Figure 2-10. Minority-Carrier Lifetime in GaAs on Si

2.2.4.3 Minority-Carrier Lifetime: Experiment 2

Table 2-1 shows the data from a recent experiment aimed at optimizing the material quality without resorting to the use of thick buffer layers which have the drawbacks of increased cracking and wafer bow, decreased surface quality, and increased deposition time. Keeping the total buffer thickness to only 2 microns, we compared the variables shown in Table 2-1. Unfortunately, some unexplained contamination in these runs resulted in low lifetime values for most samples as compared with the results of experiment 1. The growth runs in experiment 2 had stained surfaces on most wafer areas; the actual DH deposition runs gave high lifetimes on the GaAs control wafers (129 and 140 nsec in the two runs) and therefore are not the problem. Incidentally, the lifetime values on the GaAs substrates, while much higher than the radiative lifetime limit for GaAs at $n = 1 \times 10^{17} \text{ cm}^{-3}$ of 50 nsec, are typical of our MOCVD material and are discussed in detail in the literature [9]; the explanation for these high values is based on a "photon-recycling" theory.

Table 2-1. GaAs-on-Si Lifetime Data from Experiment 2

Nucleation Layer:	S	S	S	S	A	A	A	A
GaAs Buffer:	S	T	S	T	S	T	S	T
Strained Layer:	I	I	-	-	I	I	-	-
Lifetime (nsec):	0.68	0.50	0.46	0.51	0.43	0.60	0.37	0.65

GaAs-on-GaAs Controls: lifetime = 129,140 nsec

Note: S = standard MOCVD; A = ALE growth; T = TCG process; I = InGaAs layer.

Despite the problem encountered, we can still try to draw some conclusions from the data of Table 2-1 by looking at the values averaged over each structural variable. From these it appears that the parameters which improve the lifetime are the use of the standard nucleation process, the TCG process, and the strained InGaAs layer. Due to the large scatter in the data, these conclusions are quite tentative and require further study.

2.2.4.4 Effect of Dislocation Density on Lifetime

Figure 2-11 is a plot of lifetime versus dislocation density for all the samples discussed above but not including those runs with obvious visual surface contamination problems. As expected, high lifetime values correlate with low dislocation densities; it is seen that a change from $4 \times 10^8 \text{ cm}^{-2}$ to $4 \times 10^7 \text{ cm}^{-2}$ in dislocations results in the lifetime increasing from ~ 0.1 nsec (system baseline) to over 1.5 nsec. This trend agrees well with the results of our ongoing modelling study which shows that a reduction in defect density to approximately $1 \times 10^6 \text{ cm}^{-2}$ is needed in order to achieve lifetimes (and solar cell efficiencies) comparable to those of homoepitaxial GaAs [10].

2.2.4.5 Transmission Electron Microscope Analyses

Planview and cross section TEM have been used to study a variety of GaAs-on-Si samples and the defect-density results are summarized in Table 2-2; typical planview micrographs are shown in Figure 2-12. We note that stacking faults are easily eliminated by annealing, and that our TCG process is much more effective at reducing the dislocation density than is the TCA method.

Figure 2-11. Lifetime versus Dislocation density in GaAs on Si

Table 2-2. Planview TEM Results for GaAs on Si

Buffer Thickness	Buffer Growth	InGaAs Layer	Dislocation Density	Stacking Faults
2	TCG	-	3×10^7	no
2	TCG	-	4×10^7	no
5	TCG	-	4×10^7	no
5	TCA	-	4×10^7	no
5	Std	-	1.3×10^8	4×10^6
5	Std.	-	9×10^7	4×10^6
2	Std.	-	2.2×10^8	-
1.6	TCG	$x = 0.15$	-	no
1	Std.	$x = 0.10$	3×10^7	no

Notes: All samples used standard nucleation. Buffer thickness in microns, $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers are 0.1 micron, defect densities in cm^{-2} .

A. No Anneals

Dislocations = $1.3 \times 10^8 \text{ cm}^{-2}$

Stacking Faults = $4 \times 10^6 \text{ cm}^{-2}$

B. TCA

Dislocations = $8.9 \times 10^7 \text{ cm}^{-2}$

C. TCG

Dislocations = $3.7 \times 10^7 \text{ cm}^{-2}$

Figure 2-12. Planview TEM's of GaAs on Si; DH on 5 micron buffers

Figure 2-13 shows a cross section TEM of a DH-GaAs-Si sample grown by the TCG process. The heavily defected region near the interface is confined to the first 1000 angstroms of growth, and dislocation looping and interaction is evident. Above this region, the defect density falls off dramatically; at the top of the sample, the dislocation count is $4 \times 10^7 \text{ cm}^{-2}$ by planview analysis. Unfortunately, some dislocations appear to be generated at the first AlGaAs layer, and these may contribute to the defect density counted. A GaAs-on-Si sample (without the AlGaAs layers) has been grown by the same TCG process and studied by TEM. A cross section of this sample is shown in Figure 2-14; this figure quite clearly shows how the TCG process confines most dislocations to the near-interface region. The planview analyses of this wafer yields a dislocation density of approximately $1-2 \times 10^7 \text{ cm}^{-2}$.

Buffer Growth by TCG

Figure 2-13. Cross section TEM of DH on GaAs on Si

Figure 2-14. Cross section TEM of GaAs-on-Si Sample Grown by the TCG Process

The cross section TEM of an unannealed GaAs-on-Si structure containing a 1000 angstrom $\text{Ga}_{0.9}\text{In}_{0.1}\text{As}$ layer is shown in Figure 2-15; it is clear that the strain in this single layer causes a significant defect-density reduction by the bending over of threading dislocations. Planview TEM study of this sample yields a dislocation count of $3 \times 10^7 \text{ cm}^{-2}$ in the top GaAs layer.

Figure 2-15. Cross Section TEM of Unannealed GaAs on Si with Buried GaInAs Layer

The most effective defect-reduction technique may involve a combination of the TCG and strained-layer procedures. A preliminary attempt in this direction has been made, though much work remains to be done. We have deposited a 1000 angstrom-thick layer of $\text{Ga}_{0.85}\text{In}_{0.15}\text{As}$ on top of a TCG GaAs-on-Si structure; no GaAs layer was grown on top of the GaInAs. This sample was studied by planview and cross section TEM. Figure 2-16 is a cross section which shows a number of interesting features. We can see that the TCG process has confined most defects to the near interface region; one defect, shown clearly at the left edge of the photo, has propagated upwards but appears to have been bent over, probably at one of the TCG interruption points. The GaInAs layer in this sample is filled with misfit dislocations, lying parallel to the interface, and these dislocations seem to be generated in the GaInAs layer; this generation of defects was caused by the fact that for $\text{Ga}_{0.85}\text{In}_{0.15}\text{As}$ on GaAs, the 1000 angstrom thickness exceeds the critical value, and misfit dislocations are generated, as shown clearly in Figure 2-17. Studies to optimize this type of structure are in progress, and hopefully will result in increased cell efficiencies in the near future.

GaAs Buffer Growth by TCG

Figure 2-16. Cross Section TEM of GaInAs Layer on Annealed GaAs on Si

0.25 μ m

Structure=0.1 μ m Ga_{.85} In_{.15} As on 2 μ m GaAs on Si

Figure 2-17. Planview TEM of GaInAs on GaAs on Si

2.2.5 Summary

In summary, we have presented data relating the minority-carrier lifetime and the structural quality of GaAs on Si to a number of buffer-layer design features and growth parameters. The use of a thermal-cycle-growth method is shown to be a major factor in improving material properties. Solar cell device results are presented in Section 3.3.

SECTION 3.0

DEVICES

3.1 DEVICE DESIGN

3.1.1 Optimization of AlGaAs Window Thickness

We have used computer modeling to design the AlGaAs window thickness and antireflection coating thicknesses giving a maximum J_{sc} . The procedure was to calculate internal quantum efficiency (IQE) curves for different AlGaAs thicknesses, using material parameters derived from the 24.3% efficient cell of Section 3.3.2. For each IQE curve, optimum thicknesses of antireflection coating layers were calculated, giving a maximum J_{sc} . Three different AR coating systems were evaluated (ZnS/MgF₂, Si₃N₄/MgF₂, and Si₃N₄). The results are summarized in Figures 3-1 and 3-2.

The optimum AlGaAs thickness is in the range of 150 to 200 angstroms, less than our present value of 300 angstroms. Thinner AlGaAs layers absorb less light, but when too thin the reflectance loss increases. The surface passivation effect will also be lost when the AlGaAs layer becomes thin enough to tunnel through, but this should be a problem only for layers well below 100 angstroms.

We find that our present antireflection coating of ZnS/MgF₂ gives the highest short circuit currents, but Si₃N₄/MgF₂ is nearly as good. ZnS has a better refractive index than Si₃N₄, giving lower reflectance, but has the disadvantage of absorption losses in the UV. Si₃N₄ is being considered for future work because of its environmental stability, and in particular its resistance to moisture relative to ZnS. Both double-layer coatings are much better than a single-layer coating of silicon nitride.

Figure 3-1. Optimum AM1.5 Short Circuit Current Density as a Function of AlGaAs Window Layer Thickness for GaAs Cells with Different Antireflection Coatings

Figure 3-2. Calculated External Quantum Efficiency for GaAs Cells with Different AlGaAs Window Thicknesses and Optimum ZnS/MgF₂ Antireflection Coatings

3.1.2 Optimization of Base Layer Thickness

The model was also used to calculate short circuit current collected by the base layer as a function of base thickness and diffusion length. The results, shown in Figure 3-3, confirm that our present base thickness of 3 microns is nearly optimum for diffusion lengths characteristic of present cells (3 to 3.5 microns). Improvements in base collection must come from improved diffusion length rather than changes in the cell structure.

3.1.3 Optimization of Antireflection Coating Thicknesses

We re-optimized our ZnS and MgF₂ antireflection coating thicknesses using the computer model and the internal quantum efficiency measured for the 24.3% efficient cell. The resulting optimum thicknesses, shown in Figure 3-4, are somewhat less than what we have used in the past. This is because the thickness and composition of the AlGaAs window have decreased relative to older cells. Figure 3-4 also provides a recipe for tailoring the thickness of the second antireflection layer (MgF₂) for non-ideal thicknesses of the first layer (ZnS). Rather large errors in ZnS thickness can be compensated with changes in the MgF₂ thickness, with little short circuit current penalty. This new optimization was used for the cells in Lot 5196 described in Section 3.4.4, with excellent results.

Figure 3-3. Calculated Short Circuit Current Density Collected from the Base Layer as a Function of Base Thickness for Different Minority Carrier Diffusion Lengths

Figure 3-4. Optimum Thicknesses of ZnS and MgF₂ Antireflection Layers for GaAs Cells with a 300 angstrom Al_{0.8}Ga_{0.2}As Window Layer under an AM1.5 Global Spectrum. Numbers next to each calculated point are short circuit current densities.

3.2 DEVICE PROCESSING

During the past year, we have investigated several changes in device fabrication procedures. These include the following:

- (1) A new mesa etch, designed to relieve mask undercutting with our existing etchant.
- (2) The use of an oxide-assisted liftoff process for defining grid lines.
- (3) The use of sulfide surface treatments to reduce the surface component of junction leakage current.

3.2.1 New Solar Cell Mesa Etch

A new mesa etch based on phosphoric acid was implemented to alleviate undercutting with our previous HCl-based etch. In this experiment we compared the old and new mesa etches on solar cells from the same wafer. The objective was to compare edge definition and surface space-charge recombination leakage currents with the two mesa etches.

Two pieces from wafer #875-5 (Lot 5151), containing either 8 or 12 GaAs 0.25 cm^2 solar cells, were used. Each piece was mesa etched with conditions listed in Table 3-1. After etching, the cells were examined microscopically and the log I-V curves were measured.

Table 3-1. Processing Parameters and Mechanical Results for Mesa Etch Comparison.

	System 1	System 2
Composition	$1\text{H}_2\text{O}_2:1\text{HCl}:1\text{H}_2\text{O}$	$1\text{H}_2\text{O}_2:1\text{H}_3\text{PO}_4:3\text{CH}_3\text{OH}$
Expected Etch Rate	1.5-2.0 microns/min	1.6-2.2 microns/min
Temperature	26°C	27°C
Etch Time	2 min	2 min
Etch Rate	1.7 microns/min	1.4 microns/min
Mesa Depth	3.4 microns	2.8 microns
Relative Stability	Less Stable	More Stable
Bubbles?	Yes	No
Cell Edges	Jagged	Smooth
Etched Surface	Rugged	Smooth
Mesa Walls	Tapered (outward)	Straight
Maximum Undercut	≤ 50 microns	≤ 3 microns

Results: As noted in Table 3-1, the new phosphoric acid etch gave far less undercutting than the old HCl etch, straighter walls, and smoother bottoms in the etched areas. Electrically, the surface leakage currents (J_{02}) were quite similar for the two etches. The results of log I-V analysis are listed in Table 3-2. We therefore see distinct advantages and no disadvantages to using the new mesa etch, and have incorporated it in our standard cell process.

Table 3-2. Log I-V Analysis Results for Mesa Etch Comparison. Averages are shown for 4 cells with HCl etch and 11 cells with H₃PO₄ etch. Data from 4 additional HCl-etched cells and 1 additional H₃PO₄-etched cell are not included because of unusually high values of J_{o2} or shunting

Etch	V _{oc} * (V)	J _{o1} (A/cm ²)	J _{o2} (A/cm ²)
HCl	0.983	1.20 x 10 ⁻¹⁹	4.81 x 10 ⁻¹²
H ₃ PO ₄	0.983	1.22 x 10 ⁻¹⁹	4.69 x 10 ⁻¹²

* Evaluated at a J_{sc} of 6 mA/cm², about 1/4 sun.

3.2.2 Oxide-Assisted Liftoff Process

A simple photoresist liftoff process and an oxide-assisted liftoff process for defining metal grid lines are compared in Figure 3-5. The silicon dioxide layer is deposited by chemical vapor deposition (Silox). The oxide-assisted process has these advantages:

- (1) No organic contamination of the GaAs surface by photoresist residues. Organic residues interfere with the cap removal etch later in the process sequence. Insoluble photoresist can result from the high temperatures associated with the evaporation of thick gold layers.

Figure 3-5. Comparison of Conventional Photoresist Liftoff Process and Oxide-assisted Liftoff Process

- (2) Physical separation of the photoresist layer and GaAs surface, preventing bridging of the deposited metal layer from the grid lines to the photoresist. This facilitates an easier liftoff.

Because of these advantages, we have incorporated the oxide-assisted liftoff into our fabrication processes for both one-sun and concentrator cells.

3.2.2.1 Trench Formation Along Grid Lines

An unexpected side effect of the oxide-assisted liftoff process was the formation of a narrow trench along-side the grid lines during the cap removal etch. This trench extended through the window and emitter layers, and in severe cases could completely cut off the grid lines from the rest of the cell area (see Figure 3-6). Depending on the severity in an individual cell, it could have very small or very large effects on the cell efficiency.

In most cases the trenches degraded cell efficiency through decreased short circuit current and fill factor, but in some cases they improved it significantly, especially for lightly-doped emitters (see Section 3.4.1). Our interpretation of this peculiar behavior is discussed later in Section 3.4.1.

After conducting a number of experiments, we have concluded that the following mechanism is responsible for trench formation. The source of the problem is a photo-electrochemical etching process which occurs when the silicon dioxide masking layer is removed in buffered HF. See Figure 3-7 for a schematic description of the process. In the presence of light, a forward bias voltage appears across the p-n junction of the cell. When the cell is immersed in buffered HF, an electrochemical cell is formed. Gallium arsenide is dissolved from the p-side (anode) and plates out on the n-side of the wafer (cathode). Because most of the p-side is masked with oxide, there is a high current density in the narrow exposed GaAs strip beside the grid lines and it etches rapidly. If the etching reaches the AlGaAs window, it too is etched both electrochemically and chemically by HF. When the wafer is later subjected to the selective cap removal etch, there is no etch stop remaining and a trench is etched in the emitter.

This hypothesis is supported by several observations. First, the trenches only occur with the oxide-assisted liftoff process. Second, cells with ohmic shunts do not form trenches. This is because the junction is shorted and no photovoltage is developed. Third, if the HF etch is carried out in the dark, no trenches are formed. Again, in the absence of voltage the electrochemical cell does not operate.

We have confirmed that etching the oxide layer in the dark prevents etching of the GaAs cap layer and trench formation. This modification has been successfully incorporated into our cell process; recent process lots have had no trenching problem.

3.2.3 Sulfide Surface Passivation

There have been a number of recent reports in the literature of reduction of surface recombination in GaAs using sodium sulfide chemical treatments [1,11]. Since surface recombination controls the space-charge recombination current in our GaAs cells, which in turn controls the fill factor of one-sun cells, we wished to verify the effect and see if it could be used to improve our cells. The experiment (process lot 5151) consisted of

a

b

c

Figure 3-6. SEM Cross Sections Showing Trenches Along Grid Lines After Cap-removal Etch. (a) low magnification of grid line, (b) high magnification of grid line edge, (c) schematic diagram of photo in (b)

Figure 3-7. Schematic Diagram of the Trench Formation Process

monitoring log I-V curves of solar cells before and after several chemical treatments. The space-charge recombination current was then extracted from the log I-V curve.

Groups of several 0.5 cm x 0.5 cm GaAs cells without antireflection coatings were subjected to one of the following treatments:

- I. 0.5M $\text{Na}_2\text{S} \cdot 9\text{H}_2\text{O}$ (3-minute immersion, 70-second spin-on at 4000 rpm, or 2-minute anodization at 10 mA/cm^2)
- II. 0.5M Na_2SO_3 (3-minute immersion)
- III. 0.5M $\text{Na}_2\text{S}_2\text{O}_3 \cdot \text{SH}_2\text{O}$ (3-minute immersion)

We found that the sodium sulfide treatment does reduce the space-charge recombination current by up to 40%, a significant improvement. Figure 3-8 compares typical before and after I-V curves. Bulk space-charge recombination may be limiting the dark current after the sulfide treatment, preventing even larger gains as reported in the literature [11]. Although the best results were for immersion in $\text{Na}_2\text{S} \cdot \text{H}_2\text{O}$, some degree of improvement was observed for all treatments except Na_2SO_3 (see Table 3-3). We noted the appearance of crystallographically oriented pits in the junction area for electrically active cells; pitting was not observed for shunted cells near the wafer edge. This electrochemical pitting has not been reported before.

Figure 3-8. Comparison of Log I-V Characteristics of a 0.25 cm² GaAs Cell before and after Treatment with Sodium Sulfide

Table 3-3. Comparison of Space-charge Recombination Saturation Currents Before and After Sulfide Treatments. Values are for one representative 0.5 cm x 0.5 cm solar cell

Treatment	J_{o2} Before (A/cm²)	J_{o2} After (A/cm²)	Ratio
Na ₂ S·9H ₂ O, dip	3.81x10 ⁻¹²	2.31x10 ⁻¹²	0.61
Na ₂ S·9H ₂ O, spin	5.39x10 ⁻¹²	3.93x10 ⁻¹²	0.73
Na ₂ S·9H ₂ O, anodize	4.87x10 ⁻¹²	3.72x10 ⁻¹²	0.76
Na ₂ SO ₃ , dip	4.34x10 ⁻¹²	5.26x10 ⁻¹²	1.21
Na ₂ S ₂ O ₃ ·SH ₂ O, dip	7.57x10 ⁻¹²	4.89x10 ⁻¹²	0.65

The problem with this technique is that the improvement is often temporary; it can be lost in a water rinse or simply with extended exposure to room air. We have not yet found a way to make the improvement permanent.

3.3 GaAs-on-Si SOLAR CELLS

3.3.1 Concentrator Cells, Lot 5163

A point-focus concentrator grid pattern was applied to GaAs/Si and GaAs/GaAs solar cell wafers. The pattern, designed for 500 suns operation, had a 1/4 inch diameter circular active area (0.3167 cm^2) enclosed in a square bus bar. The GaAs/Si wafer was previously grown as part of a base doping experiment. It employed a number of growth improvements, including thermal cycling during growth, an AlGaAs back-surface-field layer, and a thick buffer layer. The GaAs control wafer was also grown earlier, and used our standard structure. The purpose of the experiment was not only to investigate the performance of GaAs/Si cells at concentration, but also to use high-current operation to probe the diffusion current component of the dark current of GaAs/Si cells, which has previously been masked by high space-charge recombination currents. The diffusion current contains information about minority carrier lifetimes useful in loss analyses, and sets the upper limit on V_{oc} and fill factor in the cells.

Table 3-4 summarizes the results for the best cell of each type at 1 and 20 suns, under standard concentrator test conditions (AM1.5 Direct, 100 mW/cm^2 , spectral mismatch corrected, 28°C). 20 suns is the maximum concentration we can achieve in our dc simulator without excessive cell heating.

Table 3-4. Best-cell Efficiency Results for Concentrator Cells from Lot 5163

Cell Type	MOCVD Run	Suns	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)
GaAs/Si	1317	1	0.840	19.97	77.8	13.0
		21	0.971	419.6	79.6	15.6
GaAs	1070	1	1.007	25.17	86.8	22.0
		20	1.085	500.7	88.2	24.1

The efficiencies of both types of cells were very good at one sun. The efficiency of the GaAs/Si cell is lower than the 15.2% we achieved previously for a one-sun cell in the same material, for reasons relating to device design and test conditions. The short circuit current density is lower because there is more grid shadow for a concentrator cell and because there is less light available to a GaAs cell in the AM1.5 Direct spectrum than in the AM1.5 Global spectrum. The open circuit voltage is lower because the measurements are made at a higher temperature, because there is a large shaded area under the bus bar which contributes dark current but not photocurrent, and because the J_{sc} is lower. Nevertheless, this cell is a large improvement over our previous GaAs/Si concentrator cells, which were 9% efficient at one sun. The GaAs control efficiency of 22% at one sun is equal to our previous best under Sandia funding.

For testing at higher concentrations, GaAs/Si and GaAs/GaAs cells were measured at Sandia National Laboratories in a flash simulator (courtesy of Dr. Doug Ruby). The best GaAs/Si concentrator cell was 18.46% efficient at 370 suns. This is a large improvement over our previous result of 13.7% [12]. Table 3-5 lists the data for the best cell as a function of concentration, and Figure 3-9 shows its efficiency at 25 and 80°C. Table 3-6 summarizes the results for the four cells tested at Sandia at a concentration of 500 suns, the design value for this mask pattern. The uniformity of the results was very good.

Table 3-5. Efficiency Data Measured for the Best GaAs/Si Concentrator Cell from Lot 5163 (AM1.5 Direct, 100 mW/cm², 0.317 cm²)

Suns	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff. (%)	Temp. (°C)
1.00	0.836	20.81	76.9	13.38	24.9
4.87	0.909	101.3	76.4	14.44	24.9
10.84	0.947	225.6	78.0	15.38	25.0
21.48	0.979	447.0	79.0	16.10	24.9
54.95	1.021	1143.	80.3	17.06	25.0
109.24	1.045	2273.	81.0	17.61	25.0
215.06	1.069	4475.	81.7	18.18	25.0
369.68	1.088	7693.	81.6	18.46	25.1
534.24	1.098	11118.	80.7	18.43	25.2
1056.59	1.113	21988.	77.8	18.01	25.2
1.00	0.717	21.46	72.4	11.18	80.1
5.15	0.801	110.5	73.2	12.57	80.1
11.01	0.840	236.3	74.9	13.50	80.0
21.90	0.876	469.9	75.7	14.22	80.4
55.52	0.920	1191.	77.5	15.29	80.0
110.29	0.947	2367.	78.5	15.95	80.2
218.12	0.975	4680.	79.2	16.58	80.2
377.29	0.995	8096.	79.1	16.88	80.2
540.00	1.006	11587.	78.8	17.01	80.0
1072.03	1.026	23003.	75.7	16.67	80.2

Figure 3-9. Efficiency as a Function of Concentration Ratio for a GaAs/Si Cell from Lot 5163. The cell was measured at two different temperatures.

Table 3-6. Comparison of Four GaAs/Si Cells at 500 Suns Concentration (AM1.5 Direct, 25°C)

Cell	Suns	V _{OC} (V)	I _{SC} (A)	FF (%)	Eff. (%)
1317-2	540	1.096	3.500	82.3	18.44
1317-3	531	1.099	3.447	81.4	18.33
1317-6	550	1.098	3.582	81.0	18.26
1317-7	534	1.098	3.524	80.7	18.43

Four GaAs/GaAs control cells were also tested. The efficiency peaked at 24.2% at 360 suns. Table 3-7 compares the results for the four cells at 500 suns; again the uniformity of results was good. Figure 3-10 compares the efficiency versus concentration of the best cell in this lot to our best previous GaAs concentrator cell, which had a peak efficiency of 25.4%. The present cells are lower in efficiency because of lower J_{SC} , which in turn was caused by AlGaAs window oxidation in this particular cell material. We note that the J_{SC} of the control cells dropped about 5% between Spire's and Sandia's measurements, while the GaAs/Si cells showed no change. If the cells had maintained their starting J_{SC} , the efficiency at concentration would have been 25.4%, equaling our previous best. The cells of this lot, however, maintained their efficiencies to higher concentrations, as can be seen from the high-concentration rolloff in Figure 3-10 and the fill factor comparison in Figure 3-11.

Table 3-7. Comparison of Four GaAs Control Cells at 500 Suns Concentration (AM1.5 Direct, 25°C)

Cell	Suns	V_{oc} (V)	I_{sc} (A)	FF (%)	Eff. (%)
1070-4	507	1.179	3.768	86.0	23.77
1070-5	518	1.179	3.908	85.9	24.10
1070-6	527	1.179	4.019	84.9	24.08
1070-8	521	1.176	3.847	85.2	23.33

Figure 3-10. Efficiency as a Function of Concentration Ratio for a GaAs Control Cell from Lot 5163, Compared to Our Best Previous GaAs Concentrator Cell

Figure 3-11. Comparison of Fill Factors for the Two Cells in Figure 3-10

As noted earlier, a major goal of this experiment was to measure the bulk diffusion current of GaAs/Si cells by going to high concentrations. In this we were successful. Figure 3-12 compares the log I-V characteristics of GaAs/Si and GaAs concentrator cells. The GaAs control follows an ideality factor (n) of 1.0, showing that it is dominated by diffusion current at intensities above one sun. The GaAs/Si cell shows a break from $n = 1$ to $n = 2$ at high concentrations and a clear $n = 1$ region from which we can measure the diffusion current. To further enhance the $n = 1$ current, the cells were also measured at an elevated temperature (80°C). Figure 3-13 compares the log I-V curves of the GaAs/Si cell at 25 and 80°C . As a further confirmation that diffusion current is responsible for the $n = 1$ region, we compared the temperature dependence of the saturation currents derived from Figure 3-13. The $n = 1$ current had the same temperature dependence as n_1 , as expected for diffusion current. The $n = 2$ current was proportional to n_2 , as expected for space-charge recombination.

Using the diffusion saturation current, we can project the performance of GaAs/Si cells at one sun in the absence of $n = 2$ current, which dominates present cells. The diffusion currents in the GaAs/Si cells were 7 to 10 times higher than in the GaAs controls, in fairly good agreement with what we had predicted based on diffusion lengths from quantum efficiency modeling [12]. This results in a V_{oc} loss of only 50 to 60 mV relative to GaAs cells, so that a V_{oc} of 970 mV would be achievable at one sun without the $n = 2$ current.

Figure 3-12. Comparison of I_{sc} - V_{oc} Characteristics at Concentration for GaAs/Si and GaAs Control Cells from Lot 5163

Figure 3-13. Temperature-dependent I_{sc} - V_{oc} Characteristics for a GaAs/Si Cell from Lot 5163

Comparing efficiencies for the two materials, we find a difference of about 6 absolute percentage points between GaAs/Si and GaAs/GaAs cells. Most of this is attributed to crystal defects in GaAs/Si material. However, in examining the cells it was found that the grid line widths were larger for GaAs/Si cells than for the GaAs controls. The resulting decrease in short circuit current through shadowing (about 3% relative difference) is an additional loss mechanism related to device processing.

3.3.2 Thermal Cycle Growth Variations, Lot 5188

In this experiment, we tried a number of variations of the thermal cycling process during growth of the GaAs buffer layer on silicon. The general process was to grow a 1-micron buffer on the Si substrate, cycle the layer to a high and then low temperature, grow more GaAs, thermal cycle up and down again, then grow a final GaAs layer. After all the buffers were grown, nominally identical solar cell active layers were grown on them. One GaAs substrate was included in each solar cell growth run as a control. The experimental parameters were the upper and lower temperatures of the thermal cycle, time at high temperature, and overall thickness of the buffer. The parameters for each run are summarized in Table 3-8.

The solar cell structures used the single-temperature growth process at 740°C. Other notable features of these cells were a thin emitter (0.25 micron) optimized for the short diffusion lengths in GaAs/Si, and an AlGaAs window layer with the optimum thickness of 300 angstroms and a composition of $x = 0.80$ to minimize oxidation.

Efficiency results for the best cell on each wafer are summarized in Table 3-9; averages and standard deviations are summarized in Table 3-10.

The GaAs/Si efficiency of 18.1% is the best we have achieved. The GaAs control cells were also very good, with several over 24%. The average for wafer 1471-1 is higher than our record efficiency of a year ago. Samples of both types were tested at SERI, with results in Table 3-11.

SERI's efficiency measurements of the GaAs/Si cells were slightly lower than ours, by about 0.7% in V_{OC} , J_{SC} , and FF. SERI's GaAs efficiency measurements were very close to ours, with the best cell being slightly higher in efficiency. The best efficiency of 24.3% set a new one-sun efficiency record, improving upon our 24.2% from Lot 5172 (see Section 3.4.1).

To our surprise, we did not find any significant efficiency differences between the different thermal cycling conditions. In some ways this is good, because it means the process is very reproducible. However, it also means that we need to examine other variables to achieve further efficiency improvements. Based upon recent conversations with Dr. Yamaguchi from NTT, the number of thermal cycles should be investigated as a variable in future experiments.

The scatter in the results of Table 3-10 is attributed primarily to the formation of trenches along the grid lines, as discussed in Section 3.2.2.1. It was particularly severe for GaAs control wafer 1473-1.

Table 3-8. Thermal Cycling Parameters for the GaAs/Si Wafers in Lot 5188

MOCVD Run	Wafer #	Upper, Lower Temps. (°C)	Time (min)	Layer Thickness (microns)		
				Top	Mid	Bot
1471	2	900 - 75	2	1	4	1
1471	3	900 - 75	20	1	4	1
1471	4	950 - 75	2	1	4	1
1471	5	950 - 75	20	1	4	1
1472	2	950 - 75	20	0	4	2
1472	3	950 - 285	20	1	4	1
1472	4	900 - 75	20	1	2	1
1472	5	950 - 75	20	1	2	1

Table 3-9. Comparison of Best-cell Efficiency Results from Lot 5188. Test conditions: AM1.5 Global, 100 mW/cm², no spectral mismatch correction, 25°C, total area, 0.25 cm²

Wafer ID	Type	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff. (%)
1471-2	GaAs/Si	0.888	25.29	78.0	17.5
1471-3	GaAs/Si	0.894	25.57	77.7	17.8
1471-4	GaAs/Si	0.883	25.41	77.9	17.5
1471-5	GaAs/Si	0.896	25.56	78.2	17.9
1472-2	GaAs/Si	0.896	25.59	78.0	17.9
1472-3	GaAs/Si	0.892	25.36	78.2	17.7
1472-4	GaAs/Si	0.895	25.68	77.3	17.8
1472-5	GaAs/Si	0.898	25.89	77.8	18.1
1471-1	GaAs	1.023	27.26	86.3	24.1
1472-1	GaAs	1.020	26.66	85.7	23.3
1473-1	GaAs	1.017	27.19	84.1	23.3

Table 3-10. Comparison of Average Efficiency Results from Lot 5188. Standard deviations are in parentheses. Test conditions: AM1.5 Global, 100 mW/cm², no spectral mismatch correction, 25°C, total area, 0.25 cm²

Wafer ID	Type	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff. (%)	# of Cells
1471-2	GaAs/Si	0.855 (0.024)	24.76 (0.56)	76.35 (1.18)	16.18 (0.83)	36
1471-3	GaAs/Si	0.889 (0.006)	25.26 (0.24)	77.45 (0.64)	17.39 (0.23)	26
1471-4	GaAs/Si	0.877 (0.009)	24.95 (0.26)	76.90 (1.17)	16.83 (0.41)	26
1471-5	GaAs/Si	0.884 (0.017)	25.32 (0.40)	76.92 (1.53)	17.22 (0.69)	41
1472-2	GaAs/Si	0.888 (0.008)	25.27 (0.25)	77.53 (0.95)	17.39 (0.40)	37
1472-3	GaAs/Si	0.887 (0.005)	25.08 (0.23)	77.48 (0.99)	17.24 (0.31)	27
1472-4	GaAs/Si	0.888 (0.005)	25.14 (0.49)	76.09 (1.79)	16.98 (0.63)	19
1472-5	GaAs/Si	0.886 (0.010)	25.37 (0.22)	76.89 (1.28)	17.29 (0.46)	28
1471-1	GaAs	1.024 (0.003)	27.08 (0.15)	85.65 (0.82)	23.75 (0.21)	20
1472-1	GaAs	1.021 (0.004)	25.77 (0.42)	84.04 (1.02)	22.12 (0.54)	18
1473-1	GaAs	1.001 (0.013)	26.88 (0.37)	78.21 (5.97)	21.08 (2.02)	17

Table 3-11. Efficiency Measurements Made at SERI for Cells from Lot 5188. Test conditions: AM1.5 Global, 100 mW/cm², 25°C, total area

Cell ID	Type	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff. (%)
1471-5-3	GaAs/Si	0.892	25.30	77.73	17.5
1471-5-19	GaAs/Si	0.889	25.50	77.50	17.6
1471-5-22	GaAs/Si	0.891	25.47	77.68	17.6
1471-5-26	GaAs/Si	0.887	25.51	77.74	17.6
1471-5-38	GaAs/Si	0.889	25.42	77.49	17.5
1472-5-22	GaAs/Si	0.891	25.47	77.68	17.6
1471-1-10	GaAs	1.018	27.57	86.46	24.3
1471-1-18	GaAs	1.025	27.55	85.85	24.3

One notable feature of the GaAs/Si efficiency measurements is the relatively high short circuit current. This is the largest improvement over our previous GaAs/Si cells. Figure 3-14 compares internal quantum efficiency curves for the best GaAs and GaAs/Si cells from this lot. The response of the GaAs/Si cell is nearly as high as the GaAs cell. We attribute the improved response mainly to better growth conditions and compositional control of the AlGaAs window layer. The GaAs/Si material quality, in terms of diffusion length and defect density, is apparently similar to earlier cells grown by the thermal cycling process.

Figure 3-14. Comparison of Best-cell Spectral Response Curves for GaAs and GaAs/Si Cells in Lot 5188

3.4 HIGH EFFICIENCY GaAs SOLAR CELLS

3.4.1 Emitter Doping, Lots 5171 and 5172

As part of our collaboration with Prof. Mark Lundstrom at Purdue University, GaAs solar cells were grown with four different emitter dopings. This continues earlier work which explored very high emitter dopings, and was aimed at understanding heavy doping effects. However, in these runs we used very low emitter dopings, down to $2 \times 10^{16} \text{ cm}^{-3}$. The lower doping results in longer emitter diffusion lengths and increases the sensitivity to interface recombination at the AlGaAs-GaAs interface. It was hoped that these cells would allow us to more accurately determine the heteroface recombination velocity.

The emitter dopings (measured by junction capacitance) and window layer composition and thickness (measured by optical reflectance) are summarized in Table 3-12. One 2-inch wafer from each run was processed with 0.25 cm^2 solar cells. After mesa etch, but before antireflection coating, each wafer was split in half and one half was sent to Purdue for electrical measurements. The other half was retained at Spire for antireflection coating and efficiency measurements. Another wafer from each run was used for internal quantum efficiency measurements.

Table 3-12. Emitter Doping and Window Layer Parameters for the Emitter Doping Comparison

MOCVD Run	Emitter Doping (cm^{-3})	Window Thickness (Å)	Window Composition x
1424	2×10^{16}	328	0.77
1425	1×10^{17}	410	0.83
1423	1×10^{18}	304	0.76
1426	6×10^{18}	462	0.85

Figure 3-15 compares the internal quantum efficiency of cells with a wide range of emitter dopings. There is very little difference attributable to the emitter doping, reinforcing our earlier conclusion that in all cases the emitter diffusion length is much larger than the emitter thickness. Differences in the curves below 500 nm are caused by different AlGaAs window thicknesses. Peak internal quantum efficiencies reach 100% (within experimental error), implying low interface recombination velocities.

To check for absorption in the antireflection coatings, which has been identified as a potential problem, the same samples were antireflection coated and the internal quantum efficiencies remeasured. Figure 3-16 shows the quantum efficiency curves before and after coating. There was a substantial loss at short wavelengths. Separate measurements of the optical properties of ZnS and MgF_2 films by spectroscopic ellipsometry and by transmission measurements showed that the absorption loss is entirely in the ZnS layer.

Figure 3-15. Internal Quantum Efficiency Comparison of GaAs Cells with Different Emitter Dopings (no antireflection coating)

Figure 3-16. Internal Quantum Efficiency Comparison of GaAs Cells With and Without ZnS/MgF₂ Antireflection Coating

Log I-V measurements of the solar cells were used to extract the $n = 1$ and $n = 2$ saturation currents. These are compared in Table 3-13. The bulk diffusion current, J_{o1} , changes only slightly with doping, continuing the trend found earlier. Figure 3-17 combines the results of J_{o1} measurements for cells with a wide range of emitter dopings. There is a shallow minimum in J_{o1} at a doping of about 1×10^{18} , but little variation over 3 decades in emitter doping.

The insensitivity of J_{o1} to emitter doping has at least two possible explanations. One is that J_{o1} is limited primarily by the base, and that the emitter component is in all cases small. The second is that increased doping is accompanied by decreased minority carrier lifetime, so that the emitter diffusion current is constant with doping. This can be seen from the expression for emitter-limited J_{o1} when the emitter is thinner than a diffusion length and has a passivated surface:

$$J_{o1} = q n_i^2 t_e / (N_A \tau_e)$$

Where q is the electron charge, n_i is the intrinsic-carrier concentration, t_e is the emitter thickness, N_A is the emitter doping, and τ_e is the minority-carrier electron lifetime. If the minority-carrier lifetime is inversely proportional to the emitter doping (as is the case for radiative recombination lifetime), then J_{o1} is independent of doping. At very high dopings J_{o1} could increase due to bandgap narrowing (increased n_i) or Auger recombination (decreased τ_e). J_{o1} could also increase at very low dopings if surface recombination became comparable to bulk recombination. We note that a similar argument could also be made for the base of the cell, so that J_{o1} might also be independent of base doping.

Based on the measured values of J_{o1} , we can place limits on the heteroface recombination velocity. Figure 3-18 shows calculated values of J_{o1} as a function of emitter diffusion length and heteroface recombination velocity for the most lightly doped emitter. An upper limit of 5×10^3 cm/s can be placed on S_j based on the measured value of J_{o1} . This is much lower than the value of approximately 1×10^5 that has previously been inferred from cell modeling. The results of similar plots for the other emitter dopings are listed in Table 3-14.

Table 3-13. Comparison of Dark Saturation Currents for GaAs Cells with Different Emitter Dopings (average of several cells)

MOCVD Run	Emitter Doping (cm ⁻³)	J_{o1} (A/cm ²)	J_{o2} (A/cm ²)
1424	2×10^{16}	1.32×10^{-19}	1.68×10^{-11}
1425	1×10^{17}	1.27×10^{-19}	9.72×10^{-12}
1423	1×10^{18}	9.68×10^{-20}	6.19×10^{-12}
1426	6×10^{18}	1.11×10^{-19}	5.74×10^{-12}

Figure 3-17. Bulk Diffusion Saturation Current J_{01} at 25°C as a Function of Emitter Doping

Figure 3-18. Calculated Emitter Diffusion Current for a Doping of 2×10^{16} cm⁻³

Table 3-14. Minimum Emitter Diffusion Lengths and Maximum Heteroface Recombination Velocities Consistent with Measured Values of J_{01} . Also listed are measured values of radiative- recombination-limited diffusion length for p-GaAs from Wight.

MOCVD Run	Emitter Doping (cm ⁻³)	Maximum S_i (cm/s)	Minimum L_e (μm)	Literature L_e (μm)
1424	2×10^{16}	5×10^3	8	50
1425	1×10^{17}	2.5×10^4	3	20
1423	1×10^{18}	6×10^4	2	8
1426	6×10^{18}	2×10^5	1	4

The limits in Table 3-14 assume that J_{01} is completely from the emitter. Any contribution from the base will lower the value of S_i . We wondered if unique values of S_i and the base saturation current (J_{01B}) could fit all of the measured data. We therefore did the following calculation. First we picked different values of J_{01B} and subtracted them from the measured J_{01} to get the emitter saturation current, J_{01E} . We then assumed that the emitter diffusion length was the value given by Wight [13] and found the value of S_i needed to match J_{01E} . Plots of S_i as a function of J_{01B} were constructed for cells with different emitter dopings, and we looked for points of intersection. The results are shown in Figure 3-19.

If we assume that the emitter dominates J_{01} (J_{01B} is small), then we must conclude that the heteroface recombination velocity varies strongly with emitter doping. It is not clear why this should be so. However, if we assume that S_i should be roughly independent of emitter doping, and look for points of intersection, we conclude that J_{01B} must be a large fraction of J_{01} . Although there is no point where all of the curves in Figure 3-19 coincide, three of them converge at a value of $J_{01B} = 8 \times 10^{-20}$ A/cm² and $S_i = 8 \times 10^3$ cm/s. Because the base layers were nominally identical for all runs, the value of J_{01B} should be constant. This implies that the run doped 6×10^{18} had a recombination velocity of about 2.7×10^4 , while the most lightly doped run had $S_i = 1.8 \times 10^3$. In other words, there does appear to be some variation in S_i from run to run. However, all of these values are significantly lower than we have determined in the past.

If we go back to previous cell analyses, the major reason for inferring high recombination velocities was internal quantum efficiencies less than 100%. Small unaccounted-for losses, on the order of a few percent, could be responsible for the non-unity measured quantum efficiencies. Figure 3-20, for example, shows calculated quantum efficiencies at 600 nm as a function of interface recombination velocity. Measurement errors on the order of 1% can mean the difference between an inferred recombination velocity of 10^3 and 10^5 cm/s. Some possibilities include scattered light in the measurement apparatus, absorption in the antireflection coating (for finished cells) or other sources of systematic error in the measurement. Calibration accuracies of reference detectors are also of this order. Based on the J_{01} results for lightly-doped emitters, it would be worthwhile to reassess our previous conclusions about the heteroface recombination velocity.

Figure 3-19. Combinations of Interface Recombination Velocity and Base Saturation Current Fitting the Measured J_{01} , for Different Emitter Dopings

Figure 3-20. Sensitivity of Internal Quantum Efficiency at 600 nm to Interface Recombination Velocity

Turning now to the $n = 2$ dark current, Table 3-13 shows a steady decrease in J_{O2} with increasing emitter doping. We believe that this is a result of changing space-charge-layer (SCL) width with doping. Figure 3-21 plots J_{O2} as a function of bulk SCL width. The direct proportionality can be explained by the expression for perimeter-limited J_{O2} ,

$$J_{O2} = q n_i W s (P/A)$$

where q is the electronic charge, n_i is the intrinsic carrier concentration, W is the SCL width at the junction perimeter (also called the surface diffusion length by some authors), s is the surface recombination velocity, P is the perimeter and A is the area of the junction. We assume here that the surface depletion width is proportional to the bulk depletion width. Note that for emitter dopings above 10^{18} there is little change in W or J_{O2} , because most of the SCL is on the base side of the junction, doped $2 \times 10^{17} \text{ cm}^{-3}$. This accounts for the fact that we have not seen this effect previously. It implies that increasing the base doping, and thereby shrinking the SCL, should provide a further decrease in J_{O2} . It is also worth noting that if J_{O2} were bulk-lifetime-limited, and not surface-limited, we would expect to see a different trend of J_{O2} with doping. In addition to the dependence on W , J_{O2} would be inversely proportional to the bulk lifetime, which should decrease with increased doping. J_{O2} would then be expected to decrease less strongly or even increase somewhat with increased doping.

Figure 3-21. Space-charge Recombination Current J_{O2} as a Function of Space-charge Layer Width for Cells with Different Emitter Dopings

The preceding discussion was based on measurements made before antireflection coating. Table 3-15 summarizes Spire's efficiency results for the best cell from each wafer after antireflection coating. The efficiency of 24.4% was the best we had measured for a GaAs cell at the time. Wafer 1423 was sent to Keith Emery at SERI for confirming measurements. His results were the following (for cell #9): $V_{oc} = 1.036$ V, $J_{sc} = 27.36$ mA/cm², FF = 85.25%, Efficiency = 24.17%. This was the highest one-sun cell efficiency measured at SERI at the time.

Table 3-15. Best-cell Efficiencies Measured at Spire for the GaAs Cells of Lot 5172. Test conditions: AM1.5 global, 100 mW/cm², no spectral mismatch correction, 25°C, total area, 0.25 cm²

Cell #	Emitter Doping (cm ⁻³)	V_{oc} (V)	J_{sc} (mA/cm ²)	FF (%)	Eff. (%)
1424-18	2×10^{16}	1.036	27.34	83.5	23.7
1425-4	1×10^{17}	1.036	27.33	81.9	23.2
1423-9	1×10^{18}	1.036	27.86	84.6	24.4
1426-37	6×10^{18}	1.024	26.22	84.9	22.8

Although the efficiency results were quite good, they were also difficult to understand. In particular, the open-circuit voltages for the two most lightly doped emitter samples were much higher than expected from the before-AR log I-V measurements reported above. When we re-checked the log I-V curves, we found that they had improved considerably after AR coating. One example is shown in Figure 3-22. This has not been seen before. We also noted a tremendous spread in efficiency values across most of the wafers, caused primarily by J_{sc} differences. Detailed microscopic investigation showed that trenches were present along the grid lines, similar to Figure 3-6. In most cases the trenches degraded cell efficiency, but in some cases they improved it significantly, especially for lightly-doped emitters. We believe that by isolating the grid lines from the rest of the emitter, the trenches dramatically reduced the emitter component of dark current. For cells with lightly-doped emitters in which the emitter component was dominant, this improved the V_{oc} . To explain the high J_{sc} , we postulate that the carriers collected by the floating emitter were re-injected into the base near the trenches, then diffused to the junction under the grid lines to be collected (see Figure 3-23). The mechanism is analogous to that in so-called "tandem junction" silicon cells developed several years ago by Texas Instruments [14]. For this to work the trench could not extend very deeply into the base and could not be wider than a diffusion length in the base, roughly 3 microns. Both conditions appear to be satisfied from the SEM micrographs of these cells. A discussion of the method of formation of the trenches can be found in Section 3.2.2.1 of this report.

Figure 3-22. Log I-V Characteristics Before and After Antireflection Coating for a Lightly-doped Emitter Cell from Lot 5172

Figure 3-23. Proposed Method of Operation of GaAs Cells with Trenches Etched Along the Grid Lines

Although this is an extremely interesting phenomenon, it may not be terribly useful for solar cells. First, the improvement was not seen for cells with conventional (higher) emitter dopings, presumably because they are base-limited. The cells which improved were still not the best ones. Second, unless the trench etching can be brought under better control, the line between improvement and disaster is very fine. Wide or deep trenches shut off the photocurrent almost completely.

3.4.2 Continuous Growth Process, Lots 5184, 5185

Our standard GaAs cell growth process had used growth temperatures of 700°C for the GaAs layers and 800°C for the AlGaAs window layer. These are optimum growth conditions for the two materials. However, the critical interface between the GaAs emitter and AlGaAs window was left exposed to the gas stream for 10 minutes while the temperature was raised from 700°C to 800°C and stabilized. There was concern that contamination or defects could result which would increase the recombination velocity at this interface. We therefore changed the process to grow all layers at 740°C with no interruption in growth at the emitter/window interface. In lot 5184 we evaluated the internal quantum efficiency of cells grown in this manner, and in lot 5185 we went through the full solar cell process.

Figure 3-24 compares internal quantum efficiencies of cells grown with the standard growth process and the single-temperature growth process. The measurements were on simple test structures with no grid lines or antireflection coatings. The standard process cells were from Lot 5171, reported in the previous section, which had record efficiencies. For both growth processes, the peak internal quantum efficiency is 100%, within experimental error, indicating a very low interface recombination velocity. The single-temperature growth gives somewhat lower blue response but higher red response. The higher red response is indicative of higher base diffusion length, since the layer thicknesses were identical. We speculate that the higher diffusion length may result from a higher GaAs growth temperature. However, the base doping was slightly lower than usual, 1.1×10^{17} instead of $2.0 \times 10^{17} \text{ cm}^{-3}$, and this could also increase the diffusion length. The difference in blue response is not fully understood. Normally a lower blue response is indicative of a thicker AlGaAs window, but reflectance modeling shows that this is not the case (window thicknesses and compositions are shown in Figure 3-24). One possibility is that the lower AlGaAs growth temperature reduces the diffusion length, reducing collection from the window.

Representative log I-V curves are compared in Figure 3-25 for the two growth processes. The cell structures were nominally the same. These curves were measured for cells with the full cap layer still in place, before antireflection coating. The single-temperature growth has a higher $n = 1$ current component, but a much lower $n = 2$ current. Table 3-16 summarizes the results of log I-V analysis for the two wafers. The $n = 1$ component, from bulk diffusion current, may be higher because the base doping is lower. This higher $n = 1$ current results in lower V_{oc} (see efficiency results below); an 11 mV difference at AM1.5 is predicted. The $n = 2$ current, which is believed to be caused by surface recombination around the perimeter of the cell, should not depend on the growth process. We believe the difference is one of aging of the cells. The single-temperature cells were measured one day after the mesas were etched, while the standard cells were measured 12 days after mesa etching. It is known that the freshly-etched GaAs surface has a low recombination velocity which increases with time. A higher recombination velocity increases the $n = 2$ current. Although we believe this is the explanation, the difference between the two curves is striking and further work should be done to confirm our hypothesis.

Figure 3-24. Comparison of Internal Quantum Efficiencies for Cells grown by the Standard Two-temperature Process (Lot 5171) and by the Single-temperature Process (Lot 5184). The numbers after the cell identification are the emitter doping concentration, AlGaAs window composition, and window thickness

Figure 3-25. Comparison of Log I-V Curves for Cells Grown by the Two Processes. The cells were measured before removal of the GaAs cap layer

Table 3-16. Comparison of Wafer-average Saturation Currents for Cells Grown by the Standard Two-temperature and New Single-temperature Methods. Standard deviations are shown in parentheses. There were 23 cells measured from run 1423 and 35 from run 1459. Cell area was 0.25 cm^2 and the temperature was 25°C .

Process Lot	MOCVD Run	Type	J_{01} (A/cm^2)	J_{02} (A/cm^2)
5172	1423	Standard	9.49×10^{-20} (0.70×10^{-20})	7.84×10^{-12} (1.49×10^{-12})
5185	1459	Single-Temp.	15.7×10^{-20} (0.82×10^{-20})	2.09×10^{-12} (0.22×10^{-12})

Table 3-17 compares the best-cell results for standard cells from Lot 5172 and single-temperature cells from this lot. The single-temperature cells have lower V_{OC} , as expected from higher $n = 1$ dark current, and lower J_{SC} , from the lower blue response. However, the difference in both parameters is larger than expected from the IQE and log I-V data, and the fill factor should be larger for the single-temperature cells, based on lower $n = 2$ dark current. The discrepancy is caused by the trench formation processing problem discussed above. Although this problem was seen in both process lots of Table 3-16, it was much more severe for the single-temperature cell wafer. The efficiency measurements therefore do not present a fair comparison between the two growth processes. The data of Figures 3-23 and 3-24, measured before the cap etch was performed, are more representative.

Table 3-17. Comparison of Best-cell Efficiency Results from Lots 5172 (standard growth process) and 5185 (single-temperature growth process). Test conditions: AM1.5 Global, $100 \text{ mW}/\text{cm}^2$, no spectral mismatch correction, 25°C , total area.

Process Lot	MOCVD Run	Type	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Eff. (%)
5172	1423	Standard	1.036	27.86	84.6	24.4
5185	1459	Single-Temp.	1.014	26.94	83.1	22.7

To summarize, the single-temperature growth method resulted in cells with a very low window/emitter recombination velocity, as desired. However, some recent cells with the standard process have also had low recombination velocities, so this is not an improvement. Although there were minor differences, cell performance was similar to recent record-efficiency cells grown by the standard process. The advantage we see for single-temperature growth, which is not discussed in detail in this report, is better reproducibility of composition and thickness of thin AlGaAs window layers.

3.4.3 Short Circuit Current Loss Analysis

We have performed an analysis of internal losses in the 24.3% efficient cells from Lot 5188, reported in Section 3.3.2. The analysis was carried out by fitting the measured internal quantum efficiency with our analytical model, and comparing to a modeled cell with no losses. The results are summarized in Table 3-18.

Table 3-18. Short Circuit Current Internal Loss Analysis for a 24.3% Efficient Cell from Lot 5188. Current densities are in mA/cm². External losses (reflectance and grid shadow) are not included.

Layer	Window	Emitter	SCL	Base	Total
Theor. Max. J _{sc}	1.76	17.77	2.56	9.56	31.64
Measured J _{sc}	0.51	17.75	2.56	8.82	29.64
J _{sc} Loss	1.25	0.02	0.00	0.73	2.00

The lost current is approximately 2/3 from the window and 1/3 from the base. Collection from the emitter and space charge layer (SCL) is essentially complete. The window loss results from a high recombination velocity at the AlGaAs free surface and a low minority carrier diffusion length in the AlGaAs, while the base loss is caused by a diffusion length lower than the radiative limit. The window loss can be reduced by making the window thinner, while the base loss can be reduced by optimizing the MOCVD growth conditions for long diffusion lengths. These should be areas for future work.

3.4.4 Dislocation Density Effects, Lot 5196

GaAs_{1-y}P_y buffer layers with different compositions (y) were grown on GaAs substrates and used to introduce controlled amounts of growth defects into GaAs cell structures grown on the buffers. (The lattice mismatch and dislocation density increase with y). The resulting wafers were used to assess the effects of dislocations on GaAs cell efficiency. By comparing the results to those of GaAs-on-Si cells, which have other materials problems in addition to dislocations (thermal expansion cracks, silicon autodoping, and possibly antiphase boundaries), we can address the question of whether dislocations are the dominant problem in GaAs-on-Si material.

The results of efficiency measurements at Spire are summarized in Table 3-19 and Figure 3-26. As expected, there is a loss of efficiency with increasing lattice mismatch between the GaAsP buffer and GaAs cell layers. (The percent mismatch is given by $3.575y$; y was determined by photoluminescence.) Although the efficiency decreases, the wafer average efficiency is still 22% for 0.3% mismatch. V_{oc}, J_{sc}, and FF all decrease, but at different rates. This is shown in Figure 3-27, with all parameters normalized to cells with no lattice mismatch.

Table 3-19. Lot 5196 Efficiency Summary (AM1.5 global, 100 mW/cm², 25°C, corrected for spectral mismatch)

Cell ID	y in GaAs _{1-y} P _y	Best Cells			Eff. (%)	Base L _h (μm)
		V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)		
1512-1-20	0.00	1.029	27.29	87.2	24.4	4.32
1513-1-18	0.00	1.028	27.58	86.5	24.5	4.16
1511-3-21	0.02	1.032	26.96	86.1	23.9	3.86
1511-1-35	0.05	1.016	26.78	84.4	23.0	3.45
1513-4-26	0.07	1.016	27.18	83.9	23.1	3.49
1512-4-15	0.08	1.009	27.05	83.2	22.8	3.24
1512-2-39	0.18	0.859	25.74	78.5	17.4	1.64
1511-5-2	0.27	0.793	24.65	77.2	15.1	1.16

Wafer Averages, Standard Deviations

Wafer ID	Mismatch (%)	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff. (%)	# of Cells
1512-1	0.00	1.030 (0.001)	27.14 (0.18)	86.1 (0.8)	24.1 (0.3)	25
1513-1	0.00	1.029 (0.003)	27.44 (0.16)	85.6 (0.6)	24.2 (0.3)	29
1511-3	0.07	1.031 (0.002)	26.73 (0.16)	85.4 (0.9)	23.5 (0.3)	40
1511-1	0.18	1.016 (0.003)	26.51 (0.22)	83.4 (0.9)	22.5 (0.3)	39
1513-4	0.25	1.015 (0.003)	27.00 (0.16)	82.9 (0.9)	22.7 (0.3)	39
1512-4	0.29	1.008 (0.004)	26.39 (0.42)	82.2 (1.4)	21.9 (0.6)	28
1512-2	0.64	0.835 (0.013)	25.32 (0.33)	77.6 (0.7)	16.4 (0.5)	37
1511-5	0.97	0.787 (0.007)	24.22 (0.22)	76.4 (0.7)	14.5 (0.3)	39

a

b

c

d

Figure 3-26. Efficiency Results as a Function of Buffer Lattice Mismatch for GaAs Cells in Lot 5196. (a) AM1.5 efficiency, (b) open circuit voltage, (c) short circuit current density, (d) fill factor. The curves are intended only to guide the eye

Figure 3-27. Normalized Efficiency Parameters as Functions of Buffer Lattice Mismatch. Values are normalized to GaAs control cells

While J_{sc} and FF decrease at roughly constant rates with mismatch, V_{oc} shows only minimal losses below 0.3% mismatch and a large drop between 0.3 and 0.6%. The log I-V curves in Figure 3-28 can be used to explain this behavior. The major effect of mismatch is to increase the $n = 2$ component of dark current. Because the fill factor is controlled by $n = 2$ current, it is sensitive to all levels of mismatch. The V_{oc} , however, is largely controlled by the $n = 1$ current for GaAs cells, and small amounts of mismatch appear to have little effect on the $n = 1$ current. The small decreases in V_{oc} below 0.4% mismatch are due to the increasing importance of the $n = 2$ current, but the $n = 1$ current is still significant. Above 0.6% mismatch, the $n = 1$ current is completely swamped by the $n = 2$ current, and so V_{oc} drops sharply. Figure 3-29 shows the dependence of the $n = 1$ and $n = 2$ saturation currents on lattice mismatch.

The log I-V results also give us information about bulk vs. surface space-charge recombination currents. We have previously determined that the $n = 2$ current for GaAs cells is dominated by surface space-charge recombination. It scales with the junction perimeter and changes with time as the unpassivated GaAs surface changes. In this lot we saw the value of J_{o2} increase by a factor of 2 over a period of 3 weeks for the GaAs control cells. However, the value of J_{o2} did not change for cells with more than 0.1% lattice mismatch.

Figure 3-28. Log I-V Curves for GaAs Cells with Different Amounts of Buffer Lattice Mismatch

Figure 3-29. Dependence of Diffusion Saturation Current (J_{o1}) and Space-charge-recombination Saturation Current (J_{o2}) on Buffer Lattice Mismatch

The cells with more mismatch also had slightly lower n -values, closer to 1.85 than 2.0. Both the n -value and temporal invariance point to bulk space-charge recombination as the dominant mechanism in cells with significant mismatch. Presumably the dislocations caused by lattice mismatch are acting as recombination centers in the junction space-charge layer. To summarize, the major effect of lattice mismatch on V_{oc} and FF is from increased $n = 2$ current attributed to bulk space-charge recombination.

The cause of the short-circuit current decrease can be seen in the quantum efficiency curves of Figure 3-30. For large mismatch ($>0.5\%$), there is a noticeable decrease in the red response caused by lower base diffusion length. For small mismatch, the effects are more subtle. Reduced collection from both the emitter and base layers can be deduced from quantum efficiency modeling. Base diffusion lengths were included in Table 3-19.

To summarize the results, there appear to be two regions of lattice mismatch effects. For mismatch less than approximately 0.5%, there are small decreases in V_{oc} , FF, and J_{sc} attributed to crystal defects. Above 0.5% mismatch there is a large drop in V_{oc} caused by high $n = 2$ currents. The short circuit current is also affected significantly by reduced minority carrier diffusion lengths. Coincident with these changes is a noticeable degradation in surface morphology of the layers.

Figure 3-30. Internal Quantum Efficiency Curves for GaAs Cells with Different Amounts of Buffer Lattice Mismatch

Dislocation densities were measured by Electron Beam Induced Current (EBIC), Cathodoluminescence (CL), and Transmission Electron Microscopy (TEM) at SERI on characterized solar cells (AM1.5 efficiencies were also measured at SERI). Results of dislocation density and efficiency measurements on the same cells are summarized in Table 3-20, and Figures 3-31 and 3-32 present the results graphically. Figure 3-33 shows the dependence of base diffusion length on dislocation density.

Table 3-20. Dislocation Densities and AM1.5 Efficiencies Measured at SERI for GaAs Cells with Different Composition GaAsP Buffer Layers. The last two dislocation densities were measured by TEM; the others by EBIC or CL

Wafer	y in GaAs _{1-y} P _y	Dislocation Density (cm ⁻²)	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff (%)
1512-1	0.00	0	1.028	27.1	86.3	24.1
1513-1	0.00	8 x 10 ³	1.033	27.0	84.3	23.5
1511-3	0.02	3 x 10 ⁴	1.032	26.7	85.4	23.7
1511-1	0.05	3.3 x 10 ⁵	1.015	26.6	84.0	22.7
1513-4	0.07	5 x 10 ⁵	1.014	26.7	83.2	22.6
1512-4	0.08	4 x 10 ⁵	1.009	26.9	82.5	22.4
1512-2	0.18	1.5 x 10 ⁷	0.844	25.3	78.1	16.7
1511-5	0.27	7.3 x 10 ⁷	0.787	24.6	76.9	14.9

Figure 3-31. AM1.5 Efficiency as a Function of Dislocation Density for GaAs Cells Grown on GaAsP Buffer Layers. Also shown for comparison are Spire and NTT results for GaAs-on-Si cells

Figure 3-32. Efficiency Parameters as Functions of Dislocation Density for GaAs Cells Grown on GaAsP Buffer Layers (a) Open-circuit Voltage, (b) Short-circuit Current, (c) Fill Factor

Figure 3-33. Base Diffusion Length as a Function of Dislocation Density

The effects of intentional mismatch are very similar to results for GaAs-on-Si solar cells, as seen in Figure 3-31. Here we compare GaAs-on-Si results reported by Spire and the two groups at NTT [15,16] to the present experiment. Also shown is a theoretical curve from Dr. Yamaguchi's group at NTT, based on dislocation effects, which fits their data [15]. Note that the efficiency results of Spire and the other group at NTT are shifted upward, probably because of better cell processing technology, but follow the same general trend. The results support our previous conclusion that dislocations from lattice mismatch are the major problem with present GaAs-on-Si cells. Reducing the dislocations to the equivalent of 0.3% mismatch ($1 \times 10^6 \text{ cm}^{-2}$) should give efficiencies within 10% (relative) of GaAs-on-GaAs cells.

NTT's model includes a reduction in minority carrier diffusion length and lifetime due to recombination at dislocations. It is assumed that the dislocations are randomly spaced and that they act as perfect sinks of carriers. The diffusion length of holes is expressed as:

$$L_p^{-2} = L_0^{-2} + 3 \times 10^{-11} \cdot n + \pi^3 \cdot N_d / 4$$

where L_p is the hole diffusion length, L_0 is the intrinsic hole diffusion length at low doping levels, n is the doping concentration, and N_d is the dislocation density. The second term reflects an empirical reduction in dislocation density with doping in low-dislocation GaAs, and the third term is the dislocation effect. The model curve in Figure 3-33 uses a value of 10.5 microns for L_0 , to match the low-dislocation results, but has no other adjustable parameters. The model shows good agreement to the measured data for low

dislocation densities, but tends to underestimate the diffusion length for greater than 10^7 cm^{-2} dislocations. This is probably because of the dislocation counting method and the random-spacing assumption of the model. In heavily-dislocated material the dislocations interact and are clumped, not randomly spaced. TEM, used for high densities, counts the individual dislocations. Densities measured by TEM are typically higher than by EBIC, CL, or etch pit methods, which cannot resolve the clumped dislocations. Dislocation densities counted by one of these other methods, which correspond more closely to the assumptions of the model, would show better agreement.

It should be noted that the efficiencies of the GaAs control cells in this lot were very high, up to 24.5%. The wafer averages for the two control wafers were both over 24%. This is the fourth consecutive process lot with efficiencies over 24%, showing that our high-efficiency process is quite reproducible. It should also be noted that the process changes discussed in Section 3.2.2.1 were successful in preventing the formation of trenches along the grid lines.

3.4.5 Comparison of High Efficiency GaAs Cells Grown by MBE and MOCVD, Lot 5210

As part of our collaboration with Purdue University, Professor Michael Melloch has grown GaAs solar cell structures by MBE using Spire's standard high-efficiency structure. Two MBE wafers from Purdue and two MOCVD wafers from Spire were processed together to compare materials grown by the two processes. The results were excellent, with record-efficiency cells for both growth methods. Efficiencies of 24.8% for the MOCVD cells and 23.8% for the MBE cells were measured at SERI. The cells were analyzed to relate cell performance to materials properties of the two growth methods, and the reason for the 1 percentage point difference in efficiency has been identified. This work is summarized in a paper submitted to the IEEE Transactions on Electron Devices for a special issue on photovoltaics, and is included as Appendix B.

3.4.6 High Efficiency GaAs Concentrator Cells, Lot 5217

The cells described in this section were processed under funding from a different source for space applications. However, they were also tested under terrestrial conditions, and so the results are very applicable to this contract. Most of the process development leading up to these high efficiencies has been supported by SERI contracts over the years. The results demonstrate that high efficiencies at one sun are readily transferrable to concentrator cells.

GaAs cells grown on GaAs substrates were used for this work. The wafer was from one of the same MOCVD runs (#1527) used in the MOCVD versus MBE study reported in Section 3.4.5. The grid pattern was designed for 100 AM0 suns concentration and featured a 4 mm diameter circular active area on a 5 mm square die. Tall, narrow grid lines were formed by an evaporated metal liftoff process, with height and width of about 3 microns. The rest of the process was identical to our high-efficiency one-sun cells.

Results of efficiency versus concentration for the best cell are shown in Figure 3-34; individual efficiency parameters are listed in Table 3-21. The measurements were made at Sandia National Laboratories, courtesy of Dr. Doug Ruby, at AM0 and AM1.5, and at 25 and 80°C. At 25°C, the AM1.5 efficiency peaked at 28.7% at 200 suns. This value can be

Figure 3-34. Efficiency versus Concentration for the Best GaAs Concentrator Cell

Table 3-21. Efficiency Parameters at Different Concentrations for the Best GaAs Concentrator Cell (cell # 5217-1527-10). Test conditions: AM1.5 Direct, 1000 W/m², 0.125 cm² illuminated area

Temp. (°C)	I _{sc} (A)	V _{oc} (V)	FF (%)	Suns	Eff. (%)
25	0.003511	0.998	85.6	0.977	24.55
25	0.0183	1.044	86.0	5.09	25.81
25	0.0355	1.063	86.5	9.88	26.44
25	0.0720	1.079	87.1	20.02	27.02
25	0.1798	1.104	87.3	50.02	27.71
25	0.3523	1.124	87.6	98.01	28.31
25	0.7146	1.139	87.5	198.8	28.66
25	1.067	1.148	86.5	296.9	28.55
25	1.787	1.159	84.8	497.2	28.26
25	3.703	1.173	78.7	1030.	26.54
80	0.003708	0.886	82.4	0.977	22.17
80	0.0202	0.944	82.9	5.33	23.76
80	0.0375	0.963	83.8	9.89	24.50
80	0.0765	0.989	84.4	20.15	25.34
80	0.1911	1.015	84.9	50.36	26.16
80	0.3774	1.035	85.7	99.45	26.93
80	0.7664	1.054	85.5	202.0	27.36
80	1.153	1.065	84.2	303.9	27.22
80	1.907	1.079	82.0	502.6	26.86
80	3.745	1.094	74.9	986.8	24.88

1-sun short-circuit-current densities (mA/cm²):
 AM1.5D, 25°C: 28.75 (Sandia measurement)
 AM1.5D, 80°C: 30.36 (Sandia measurement)

compared to recent Varian results of 28.1% at 400 suns for GaAs cells without prismatic covers, and 29.2% at 200 suns for cells with prismatic covers. It can also be compared to Stanford's result of 28.2% at 150 suns for a silicon back point contact cell.

It should be noted that there was a substantial disagreement in AM1.5D one-sun short-circuit currents between Spire's and Sandia's measurements. Both measurements used silicon reference cells and spectral mismatch corrections to determine the one-sun currents. Sandia's reference cell was calibrated by NASA, while Spire's was calibrated by JPL.

As an independent check, we also determined the one-sun J_{sc} using absolute spectral response curves measured by Spire and Sandia and the reference AM1.5 direct spectrum. All of these measurements are summarized in Table 3-22. The quantum efficiency measurements were in relatively good agreement and fell between the two simulator measurements. We have chosen to report Sandia's reference cell value for two reasons. First, Sandia is the de facto standards laboratory for concentrator cell measurements. The same test procedure was used for other high efficiency concentrator cells reported in the literature. Second, Sandia finds good agreement between these indoor simulator measurements and outdoor concentrator measurements. When the same comparison was made for AM0 conditions, one-sun short-circuit currents were in good agreement by all methods (Table 3-22).

Table 3-22. Comparison of Measured One-sun J_{sc} (mA/cm²) for GaAs Concentrator Cell.

Spectrum	Spire		Sandia	
	Simulator	Spectral Response	Simulator	Spectral Response
AM1.5D	25.72	26.79	28.75	26.16
AM0	32.92	33.22	33.61	33.42

3.5 AlGaAs SOLAR CELLS

3.5.1 AlGaAs Cells, Lots 5168 and 5195

As part of our ongoing collaboration, Professor Mark Lundstrom at Purdue University requested some 1.7 eV AlGaAs solar cells for analysis. The goal is to study the physics of AlGaAs cells, similar to what has been done for GaAs in the last few years. Because we had no good AlGaAs solar cells in stock, three previously-grown wafers were processed into cells. Wafers from these same MOCVD runs had been previously processed, giving high efficiencies [12].

After the cells were metallized and the junctions were defined by mesa etching, but before antireflection coating, each wafer was split in half. One half was sent to Purdue for electrical measurements, and the other half was antireflection-coated at Spire. Unfortunately, the AlGaAs windows oxidized before the AR-coated cells could be measured. This was a common problem in cell material grown several years ago, before we had a way to monitor and control the AlGaAs composition. Reflectance modeling

showed that the window layers in these cells were nearly pure AlAs at the surface, explaining the rapid oxidation. Because internal quantum efficiency data is needed for modeling, another attempt was made to measure the cells' quantum efficiencies. A half wafer of AlGaAs cells was returned to Spire from Purdue. The GaAs cap layer was stripped from the cells and then internal quantum efficiency was immediately measured. The quantum efficiency was used to calculate an AM1.5 short circuit current. The log I-V characteristics were also remeasured for each cell, and used to determine the V_{oc} , fill factor, and efficiency at one sun. We also used photoluminescence to measure the band gap of each cell, an important parameter for cell modeling. The results, summarized in Table 3-23, are similar to what was measured several years ago on other wafers from this same MOCVD run [12].

Table 3-23. Efficiency Values Calculated for AlGaAs Cells from Lot 5195, Wafer 519-5, using Quantum Efficiency and Log I-V Data. (AM1.5 Global, 100 mW/cm², 25.0°C, total area)

Cell #	E _g (eV)	J ₀₁ (A/cm ²)	J ₀₂ (A/cm ²)	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff. (%)
3	1.653	5.05E-23	7.25E-13	1.196	17.79	83.45	17.76
4	1.653	5.71E-23	3.82E-12*	1.195	17.80	82.75	17.60
8	1.656	4.49E-23	3.08E-13	1.210	18.00	85.28	18.57
9	1.655	4.03E-23	4.08E-13	1.210	18.14	84.26	18.49
10	1.652	4.05E-23	5.22E-13	1.206	17.98	83.61	18.13
15	1.660	3.26E-23	2.99E-13	1.217	17.82	84.81	18.39
16	1.657	3.61E-23	3.47E-13	1.214	18.17	84.35	18.65
17	1.652	3.97E-23	4.66E-13	1.209	18.34	83.89	18.60
23	1.663	3.78E-23	2.95E-13	1.213	17.35	85.14	17.92
24	1.658	4.05E-23	3.22E-13	1.212	17.95	85.00	18.49
25	1.652	4.85E-23	4.18E-13	1.206	18.19	84.64	18.57
26	1.647	6.27E-23	5.39E-13	1.199	18.90	84.36	19.12
31	1.665	2.74E-23	1.98E-13	1.223	17.45	85.55	18.26
32	1.661	3.20E-23	2.31E-13	1.219	17.51	85.39	18.23
33	1.653	4.50E-23	2.43E-13	1.212	18.23	85.66	18.93
34	1.644	6.23E-23	2.99E-13	1.205	19.02	85.68	19.64
38	1.666	2.50E-23	2.88E-13	1.221	16.68	84.65	17.24
39	1.662	3.33E-23	2.27E-13	1.218	17.27	85.50	17.98
40	1.654	4.51E-23	2.66E-13	1.211	18.15	85.59	18.81
43	1.665	3.09E-23	9.01E-12*	1.210	17.11	82.42	17.06
44	1.661	3.15E-23	1.99E-13	1.221	17.77	85.80	18.62

* $n_2 = 2.16$ for #4, $n_2 = 2.28$ for #43.

SECTION 4.0

CHARACTERIZATION TECHNIQUES

4.1 OPTICAL REFLECTANCE SPECTROSCOPY

The optical reflectance analysis program, REFIT, which has been extremely useful in characterizing AlGaAs window layers, has been upgraded to allow up to three different layers with different AlGaAs compositions to be analyzed. The AlGaAs compositions and thicknesses can be used as fitting variables. This is being used to check for compositional transients at the two interfaces of the window, and to check for compositional grading in the window. In several cases we have achieved much better fits with the multilayer model and have used this information to improve the growth process. Our work in this area has been submitted for publication in the IEEE Transactions on Electron Devices special issue on photovoltaics scheduled for February, 1990.

We have also begun a systematic evaluation of the sources of error in our reflectance measurement apparatus and the effects of errors on the fitting results. For thin AlGaAs layers, 500 angstroms or less, the measured composition is quite sensitive to absolute reflectance errors. To maintain ± 0.02 accuracy in AlGaAs mole fraction, the reflectance must be accurate to $\pm 0.5\%$. This appears to be achievable with the present apparatus.

4.2 DOPING MEASUREMENTS

The results of cell modeling analyses, particularly of the dark current, are sensitive to the doping concentrations in the n- and p-GaAs layers. We have therefore adopted several techniques for measuring these parameters on cell wafers, rather than relying on target values.

Doping levels in the emitter and base can be measured by electrochemical capacitance-voltage (ECV) profiling using a Polaron profiler. However, this is a destructive technique, and is not easily performed on actual cells. We have instead used the zero-bias junction capacitance to measure the base doping. Most of the depletion layer is in the base (n-type) because its doping is 20 times less than in the emitter (p-type). However, for maximum accuracy, the analysis takes into account the emitter doping as well. The capacitance of standard-sized cells (0.25 cm^2) is too large for our capacitance meter (maximum 3000 pF), so small test diodes adjacent to the cells are used. This allows many measurements per wafer to be made.

An idea of the cap and emitter dopings (p-type) can be obtained from sheet resistance measurements before and after the cap is removed. Sheet resistance measurements are made on transmission line patterns adjacent to each cell. Resistivity is calculated from sheet resistance and layer thickness, and doping is calculated using Hall data of resistivity versus doping. This is fairly accurate for the cap layer, because its thickness is accurately known from optical reflectance spectroscopy. It is not as accurate for the emitter because we do not measure its thickness directly, and because the doping is not constant throughout the layer (there is a doping spike adjacent to the AlGaAs window layer). Therefore, the most reliable way to measure the emitter doping remains ECV profiling on test samples.

4.3 THIN AlGaAs UNIFORMITY

We made two MOCVD runs specifically to evaluate the uniformity of thin AlGaAs window layers. The nominal structure was 300 angstroms of $x = 0.8$ AlGaAs on GaAs. The continuous growth process was used, with both layers grown at 740°C . Two consecutive runs (MO2-1514, MO2-1515) were made with five two-inch wafers in each run. Nine spots on each wafer, as shown in Figure 4-1, were measured by ellipsometry. To interpret the data we assumed a constant composition AlGaAs layer with no surface oxide. The thickness was determined directly from ellipsometry, while the AlGaAs composition was determined from the refractive index, using the conversion in Figure 4-2. To check the ellipsometry results, we used optical reflectance on one spot at the center of each wafer.

Figure 4-1. Location of Measured Spots on the 2-inch Wafers

Figure 4-2. Relationship Between AlGaAs Composition and Refractive Index at 632.8 nm [17]

4.3.1 Ellipsometry Results

The ellipsometry measurements were made twice. The first set was done one day after MOCVD growth, with six of the ten wafers measured (9/29/88). The second set was done one week later, and all 10 wafers were measured (10/6/88). The first data set allowed comparisons only within the first MOCVD run. The second data set was complete for both runs, but the accuracy was compromised by oxidation of the AlGaAs layer.

Table 4-1 summarizes the uniformity results from the first data set. Table 4-2 shows all of the measured thicknesses and compositions. In this table the wafers are shown in the same orientation as on the susceptor in the MOCVD reactor, so that spatial trends can be visualized. Table 4-3 summarizes the uniformity results from the second data set, and Table 4-4 shows the measured values.

Table 4-1.

Summary of Thickness and Compositional Uniformity for Thin AlGaAs Layers Grown in SPI-MO CVDTM 450 Atmospheric Pressure Reactor. Data were measured by ellipsometry on nine spots per wafer on 9/29/88. Thicknesses are in angstroms

MOCVD Run	Wafer	Thickness			Composition		
		Mean	S.Dev.	Range	Mean	S.Dev.	Range
1514	1	275	$\pm 4.1\%$	$\pm 6.9\%$	0.863	$\pm 1.7\%$	$\pm 2.7\%$
1514	2	299	$\pm 2.9\%$	$\pm 5.4\%$	0.855	$\pm 0.6\%$	$\pm 0.9\%$
1514	3	318	$\pm 2.6\%$	$\pm 4.3\%$	0.848	$\pm 0.6\%$	$\pm 1.1\%$
1514	4	308	$\pm 2.6\%$	$\pm 4.9\%$	0.869	$\pm 0.9\%$	$\pm 1.7\%$
1514	5	280	$\pm 4.1\%$	$\pm 5.9\%$	0.877	$\pm 1.4\%$	$\pm 2.0\%$
1514 Run Average		296	$\pm 6.4\%$	$\pm 12.2\%$	0.862	$\pm 1.6\%$	$\pm 3.4\%$
1515	1	299	$\pm 4.1\%$	$\pm 6.7\%$	0.829	$\pm 1.2\%$	$\pm 2.1\%$

Table 4-2. AlGaAs Thickness and Composition Data for 54 Points on Six Wafers Measured by Ellipsometry on 9/29/88. The gas flow direction was from top to bottom of the page

Wafer 1	2	3	4	5
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Run 1514														
Thickness (Å)														
265	264	270	294	293	297	312	313	320	305	303	308	269	271	283
261	279	282	288	300	298	310	321	314	299	310	304	265	282	289
273	299	284	294	320	303	306	333	329	306	328	309	269	298	294
Composition														
0.87	0.88	0.88	0.86	0.85	0.85	0.85	0.85	0.85	0.88	0.87	0.87	0.89	0.89	0.88
0.87	0.87	0.86	0.86	0.85	0.86	0.85	0.85	0.85	0.88	0.87	0.87	0.89	0.87	0.87
0.86	0.85	0.83	0.87	0.85	0.85	0.86	0.84	0.84	0.87	0.85	0.86	0.89	0.86	0.86

Run 1515														
Thickness (Å)														
303	289	288												
310	298	281												
312	321	293												
Composition														
0.83	0.84	0.84												
0.84	0.83	0.83												
0.83	0.81	0.82												

Table 4-3. Summary of Thickness and Compositional Uniformity for Thin AlGaAs Layers Grown in SPI-MO CVD 450 Atmospheric Pressure Reactor. Data were measured by ellipsometry on nine spots per wafer on 10/6/88. Thicknesses are in angstroms

MOCVD		Thickness			Composition		
Run	Wafer	Mean	S.Dev.	Range	Mean	S.Dev.	Range
1514	1	264	$\pm 4.1\%$	$\pm 6.6\%$	0.970	$\pm 1.4\%$	$\pm 2.5\%$
1514	2	288	$\pm 2.9\%$	$\pm 5.4\%$	0.938	$\pm 1.3\%$	$\pm 2.3\%$
1514	3	303	$\pm 2.4\%$	$\pm 4.0\%$	0.934	$\pm 1.1\%$	$\pm 1.7\%$
1514	4	294	$\pm 2.3\%$	$\pm 4.1\%$	0.963	$\pm 1.4\%$	$\pm 2.1\%$
1514	5	269	$\pm 3.7\%$	$\pm 5.8\%$	0.997	$\pm 1.9\%$	$\pm 3.1\%$
1514 Run Average		284	$\pm 6.1\%$	$\pm 12.3\%$	0.961	$\pm 2.8\%$	$\pm 5.8\%$
1515	1	288	$\pm 3.9\%$	$\pm 6.4\%$	0.902	$\pm 1.1\%$	$\pm 2.1\%$
1515	2	259	$\pm 3.3\%$	$\pm 5.0\%$	0.939	$\pm 2.0\%$	$\pm 2.8\%$
1515	3	254	$\pm 5.7\%$	$\pm 8.1\%$	0.939	$\pm 1.6\%$	$\pm 2.6\%$
1515	4	282	$\pm 3.9\%$	$\pm 6.2\%$	0.909	$\pm 1.7\%$	$\pm 2.6\%$
1515	5	310	$\pm 2.5\%$	$\pm 4.0\%$	0.885	$\pm 1.2\%$	$\pm 2.1\%$
1515 Run Average		279	$\pm 8.2\%$	$\pm 17.2\%$	0.915	$\pm 2.8\%$	$\pm 5.7\%$
Overall Batch		281	$\pm 7.3\%$	$\pm 17.1\%$	0.938	$\pm 3.7\%$	$\pm 8.4\%$

Table 4-4. AlGaAs Thickness and Composition Data for 90 Points on 10 Wafers Measured by Ellipsometry on 10/6/88, after Slight AlGaAs Oxidation. The gas flow direction was from top to bottom of the page

Wafer 1			2			3			4			5		
Run 1514														
Thickness (Å)														
254	254	263	281	281	285	299	298	303	292	287	292	259	260	272
250	266	268	278	288	286	297	305	300	290	297	292	256	271	275
261	285	277	288	308	293	296	320	311	289	311	298	261	287	280
Composition														
0.99	0.98	0.98	0.94	0.95	0.95	0.94	0.95	0.94	0.97	0.97	0.97	0.02	0.02	0.00
0.98	0.97	0.97	0.95	0.93	0.94	0.94	0.92	0.94	0.98	0.96	0.96	0.02	0.99	0.00
0.97	0.94	0.96	0.94	0.91	0.94	0.95	0.92	0.92	0.98	0.94	0.95	0.00	0.96	0.98
Run 1515														
Thickness (Å)														
296	279	278	253	252	266	243	250	262	270	277	289	310	306	305
299	288	269	246	259	268	230	257	269	263	286	289	306	311	301
294	306	282	250	272	265	236	271	270	274	298	294	302	326	319
Composition														
0.90	0.91	0.91	0.96	0.95	0.93	0.95	0.95	0.94	0.92	0.91	0.90	0.89	0.89	0.88
0.90	0.90	0.91	0.97	0.93	0.92	0.96	0.93	0.93	0.94	0.90	0.90	0.89	0.88	0.89
0.91	0.88	0.90	0.96	0.92	0.92	0.95	0.91	0.93	0.92	0.89	0.90	0.90	0.87	0.88

In general, the uniformity within a wafer was quite good, averaging $\pm 3.4\%$ in thickness and $\pm 1.1\%$ in AlGaAs composition (9/29 data). The wafer-to-wafer uniformity was not as good. For the two MOCVD runs the thickness uniformity was ± 6.1 and $\pm 8.2\%$, and the compositional uniformity was $\pm 2.8\%$ in both cases (10/6 data). The reason is a systematic variation around the susceptor, as shown in Figures 4-3 and 4-4. In these figures we have plotted the thicknesses for the top, middle, and bottom of each wafer as a function of distance around the susceptor. A clear sinusoidal trend is observed. A similar variation in composition was seen, with thicker layers generally having lower compositions. The variation around the susceptor is believed to result from asymmetry in gas flow in the reactor. It should be noted that the susceptor completed only part of one rotation during the growth of these thin AlGaAs layers. There are also trends within each wafer, such as greater thickness toward the bottom of the wafer and largest thickness at the bottom center.

The run-to-run thickness reproducibility was very good. The compositions were generally lower for run 1515, but this is partly an artifact of the measurement, as discussed below.

Figure 4-3. Variation of AlGaAs Thickness Around the Susceptor from Run MO2-1514

Figure 4-4. Variation of AlGaAs Thickness Around the Susceptor from Run MO2-1515

4.3.2. Reflectance Results

The reflectance spectra were analyzed in two ways. First, the reflectance was fit by a two-layer model with a surface oxide and a constant composition AlGaAs layer. For the initial data, Table 4-5 compares the ellipsometry and reflectance results for the center of each wafer, and Figure 4-5 shows bar charts of thickness for the same points. The numbers above the bars are the AlGaAs composition. The fits were not great, indicating that the actual structure is more complicated. Nevertheless, several points are apparent: 1) the AlGaAs composition is lower than from ellipsometry, more in line with the target value. Reasons for this are discussed below. 2) the thicknesses are in good agreement with the ellipsometry values.

Table 4-6 lists similar data for the second set of measurements. The reflectance data show evidence of oxidation in a thicker oxide layer and a slight reduction in the AlGaAs thickness. The AlGaAs compositions are in good agreement on the two days. It can be seen that the disagreement between ellipsometry and reflectance increases with increasing oxidation.

Much better reflectance fits were obtained when a multiple-layer AlGaAs structure was assumed. The best fits were for a three-layer structure with $x = 0.75$ at the surface, $x = 1.00$ below it, and $x = 0.7-0.8$ next to the GaAs. In reality there is probably some grading present, but the best we can do with the model at present is approximate the grading with discrete steps. We tried adding an oxide layer at the surface of the three-layer model but it gave little improvement in the fits. Table 4-7 summarizes the 3-layer parameters for the center of each wafer, and Figure 4-6 shows bar charts of thickness (9/29 data). The numbers above the bars are the AlGaAs composition of the layer closest to the substrate.

Table 4-5. Comparison of Ellipsometry and 2-layer Reflectance Results for the Center of Each Wafer; 9/29/88 Data. Thicknesses are in angstroms

Wafer	ELLIPSOMETRY		REFLECTANCE			
	AlGaAs Thick.	AlGaAs x	Oxide Thick.	AlGaAs Thick.	Total Thick.	AlGaAs x
1514-1	279	0.861	20	266	286	0.826
1514-2	300	0.851	6	295	301	0.822
1514-3	321	0.851	10	314	324	0.825
1514-4	310	0.867	11	305	316	0.832
1514-5	282	0.874	9	274	283	0.824
Average	298	0.861	11	291	302	0.826
1515-1	298	0.834	7	288	295	0.813
1515-2			19	254	273	0.808
1515-3			23	251	274	0.783
1515-4			31	285	316	0.787
1515-5			16	322	338	0.801
Average			19	280	299	0.798

RUN 1514 REFLECTANCE RESULTS

RUN 1515 REFLECTANCE RESULTS

Figure 4-5. Results of Double-layer Reflectance Modeling for the Thickness at the Center of each Wafer. The top layer is oxide, and the bottom layer is AlGaAs. The AlGaAs composition is indicated above each bar. (a) Run 1514, (b) Run 1515

Table 4-6. Comparison of Ellipsometry and Two-layer Reflectance Results for the Center of Each Wafer; 10/6/88 Data

Wafer	ELLIPSOmetry		REFLECTANCE			
	AlGaAs Thick.	AlGaAs x	Oxide Thick.	AlGaAs Thick.	Total Thick.	AlGaAs x
1514-1	266	0.966	31	261	292	0.815
1514-2	288	0.929	29	288	317	0.820
1514-3	305	0.922	28	309	337	0.818
1514-4	297	0.957	39	295	334	0.830
1514-5	271	0.986	38	264	302	0.821
Average	285	0.952	33	283	316	0.821
1515-1	288	0.899	18	287	305	0.809
1515-2	259	0.932	38	248	286	0.804
1515-3	257	0.932	42	247	289	0.776
1515-4	286	0.897	47	280	327	0.787
1515-5	311	0.880	24	320	344	0.782
Average	280	0.908	34	276	310	0.792

Table 4-7. Comparison of Ellipsometry and 3-layer Reflectance Results for the Center of Each Wafer; 9/29/88 Data

Wafer	ELLIPSOmetry		REFLECTANCE				
	Thick.	x	Top x = 0.75	Middle x = 1.0	Bottom Thick.	x	Total Thick.
1514-1	279	0.861	61	72	144	0.748	277
1514-2	300	0.851	70	60	170	0.768	300
1514-3	321	0.851	67	58	195	0.786	320
1514-4	310	0.867	61	69	182	0.780	312
1514-5	282	0.874	65	67	150	0.751	282
Average	298	0.861	65	65	168	0.767	298
1515-1	298	0.834	73	58	164	0.747	295
1515-2			66	64	138	0.717	268
1515-3			66	54	146	0.706	266
1515-4			59	51	188	0.742	298
1515-5			69	48	214	0.760	331
Average			67	55	170	0.734	292

RUN 1514 REFLECTANCE RESULTS

RUN 1515 REFLECTANCE RESULTS

Figure 4-6. Results of Triple-layer Reflectance Modeling for the Thickness at the Center of Each Wafer. The top layer is $x = 0.75$ AlGaAs, the middle layer is AlAs, and the bottom layer is AlGaAs. The bottom AlGaAs composition is indicated above each bar. (a) Run 1514, (b) Run 1515

The top two layers were on the order of 60 angstroms thick, and may be caused by transients at the end of growth. (Normally a GaAs cap layer is grown immediately after the AlGaAs window, so these transients are not present in the windows of solar cells.) The total thicknesses were in excellent agreement with the ellipsometry values.

Table 4-8 lists the same data for the 10/6/88 measurement. As with the 2-layer fits, the reflectance data is consistent before and after oxidation, while the ellipsometry data is thrown off by oxidation.

Table 4-8. Comparison of Ellipsometry and 3-layer Reflectance Results for the Center of Each Wafer; 10/6/88 Data

ELLIPSOmetry				REFLECTANCE			
Wafer	Thick.	x	Top x = 0.75	Middle x = 1.0	Bottom Thick.	x	Total Thick.
1514-1	266	0.966	56	61	156	0.753	273
1514-2	288	0.929	57	56	185	0.776	298
1514-3	305	0.922	53	44	219	0.792	316
1514-4	297	0.957	44	68	197	0.792	309
1514-5	271	0.986	49	69	162	0.758	280
Average	285	0.952	52	60	184	0.774	295
1515-1	288	0.899	69	55	172	0.750	296
1515-2	259	0.932	55	65	145	0.723	265
1515-3	257	0.932	52	56	158	0.717	266
1515-4	286	0.897	47	54	196	0.748	297
1515-5	311	0.880	57	33	238	0.764	328
Average	280	0.908	56	53	182	0.740	290

We can make two conclusions from the reflectance analysis: (1) the AlGaAs composition varied with depth in the layer, and (2) different wafers and different spots had different amounts of surface oxide. Both of these factors compromise the ellipsometry results for AlGaAs composition. Figure 4-7 shows the effect of surface oxide on the composition and thickness measured by ellipsometry. Here we have taken measured values of delta and psi and analyzed them using different thicknesses of a surface oxide layer. Although a thin oxide has very little effect on the calculated thickness, it has a large effect on the composition. The calculated composition decreases by 0.004 for each angstrom of oxide. It can also be seen that the assumption of no oxide when analyzing the ellipsometry data will cause the AlGaAs composition to be overestimated. This explains why the ellipsometry compositions were higher than the target value or the reflectance results. It also explains why the second set of ellipsometry measurements appeared to have higher compositions. The fact that run 1515 was measured after run 1514, and appeared to have more oxide, explains some of the apparent compositional difference between the two runs in the ellipsometry results. Only 4 angstroms of oxide could account for the difference. However, the reflectance results indicate that there was a real compositional difference of about 0.03 between the two runs.

Figure 4-7. Effect of Surface Oxide on the Composition and Thickness Measured by Ellipsometry

The conclusion is that the ellipsometry data for AlGaAs thickness is quite accurate, but the ellipsometry compositions are not reliable on an absolute scale. They may be reliable on a relative scale, but only if the oxide thickness is the same for all measurements.

4.3.3 Summary

The uniformity of thickness and composition for thin AlGaAs layers has been evaluated by ellipsometry and optical reflectance. Two consecutive runs of five 2-inch wafers each were made. Best results were as follows:

Within a wafer:	Thickness	$\pm 2.3\%$ std. dev.,	$\pm 4.0\%$ total range
	Composition	$\pm 0.6\%$ std. dev.,	$\pm 0.9\%$ total range
Within a run:	Thickness	$\pm 6.1\%$ std. dev.,	$\pm 12.3\%$ total range
	Composition	$\pm 1.6\%$ std. dev.,	$\pm 3.4\%$ total range
Both runs:	Thickness	$\pm 7.3\%$ std. dev.,	$\pm 17.1\%$ total range
	Composition	$\pm 3.7\%$ std. dev.,	$\pm 8.4\%$ total range

4.4 QUANTUM EFFICIENCY MODEL

Two changes have been made to our quantum efficiency model in an effort to improve the agreement between measured data and theory. First, we now have the option of using different absorption coefficient data files for the GaAs layers. Because the absorption coefficient of GaAs varies with carrier type and doping, and we were previously using data for undoped GaAs, this should improve the fits. Absorption coefficient data files have been created for several different dopings, using data from Casey [18]. Absorption coefficient values for arbitrary dopings are obtained by a 3-dimensional cubic spline to the measured data. Second, we have changed the model to allow different absorption coefficients for each layer of the cell. We can now use p-type data for the p-type layers and n-type data for the n-layers.

The new model has shown improved agreement with measured data at wavelengths near the band gap of GaAs. Because most of this light is absorbed in the base, the fit is sensitive to the data file used for the base, but not the emitter. While exercising the model it was noted that heavy p-type doping extends the response region of a GaAs cell to longer wavelengths, potentially increasing the short circuit current in an n-on-p configuration (provided that the diffusion length is large enough at higher dopings). For n-type GaAs the band gap changes little with doping, so that a similar effect would not be seen for p-on-n cells.

SECTION 5.0

THE EXPERIMENTAL RESULTS ACHIEVED IN THE SECOND YEAR OF THIS CONTRACT ARE FULLY DESCRIBED IN THE FIVE PUBLICATIONS ENCLOSED HERE.

ELECTRICAL PROPERTIES OF GaAs HOMOJUNCTIONS GROWN BY MOCVD ON GaAs AND Si SUBSTRATES

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Abstract—Several techniques, including DLTS, I - V - T , C - V - T , C - T and photoreflectance spectroscopy were used to investigate the electrical properties of GaAs multilayer heteroface p - n junctions epitaxially grown by MOCVD on GaAs or Si substrates in order to study the influence of heteroepitaxy on device properties. A deep level (EL2) was detected for both GaAs/GaAs and GaAs/Si structures. For GaAs/Si, a continuous distribution of trap levels was also observed which could be ascribed to misfit defects. I - V - T data revealed the saturation current of GaAs/Si diodes to be four orders in amplitude higher than for GaAs/GaAs ones. Different temperature dependences were found in saturation current density, barrier height and capacitance between the two structures. A multistep tunneling model is utilized in explaining the results for GaAs/Si. C - T measurements indicated that the free carriers are not frozen-out for GaAs/Si at the observed freeze-out temperature of GaAs/GaAs. Defect-induced bandgap tailing might be responsible for this effect.

1. INTRODUCTION

The epitaxial growth of GaAs on Si substrates has been of ever increasing importance with remarkable improvements in fabrication technology during the past few years[1]. The aim of placing GaAs epi-layers on Si (GaAs/Si) is to combine the well-known advantages of GaAs with the advantages of Si substrates such as light weight, low cost, large wafer size, high mechanical strength and monolithic integration for optoelectronics. Much effort and great strides have been made in solving the fundamental problems associated with the natural drawbacks such as the 4.1% lattice mismatch and the 59% difference in the thermal expansion coefficients. Some novel techniques like hydrogenation plus hydrogen annealing[2-4] and rapid thermal annealing (RTA)[4,5] have recently been used to reduce the density of line defects and the tensile stress.

Although much work has been done, the device performance of GaAs/Si heterostructures is still inferior to that of GaAs/GaAs homogeneous structures owing to the inevitable imperfectness from the misfit physical/chemical properties. Therefore, it is still of importance to have a better understanding of the difference in electrical properties between the homo- and hetero-epitaxial layers.

This work presents a combination of deep level transient spectroscopy (DLTS) and other characterization methodologies including current-voltage-temperature (I - V - T), capacitance-voltage-temperature (C - V - T), and capacitance-temperature (C - T) to study trap levels and current mechanisms of GaAs heretoface multilayer diodes grown on GaAs or Si substrates.

2. EXPERIMENT

The samples were originally designed for heteroface solar cells at Spire Corporation. All the epilayers were grown by MOCVD using a commercial 5-wafer SPI-MOCVD 450™ system[6]. The structure consisted of p^+ -GaAs/ p^+ -AlGaAs/ p^+ -GaAs/ n -GaAs/ n^+ -AlGaAs/ n^+ -GaAs epilayers on either n^+ -GaAs or n^+ -Si substrates as shown in Fig. 1. The wafers were cut into 3×3 mm² pieces and then cleaned with a trichloroethylene/acetone/methanol and DI water procedure. In and Ni were deposited on the front surface by thermal evaporation at a base pressure of 4×10^{-6} Torr. The metal deposition formed a circular contact of 1 mm diameter. The back contact was Au:Ge/Ni for GaAs substrates and Al for Si ones. Sintering was carried out at 400°C for 7 min in forming gas. Finally, wet etching in $H_2SO_4:H_2O_2:H_2$ (8:1:1) at 0°C was used to obtain rise-up mesa structures.

DLTS, C - V - T and C - T measurements were performed with a computer-controlled Bio-Rad Polaron S4600 DLTS spectrometer. I - V - T was done in an Air Products cryogenic refrigeration system fully controlled by computer. Photoreflectance spectra were taken at room temperature with a conventional setup[7]. The pump beam was from a 10 mW He-Ne laser with a chopping frequency of 150 Hz.

DLTS spectra were taken from 80 to 450 K with six fixed rate windows ranging from 1000 to 20 s⁻¹. The reverse bias varied from -1 to -4 V and the superposed filling pulse height varied from +0.6 to -1 V to study both minority and majority carrier traps[8].

		In/Ni	GaAs/GaAs	GaAs/Si
CAP	$p^+ - \text{GaAs}$	$> 10^{19} \text{ cm}^{-3}$	0.3 μm	0.3 μm
WINDOW	$p^+ - \text{Al}_{0.87}\text{Ga}_{0.13}\text{As} \sim 10^{18}$		350 $\text{\AA}$	500 $\text{\AA}$
EMITTER	$p^+ - \text{GaAs}$	2×10^{18}	1 μm	0.4 μm
BASE	$n - \text{GaAs}$	2×10^{17}	3 μm	3 μm
BUFFER	$n^+ - \text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$	2×10^{18}	1 μm	0.5 μm
BUFFER	$n^+ - \text{GaAs}$	2×10^{18}	1 μm	8 μm
SUBSTRATE	$n^+ - \text{GaAs}$	2×10^{18} 2° off (100)		
	OR $n^+ - \text{Si}$	5×10^{18} 2° off (100)		
			Au:Ge/Ni	Al

Fig. 1. Structure of the $p^+ - n$ junction multilayer GaAs/GaAs and GaAs/Si diodes.

3. RESULTS AND DISCUSSION

(a) DLTS analysis

Figure 2 shows DLTS spectra for two GaAs/Si (broken lines) and a typical DLTS spectrum for a GaAs/GaAs sample (solid line). All the GaAs/GaAs devices gave quite similar DLTS output but variation was seen from GaAs/Si samples. The high background doping concentration limited the detectable trap density to the order of $2 \times 10^{13} \text{ cm}^{-3}$ (0.01% of the doping concentration).

According to the theory of D.V. Lang[8], the deep levels in the n -GaAs base region, doped to $2 \times 10^{17} \text{ cm}^{-3}$, of the p^+n junction, is primarily probed by DLTS. The nature of the deep levels may be different between GaAs/GaAs and GaAs/Si samples owing to the misfit defects in GaAs/Si epilayers. Figure 2 indeed indicates this case. For GaAs/GaAs samples, only one deep level was observed with high rate windows (1000/s and 400/s). The activation energy and the trap density were deduced to be 0.71 eV and $1.0\text{--}2.0 \times 10^{14} \text{ cm}^{-3}$, respectively. This level is a mid-gap electron trap and could be attributed to the EL2 family[9,10]. EL2

Fig. 2. DLTS spectra for GaAs/GaAs and GaAs/Si samples. More defects are shown for GaAs/Si.

Fig. 3. Typical J - V - T for GaAs/GaAs samples.

is most probably described as an arsenic anti-site-arsenic interstitial ($\text{As}_{\text{Ga}}\text{-As}_i$ pair)[11], an intrinsic defect seen in many GaAs materials. The fact that no other trap levels were noticeable is consistent with the dislocation density of $\sim 10^4 \text{ cm}^{-2}$ in the epilayers due to the substrates.

For GaAs/Si samples, the EL2 level was still observable indicating that this level is an inherent defect related to the MOCVD-grown GaAs epilayers. On the other hand, an almost continuous distribution of trap levels appeared and the distribution varied with different samples. It is not easy to analyze these traps since they cross a large temperature range and hence several levels must exist in which the peaks are overlapped. A best estimation for a peak found in sample Si-O2 gave 0.42 eV as the activation energy which is close to the result in Ref.[12]. Misfit dislocations which have propagated from the heterointerface or some other Si-related defects are thought to be responsible for these traps.

Companion samples were also tested by double crystal X-ray rocking curve by C.R. Wie's group[13]. Their data indicated a dislocation density of $5.3 \times 10^7 \text{ cm}^{-2}$ and FWHM of 0.05°. These data are consistent with the electrical data reported herein and account for differences seen between GaAs/GaAs and GaAs/Si.

(b) I - V - T measurements

I - V - T data, shown in Fig. 3 for GaAs/GaAs and Fig. 4 for GaAs/Si indicate the current mechanisms of the two structures to be quite different. The GaAs/GaAs diode should follow the conventional p - n junction theory while the characteristics of GaAs/Si suggest a multistep tunneling-recombination mechanism. I - V - T data revealed the saturation current density of GaAs/Si to be about four orders in amplitude higher than for GaAs/GaAs diodes. This can be easily understood since the GaAs/Si structure contains many more defects. Also, the saturation current density of GaAs/Si is less temperature dependent

Silicon-substrate diode

Fig. 4. Typical J - V - T for GaAs/Si samples. A different mechanism is seen when compared to Fig. 3.

compared to that of GaAs/GaAs. $\ln(J_0)$ vs $1000/T$ plots derived from the I - V - T measurements are shown in Figs 5 and 6 for GaAs/GaAs and GaAs/Si,

respectively. The results agree with the DLTS measurement in that, at high temperature, the activation energy given by the slope was about 0.71 eV

Fig. 5. Activation energy data for four different GaAs/GaAs samples where J_0 is reverse saturation current density from J - V - T data.

Fig. 6. Activation energy data for three different GaAs/Si samples where J_0 is reverse saturation current density from J - V - T data.

for most of the samples of both types. At lower temperature, the curves of GaAs/Si samples are much flatter than for GaAs/GaAs samples and the turning points are at a rather high temperature, indicating the current mechanism to be more trap-related.

(c) Multistep tunneling model

Forward current mechanisms for $p-n$ diodes include the ideal diffusion current and excess current components such as SRH recombination, perimeter effect and multistep recombination-tunneling processes. Tunneling has been observed in heavily doped junctions, such as Esaki diodes, and heterojunction diodes where interface states are high and act to facilitate this excess current mechanism.

DLTS data indicated GaAs/Si structures to contain more defect levels and $I-V-T$ data revealed the slope of $\ln J_0-V$ curves of GaAs/Si to be rather independent of temperature[14]. Motivated by the DLTS and $I-V-T$ measurements, the multistep recombination-tunneling model was employed to describe the current mechanism of the GaAs/Si structure. The tunneling current is given by[15,16]

$$I = BN_T \exp[-A(\phi_i - V_a)] \quad (1)$$

where B is a temperature independent constant, N_T is the trap density in the space charge region, ϕ_i is the built-in potential and V_a is the applied voltage. In the case of multistep tunneling, the factor A can be written as

$$A = \frac{4\sqrt{m^* \epsilon_s} \theta}{3h\sqrt{N}} \quad (2)$$

where N is the doping concentration of the lightly doped side, and θ is the average fractional change in carrier energy for each step in the tunneling process[17]. Therefore, the number of steps in the recombination-tunneling process is

$$R = 1/\theta \quad (3)$$

The factor A can be found from the slope of the $\ln J_0-V$ curves. The measured $I-V$ data exhibit the factor A ranging from 11 to 14 among different GaAs/Si samples. Inserting this and the effective mass $m^* = 0.068$ in eqn (2), yields a value about 0.03 for θ , the average barrier experienced by each tunneling step. Thus, the number of steps (R) is about 30.

Equation (1) can be expressed in terms of its saturation current

$$I = I_0 \exp(AV_a) \quad (4)$$

where the saturation current is

$$I_0 = BN_T \exp(-A\phi_i). \quad (5)$$

Therefore, the small temperature dependence of J_0 for GaAs/Si might be understood from this expression. Under the fully ionized condition, the temperature effect on the current characteristics results mostly from the ϕ_i term. The temperature dependence of ϕ_i can be analyzed from the $C-V-T$ measurements which is discussed in the following section.

Fig. 7. Typical $C-V-T$ data for a GaAs/GaAs sample.

(d) $C-V-T$ measurements and correlation

Figures 7 and 8 show $C-V-T$ curves for GaAs/GaAs and GaAs/Si samples. It can be seen that the temperature dependence of the barrier height, ϕ_b , is also different between the two structures in that: first, at low temperature, a sudden change exists for GaAs/GaAs but the spacing keeps uniform or linear for GaAs/Si; secondly, ϕ_b of GaAs/Si is less temperature sensitive than for GaAs/GaAs. The measured data exhibited an almost constant value of about -0.001 eV/K for GaAs/Si, while the temperature dependence of GaAs/GaAs was not linear. The data of GaAs/Si could be explained by the multistep tunneling model. Taking the derivative with respect to temperature of eqn (1) yields

$$\partial \ln I / \partial T = -A \partial \phi_i / \partial T \quad (6)$$

Fig. 8. Typical $C-V-T$ data for a GaAs/Si sample. A lesser temperature dependence is seen compared to Fig. 7.

Fig. 9. Typical C - T data for GaAs/GaAs and GaAs/Si samples for a reverse bias = -2 V.

where the factor A is from 11 to 14 as seen above. A typical value of $\partial \ln I / \partial T = 0.01$ A/K is deduced from the I - V - T characteristics. Using these values in eqn (6), $\partial \phi_i / \partial T$ is solved to be -0.0007 to -0.0009 eV/K, close to the result of -0.001 eV/K observed from C - V - T data.

(e) C - T and photoreflectance tests

Figure 9 gives the C - T curves, indicating that the capacitance for both GaAs/GaAs and GaAs/Si exhibits similar temperature dependence for temperatures above 150 K. As temperature decreased from 150 K, the dependence remained the same for GaAs/Si but dropped suddenly for GaAs/GaAs. This is consistent in that the GaAs/Si substrate contains more defects causing a defect-induced band-tail which reduces the effective bandgap and causes carrier "freeze-out" at a lower temperature. Photoreflectance spectroscopy measurements, shown in Figs 10 and 11 for GaAs/GaAs and GaAs/Si respectively, seem to support this explanation because the measured bandgap was 1.4 eV for GaAs/GaAs and about 1.3 eV for GaAs/Si [7, 18]. The reduced bandgap of the GaAs layer on Si substrate is probably caused by strain effects of $\sim 3.65\%$ [13] and interfacial lattice mismatch.

Fig. 10. Photoreflectance spectrum for a typical GaAs/GaAs sample.

Fig. 11. Photoreflectance spectrum for a typical GaAs/Si sample.

4. CONCLUSION

In summary, DLTS I - V - T , C - V - T and photoreflectance measurements have been conducted to study the influence of heteroepitaxy on electrical properties of GaAs/GaAs and GaAs/Si structures. It was found that the GaAs homoepitaxial layer contains only one midgap trap level, but the GaAs/Si heterostructure has many dislocations which cause a continuous distribution of deep levels throughout the bandgap. The I - V - T characteristics for GaAs/Si structures agree favorably with the multistep recombination-tunneling model. In order for this excess current mechanism to dominate the current behavior, trap levels must exist at many levels in the bandgap. Therefore, DLTS and I - V - T results appear to be consistent. The slopes of GaAs/Si I - V - T characteristics are insensitive to temperature and the saturation current is slightly dependent upon temperature. These characteristics are consistent with the multistep tunneling mechanism.

C - T measurements suggest that carrier freeze-out occurs at lower temperatures for GaAs/Si than for GaAs/GaAs. Shallow traps are believed to be responsible for this observation. In addition, the bandgap reduction noted in photoreflectance spectra of GaAs/Si could be caused by effects of strain and interfacial lattice mismatch.

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Biaxial and uniaxial stress in gallium arsenide on silicon: A linear polarized photoluminescence study

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We have observed anisotropic behavior of the polarization of low-temperature photoluminescence from thick gallium arsenide grown on silicon substrates. The identification of the observed transitions was obtained from analysis of the selection rules, the temperature dependence of the feature intensities, and the transition energies. We find that the low-temperature doublet peaks are due to the emissions from two regions of material experiencing two different kinds of stress, one being biaxial and the other uniaxial. The anisotropy is due to the preferential direction created by parallel microcracks.

Gallium arsenide (GaAs) layers grown directly on silicon (Si) substrates have been of much interest recently.¹⁻¹⁸ It is believed that GaAs/Si is under biaxial tensile stress arising during postgrowth cooling from their difference in thermal expansions. The strain energy increases with epilayer thickness, with microcracks developing beyond a certain thickness. Deppe *et al.*¹⁸ have shown that the microcracks are not particularly deleterious on the devices fabricated on such layers, and may actually offer some benefit by providing strain relief. Low-temperature photoluminescence¹⁻¹⁷ (PL) has been widely used to study GaAs/Si. The band-edge emission is at lower energies than that from bulk GaAs, and is a doublet. Zemon *et al.*^{1,2} have argued that the double features are due to the strain split valence $j = 3/2$, $m_j = 3/2$, and $1/2$ bands. This has been confirmed by the study^{1,2} of the temperature dependence of these two features. However, the repeated observation^{1,3-5} of the high-energy PL feature below 20 K is anomalous, where mainly the low-energy feature is thermally populated. While some recent photoluminescence excitation (PLE) measurements^{1,6,7} have indicated that the two features are associated with the $m_j = 3/2$ - and $1/2$ -valence-band components coming from the same region of the sample experiencing the same levels of stress, other measurements^{8,9} suggested that these doublet peaks observed at low temperatures are not transitions to different valence-band components, but are both associated with the lower energy state, arising due to different regions of the sample experiencing different levels of stress. Lum⁵ *et al.* further suggested that the origin of two different stress regions may be associated with the presence of microcracks. We report here a linear-polarized-photoluminescence study of thick GaAs/Si samples, providing a more definitive identification of the origin of these PL features.

Circular polarized photoluminescence has proved^{8,9,19,20} to be very useful in distinguishing between the $m_j = 1/2$ and $3/2$ exciton when the preferential direction is perpendicular to the sample surface. Linear polarized photoluminescence is useful when the preferential direction is along the x - y plane. A linear polarized study²¹ has been done

previously on patterned GaAs grown on Si where the uniaxial stress due to patterning is along the $\langle 100 \rangle$ directions. This study is however different from ours where the uniaxial stress arises from the microcracks developing naturally along the $\langle 110 \rangle$ directions.

All three samples used in this study were grown by atmospheric-pressure metalorganic chemical vapor deposition (MOCVD) accomplished by the now-popular three-step method outlined here: the Si substrates [oriented 2° off $\langle 100 \rangle$ in the $\langle 110 \rangle$ direction] are heated in hydrogen to over 1000°C to remove the oxide, and then the temperature is lowered to approximately 400°C for nucleation and deposition of $200\text{ \AA}$ of GaAs; finally, a thick GaAs layer is deposited at typical MOCVD conditions using a 700°C growth temperature, a $4\text{ }\mu\text{m/h}$ growth rate, and a V-III ratio of 15:1. The epitaxial thickness of all three samples are $4\text{ }\mu\text{m}$.

Scanning electron microscopy on cleaved sections reveals microcracks in the GaAs layer (Fig. 1). These cracks

FIG. 1. SEM photographs of $4\text{ }\mu\text{m}$ layer of GaAs on Si showing microcracks or cleavages in GaAs. The Si has fractured at the point of the cleavages in the GaAs due to stress introduced in the Si substrate at those points.

^{a)} Also at Geo-Centers, Inc. N. J. Operations, Lake Hopatcong, NJ 07849.

are parallel and in the $\langle 110 \rangle$ direction. Since the cracks extend perpendicularly from the surface to the GaAs/Si interface, they can be considered to be $\langle 110 \rangle$ cleavage planes. The silicon at the GaAs/Si interface has also been stressed as seen in Fig. 1. The stress caused the Si to fracture at the same point where the stress was relieved in the GaAs layer.

Shown in Fig. 2 are the linear-polarized-photoluminescence spectra from sample 2 at various temperatures. The dotted lines are the spectra taken with the emission polarized parallel to the cracks, while the solid lines are those polarized perpendicular to the cracks. It is found that rotating either the analyzer or the sample by 90° has the same effect, convincingly proving that the anisotropy came from the sample.

Three features dominate the PL spectra when the emission polarization is parallel to the cracks (dotted lines in Fig. 2). We label these C , $E_{1/2}^{001}$, and $E_{3/2}^{001}$ in order of increasing energy. The $E_{1/2}^{001}$ and $E_{3/2}^{001}$ features are due to excitons⁶⁻⁹ associated with $J = 3/2^-$, $m_j = 1/2^-$, and $m_j = 3/2^-$ valence-band components of GaAs under a biaxial tensile stress. Since the linewidth at 5 K is about 6 meV we do not distinguish whether they are intrinsic excitons²³ or those bound to defects. Peak C is shifted from $E_{1/2}^{001}$ by about 20 meV, reasonable for the carbon feature in GaAs/Si, the acceptors having a reduced binding energy² due to strain. The variation of the intensity of peak C with excitation power and its disappearance at high temperature (> 40 K) confirm its extrinsic nature. The solid line in Fig. 3 is the temperature dependence of the intensity ratio of the emissions $E_{1/2}^{001}$ and $E_{3/2}^{001}$ exhibiting thermalization. An Arrhenius fit gives the activation energy of $E_{3/2}^{001}$ from $E_{1/2}^{001}$ to be 13 meV, agreeing with the measured 14 meV. The oscillator strength ratio of the two features is about 3.6, agreeing reasonably with the theoretical value of 3.3.^{22,23}

The spectra shown by the dotted lines in Fig. 2 is similar

FIG. 2. Variation of the linear-polarized-photoluminescence spectra of GaAs/Si epilayer with temperatures in the range of 5–115 K. Solid lines: emission polarized perpendicular to the cracks. Dotted lines: emission polarized parallel to the cracks. Dashed lines: difference between the solid lines and the dotted lines. $E_{3/2}^{001}$, $E_{1/2}^{001}$, and $E_{1/2}^{110}$ are denoted as $E_{3/2}$, $E_{1/2}$, and E' in the figure.

FIG. 3. Temperature dependence of PL intensity ratios of $E_{3/2}^{001}/E_{1/2}^{001}$ (solid line) and $E_{1/2}^{110}/E_{1/2}^{001}$ (dotted line). $E_{3/2}^{001}$, $E_{1/2}^{001}$, and $E_{1/2}^{110}$ are denoted as $E_{3/2}$, $E_{1/2}$, and E' in Fig. 2.

to that from thin crack-free GaAs layers,^{4,5} under uniform biaxial tensile stress. In thick samples, low-temperature photoluminescence often contains a high energy peak^{11,12} above the $E_{1/2}$ feature. High energy shoulders (or peaks) at low-temperature PL were found in the perpendicular polarization (solid line in Fig. 2). Below 35 K, there are two features, C' and E' . With increasing temperature E' broadens and merges with the $E_{3/2}^{001}$ exciton emission. However, E' does not disappear completely but can be observed from 5 to 150 K. To obtain its energy and emission intensity, we plotted by dashed lines the difference between the spectra given by the solid and dotted lines in Fig. 2. The dashed line at low temperature has two Gaussian features, C' and E' , while at higher temperatures only E' is observed. The intensity ratio of E' to $E_{1/2}^{001}$ (dotted line, Fig. 3) is a constant over a wide range of temperatures. This indicates $E_{1/2}^{001}$ and E' are emissions from physically separated regions, confirming the PLE result by Wilson *et al.*^{8,9}

The anisotropic behavior of E' excludes itself from any transition originating from a symmetric biaxially stressed region and strongly suggests a preferential direction in the x - y plane. In all three samples, the E' emission is only observed with polarization direction perpendicular to the microcracks, implying that the anisotropy is related to the microcracks. The parallel cracks relieve the strain perpendicular to them, leaving some regions with a uniaxial stress parallel to these cracks, whereas in others the biaxial stress is not relieved. Microprobe cathodoluminescence²⁴ has shown a variation of stress in different regions in patterned GaAs grown on Si. However, in our as-grown samples which develop microcracks naturally, while there may be regions of variation, there are two main regions of biaxial and uniaxial stress. This can be seen from the clear peaks and intact polarization information.

For a biaxial tensile stress in the x - y plane the preferential direction for m_j is along $\langle 001 \rangle$. The lowest intrinsic emission is the $m_j = 1/2$ exciton, and the luminescence normal to the x - y plane is isotropic. Thus emission in both linear polarizations (solid and dotted lines in Fig. 2) have the same

intensity. In the $\langle 110 \rangle$ uniaxial stress case, the preferential direction is $\langle 110 \rangle$. The coupling between $m_j = 1/2$ states to $m_j = 3/2$ states is negligible²⁵ and emission is due to the $m_j = 3/2$ exciton, polarized linearly along the perpendicular direction. We assign the $m_j = 3/2$ exciton from the uniaxial stressed region to E' as low-temperature PL probes the lowest energy transition. Luminescence polarized in the perpendicular direction (solid lines) has two components, from regions under uniaxial, and those under biaxial stress, while the emission with the parallel polarization is from the biaxially stressed region. Therefore the difference (dashed lines) between the solid and the dotted lines represents the net contribution from uniaxial stress.

We have calculated the energy of $E_{1/2}^{001}$ and $E_{3/2}^{001}$ in the biaxial-strained region and that of E' (or $E_{3/2}^{110}$ in consistent notation) in the uniaxial-strained region by assuming 0.26% expansion¹¹ of GaAs in the x - y direction (biaxial case) and 0.26% expansion in the $\langle 110 \rangle$ direction (uniaxial case). We find the shifts of $E_{1/2}^{001}$, $E_{3/2}^{001}$, and $E_{3/2}^{110}$ from unstrained GaAs bulk exciton are 31, 14, and 19 meV, respectively.²⁶ Comparing the experimental values of 28.3, 13.8, and 20.3 meV, the agreement is very good for such a simple model.

The corresponding $m_j = 1/2$ exciton ($E_{1/2}^{110}$) is not observed in PL. This may be due to it having an energy very close to the stronger $E_{3/2}^{001}$ one. However, $E_{1/2}^{110}$ is clearly observed in a modulated reflectance study,²⁷ and confirms our assignment.

In conclusion, we have observed anisotropic behavior of PL spectra from thick GaAs/Si samples with microcracks in the $\langle 110 \rangle$ direction. The low-temperature doublet PL peaks are due to emission from two regions of material experiencing two different kinds of stress, biaxial and uniaxial. The anisotropy is due to the preferential direction created by parallel cracks.

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A model for ac conduction in amorphous silicon nitrides

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The frequency-dependent conductivity of amorphous silicon nitride ($a\text{-Si}_{1-x}\text{N}_x$) films has been reported for the first time. The origin of the ac loss is discussed in terms of nitrogen-related two-level systems and electron transfer between Si dangling bond states.

There has been continued interest in the application of silicon nitride in electronic devices,¹⁻³ and a number of works concentrate on their structural and optical properties.^{4,5} Although their electronic properties depend on the

behavior of their gap states, electronic transport data are very few and hence our understanding of them is still incomplete.

Robertson and Powell⁶ have suggested for hydrogenat-

Photoreflectance study of gallium arsenide grown on Si

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Low-temperature linear polarized photoreflectance is used to study the stress and its release in thick GaAs grown on Si. We find that the GaAs layer is mainly composed of two regions with two kinds of stress, biaxial and uniaxial. Four features, two from each region due to the split valence band, are observed. Their polarization selection rules enable us to distinguish the nature of the strain as well as the nature of the transitions.

Modulation spectroscopy has been shown¹⁻¹⁸ to be very useful in studying the optical properties of semiconductors and to extract their electronic structure. The optical response of the solid is modified in some manner by the periodic variation of the measurement conditions. This modulation gives rise to sharp derivative spectra¹⁻³ for the higher transitions as well as the lowest transition and hence this technique is a very useful method for characterization of bulk and layered semiconductor structures such as multiple quantum wells and superlattices. This modulation technique is especially powerful for the investigation of strain in semiconductor material.^{19,20} In this letter, we report a low-temperature, polarized photoreflectance study on GaAs/Si, a material of great technological interest.²¹⁻⁴⁴ It is believed that GaAs/Si is under biaxial tensile stress which arises during cooling after growth due to the difference in thermal expansion characteristics of GaAs and Si which will alter the band structure, leading to a change in the optical spectra. Various optical techniques, including low-temperature photoluminescence (PL),^{21-38,44} photoluminescence excitation (PLE),²¹⁻²⁵ cathodoluminescence (CL),^{39,40} reflectance,²⁵ wavelength modulated reflectance,²⁵ room-temperature photoreflectance (PR),⁴¹ and Raman scattering,⁴² have been used to study the effect of strain in GaAs grown on Si. The splitting of the $j = 3/2$ valence band and the associated exciton (or band-to-band) transitions $E_{3/2}^{001}$ and $E_{1/2}^{001}$ were used to determine the biaxial stress in the x - y plane, which ranges from about 1.5 kbar at room temperature to about 2.5 kbar at 4.2 K. Here $E_{3/2(1/2)}^{lmn}$ denotes the transition from $m_j = \pm 3/2$ ($\pm 1/2$) state to conduction band with the preferential direction for m_j along $\langle l, m, n \rangle$. While some measurements^{21,30} have indicated that the two features observed in low-temperature PL are associated with the $m_j = \pm 3/2$ and $\pm 1/2$ valence-band components coming from the same region of the sample experiencing the same levels of stress, other measurements^{23,24,44} suggested that these doublet peaks observed at low temperatures are not transitions to different valence-band components, but are both associated with the lower energy state, arising due to two different regions of the sample experiencing two different kinds of stress. If the latter interpretation is true, the

observation of four features, two from each region due to the split valence band, is a crucial test. Four features have been observed in PLE²³ and room temperature PR.⁴¹ However neither of these studies included analysis of the polarization and the assignments are not unique. Hence their identification and their nature are not completely clear. In this low-temperature polarized photoreflectance study all four features from $j = 3/2$ valence band to conduction band have been observed, and their polarization selection rules enable us to distinguish the nature of strains as well as the nature of transitions.

Three samples are used in this study. All of them are grown by atmospheric pressure metalorganic chemical vapor deposition accomplished by a three-step method. The Si substrates are oriented 2° off (100) towards the $\langle 110 \rangle$ direction. The epitaxial GaAs layer in all three samples is $4 \mu\text{m}$ thick. Scanning electron microscopy (SEM) of the cleaved sections reveals microcracks⁴⁴ in the GaAs layer. These cracks are parallel and in the $\langle 110 \rangle$ direction. The distances between two neighboring cracks vary from about 10 to $100 \mu\text{m}$. The closely spaced parallel cracks relieve the strain perpendicular to them and leave some regions under uniaxial stress parallel to the cracks along $\langle 110 \rangle$.

The PR apparatus has been described in the literature.¹² The samples are mounted in a closed-cycle helium refrigerator. The probe beam is from a lamp filtered by a one-quarter-meter monochromator and is linearly polarized, while the He-Ne laser pump beam is unpolarized. Both probe and pump beam strike the sample at near normal reflection alignment with an angle of less than 15° . The PR signal ($\Delta R/R$) is recorded by a lock-in amplifier and normalized by division.

Room-temperature PR spectra from these samples reveal Franz-Keldysh oscillations,^{4,5,41} the result of built-in electric field¹⁸ at the surface and/or at the GaAs/Si interface.⁴¹ No significant excitonic feature is observed. Lowering the temperature reduces the built-in field due to the trapping of photon-generated carriers. This phenomenon has been observed in bulk GaAs and in GaAs grown on Si.⁴⁵⁻⁴⁷ At 77 K, the Franz-Keldysh oscillations from our samples disappear and the splitting of the heavy and light hole exciton features starts to appear. However, only at about 10 K, the features really sharpen up and all four features are well resolved. Therefore, only the results at 10 K will be discussed.

Shown by dotted lines in Figs. 1 (a) and 1(b) are the

^{a)}Geo-Centers, Inc. N. J. Operations, Lake Hopatcong, NJ 07849. Work performed at US Army ETDL, Ft. Monmouth.

PL,⁴⁴ low temperature PLE,²³ but in disagreement with room-temperature PR results in Ref. 41.

Stress variation and relief has been studied in patterned samples by CL.^{39,40} Uniaxial tensile stress along the $\langle 100 \rangle$ directions in patterned stripes was observed by PL.³⁸ In our samples, the microcracks developed naturally, and the uniaxial stress is a result of the parallel cracks along the $\langle 110 \rangle$ direction, which relieve the strain perpendicular to them. No microprobe was used either in these experiments or in the PL experiments.⁴⁴ However, while there may be small variations near the cracks, that there are two main regions of stress is clear since all four features are observed, the peaks in the spectra are not smeared out and the polarization information is intact.

In conclusion, we have used low-temperature linear polarized photorefectance to study GaAs grown on Si. We find that the GaAs layer is composed of mainly two regions with two kinds of stress, one being biaxial and the other uniaxial. Both the transition energies and the intensities of the PR features agree very well with the theoretical calculation.

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ADVANCES IN HIGH-EFFICIENCY GaAs SOLAR CELLS

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ABSTRACT

This paper describes the development of GaAs solar cells having a one-sun, AM1.5 efficiency of 24.8% (measured at SERI) and a concentrator AM1.5 efficiency of 28.7% at 200 suns (measured at Sandia). Corresponding AM0 efficiencies are 21.7 and 24.5%. These are among the highest independently-verified efficiencies for single-junction cells without cover glasses. Reasons for recent efficiency improvements are discussed. One-sun efficiencies over 26% in the near term are projected, showing that GaAs cells have not yet reached their practical efficiency limits.

INTRODUCTION

The first high-efficiency GaAs cells were developed by Woodall and Hovel using the AlGaAs/GaAs heteroface structure grown by LPE [1]. Their one-sun efficiency record of 22% stood for many years. The development of the MOCVD growth technique and a better understanding of losses has led to steady improvements in efficiency over the past several years by many laboratories. The state of the art in 1989 was reviewed in [2]. Recent progress, in our laboratory and elsewhere, has now led to the demonstration of single-junction GaAs solar cells having efficiency values of approximately 25% at one-sun illumination and 29% under concentration. While multijunction tandem cells have demonstrated higher laboratory efficiency values, their complexity makes them a less practical alternative for near-term manufacturability compared with the simpler, single-junction structures described here.

EXPERIMENTAL

The structure of our high-efficiency GaAs solar cell is shown in Figure 1. The same p-on-n double heteroface structure is used for both one-sun and concentrator cells. The epitaxial layers are deposited at atmospheric pressure in a SPI-MO CVDTM 450 system by the metalorganic chemical vapor deposition (MOCVD) technique. Details of the MOCVD epitaxial growth and solar cell processing have been reported previously [3,4].

RESULTS

Figure 2 shows the AM1.5G I-V curve of our best 0.25 cm² one-sun cell and its efficiency parameters under AM1.5G and AM0 spectra (SERI measurements courtesy of Mr. Keith Emery). The efficiencies of 24.8

Cr/Au	
p ⁺ GaAs	AR Coating
p Al _{0.3} Ga _{0.7} As	0.03 μm
p GaAs 4x10 ¹⁸ cm ⁻³	0.50 μm
n GaAs 2x10 ¹⁷ cm ⁻³	3-4 μm
n ⁺ Al _{0.3} Ga _{0.7} As 1x10 ¹⁹ cm ⁻³	1.0 μm
n ⁺ GaAs 1x10 ¹⁸ cm ⁻³	1.0 μm
	Buffer Layer
n ⁺	GaAs Substrate
	Au:Ga/Au Back Contact

Figure 1. Solar cell structure.

Spire, GaAs, global

Sample: 1552-3-5 Temperature = 25.0°C
Mar. 6, 1989 1:14 pm Area = 0.250 cm²

Figure 2. One-sun I-V curve of 24.8% efficient cell.

and 21.7% under these test conditions are among the best reported. The uniformity across the wafer was very good, with an AM1.5 wafer average of 24.4% and a standard deviation of 0.9% for all 40 cells. Additional information on yield and uniformity was reported [3]. The run-to-run reproducibility was also excellent. All wafers processed recently in four fabrication batches from four separate MOCVD runs yielded full-wafer efficiency averages over 24% at AM1.5.

Figure 3 shows the AM1.5 and AM0 efficiency as a function of concentration ratio for our best GaAs point-focus concentrator cell (Sandia measurements courtesy of Dr. Doug Ruby). The cells had a 4 mm diameter circular active area and a 5 mm square junction area. The peak AM1.5 efficiency of 28.7% at 199 suns is the highest reported value for a single-junction cell without a cover glass. Details of the cell design, fabrication, and testing can be found in [4].

Spectrum	AM0	AM1.5 D
Suns	170	199
V_{oc}	1.139	1.139
$1 \times J_{sc}$	33.61	28.75
FF	87.5	87.5
Eff.	24.5	28.7

Figure 3. Efficiency versus concentration for GaAs concentrator cell.

Factors Contributing to Improved Efficiency

Reasons for improved performance relative to earlier GaAs cells fabricated in our laboratory [3,6] can be divided into MOCVD epitaxial growth and cell processing improvements. The most significant growth change has been an increase in growth temperature from 700–740°C to 775–800°C. This significantly reduces recombination in the Si-doped base layer of the cell, both in the bulk and at the GaAs/ $Al_{0.3}Ga_{0.7}As$ heteroface. In Figure 4 we compare the internal quantum

Figure 4. Internal quantum efficiency for cells grown at different temperatures.

efficiency of cells grown at 740 and 800°C. The long-wavelength response is substantially enhanced at the higher growth temperature due to reduced recombination in the base. (Changes in the short wavelength response were caused by differences in the thickness of the $Al_{0.8}Ga_{0.2}As$ window layer, unrelated to the growth temperature.) The open-circuit voltage, which had previously been limited by recombination in the base, was also improved from 1.029 to 1.040 V. The bulk diffusion saturation current was reduced by 38% at the higher growth temperature for the cells compared in Figure 4. Another growth-temperature comparison was reported in [3] for cells grown at 740 and 775°C; again the higher growth temperature demonstrated improvements in red response and open-circuit voltage. Evidence was also found by DLTS of reduced deep level concentrations at the higher growth temperature [3]. The improvement in Si-doped GaAs at higher growth temperatures was also confirmed in photoluminescence (PL) decay measurements [7]. Table 1 summarizes PL decay lifetimes and heteroface recombination velocities as a function of growth temperature from this work.

Table 1. Photoluminescence decay lifetime and heteroface recombination velocity as functions of MOCVD growth temperature for Si-doped ($N = 1 \times 10^{17} \text{ cm}^{-3}$) GaAs with $Al_{0.3}Ga_{0.7}As$ confining layers.

Growth Temperature (°C)	PL Decay Lifetime (ns)	Interface Recomb. Velocity (cm/s)
700	15.4	3×10^4
740	129.8	2×10^3
775	180.1	5×10^2
800	193.7	5×10^2

It is significant to note that the "theoretical limit" radiative recombination lifetime for this doping level is 50 ns. The higher values of PL decay lifetime in Table 1 are explained by photon recycling, wherein photons generated by radiative recombination are re-absorbed in the material, again creating hole-electron pairs [7]. This phenomenon only occurs when non-radiative recombination mechanisms are insignificant. In summary, all of the data point to reduced base recombination for higher growth temperatures.

One result of higher base diffusion lengths is the ability to increase the base thickness to collect more weakly-absorbed photons, without increasing the base diffusion saturation current. We have consequently increased the base thickness from 3 to 4 microns in our high-efficiency cells. The major difference between our best cell and previous high-efficiency cells has therefore been higher short-circuit current at the red end of the spectrum from reduced base recombination and increased base thickness.

The major improvement in concentrator cell efficiency has come from reduction of extrinsic losses. Shadow losses have been reduced with tall, narrow grid lines defined by an image-reversal liftoff process. Grid lines for the cells in Figure 3 were roughly 3 microns high and 3 microns wide with sloping side walls that reflect some of the light back onto the cell. The shadow loss is only 3 percent for these cells. A smaller cell size relative to earlier cells [6] also improved the efficiency by reducing resistive losses. Grid pattern optimization [8] also contributed to minimizing losses in these cells.

Other improvements in the growth process which have been described earlier include a continuous, as opposed to interrupted, growth process to reduce recombination at the heteroface, higher emitter doping levels to reduce series resistance, and the use of thin, optimum thickness $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$ window layers to minimize reflectance and maximize blue response. Control of thickness and composition of these thin (30 nm) layers has been greatly improved through a new optical monitoring technique based on reflectance [9].

Design and processing improvements described previously include an optimum double-layer antireflection coating of thermally-evaporated ZnS and MgF_2 , together with an optimum thickness AlGaAs window.

Loss Analysis of One-Sun Cell

Following procedures described previously [5,6], we have analyzed losses in the 24.8% efficient cell of Figure 2. We will not discuss the open-circuit voltage and fill factor, which are similar to earlier cells, but concentrate on the short-circuit current. As noted previously, this is the area needing the most improvement to reach theoretical limits. Figure 5 displays a convenient way of viewing the losses in short-circuit current. It compares the measured external quantum efficiency spectrum with an ideal curve ($\text{QE} = 1$), reduced by various extrinsic losses. The amount of light reflected or absorbed by grid lines (Shadow) is first subtracted. Then comes the light reflected from the cell surface between grid lines. Additional losses are absorption in

Figure 5. Quantum efficiency losses for 24.8% efficient cell.

the ZnS antireflection coating at the blue end, and lack of absorption at the red end due to the band gap absorption edge in GaAs. The difference between the resulting curve and the measured QE is from photons absorbed in the cell (including the window) but not collected. These intrinsic losses can be partitioned into window, emitter, and base losses by modeling the measured QE curve and comparing the results to the same structure with no recombination. The results of the analysis are summarized in Table 2. The extrinsic losses are dominated by shadow loss; over half of this is from the contact pads, which are proportionally larger on these small test cells than on larger cells. The extrinsic losses are entirely in the window and emitter layers; at the higher growth temperature there is no base recombination loss. Modeling indicates that the emitter loss could be substantially reduced by reducing the emitter thickness.

Table 2. Short-circuit current losses in a 24.8% efficient GaAs cell. The results are expressed as percentages of the theoretically available short-circuit current.

EXTRINSIC	
Shadow	4.9 %
Reflectance	1.4 %
AR Absorption	0.5 %
INTRINSIC	
Window	3.0 %
Emitter	1.8 %

Unresolved Issues

Although the understanding of loss mechanisms in GaAs cells has improved in recent years, there are two unresolved issues related to modeling the losses in these cells. One is illustrated by Figures 6 and 7, which

Figure 6. Quantum efficiency curve measured at Spire for 24.8% efficient cell. The best modeled fit is also shown.

Figure 7. Quantum efficiency curve measured at SERI for 24.8% efficient cell. The best modeled fit is also shown.

compare modeled to measured quantum efficiency curves for the 24.8% cell. Internal QE was derived from the measured external QE (which was scaled to match SERI's short-circuit current in both cases) by correcting for grid shadow, reflectance, and ZnS absorption, all of which have been measured. The analytical model used here is that of Hovel and Woodall [10]. Model parameters are shown in the figures. Layer thicknesses and dopings were experimentally measured; heteroface recombination velocities were measured by photoluminescence decay [12]. The only adjustable fitting parameters were therefore minority-carrier diffusion lengths in the window, emitter, and base of the cell. The problem is a measurement discrepancy between Spire and SERI data, primarily in the

380-580 nm range. Spire's data in Figure 6 were measured with a monochromator system from Optronics Laboratories. The absolute reference standard is an NIST-traceable silicon photodiode. Short-circuit current measurements at each wavelength were made under dc conditions with a low light level from the monochromator. A 3 mm spot at the center of the cell was illuminated. In contrast, the data in Figure 7 were measured by SERI using a filter wheel setup and a pyroelectric detector. Relative quantum efficiency was measured, then scaled to match the one-sun short-circuit current measured in SERI's solar simulator. For the spectral response measurement, short-circuit current at each wavelength was measured in ac mode using a chopper and a one-sun dc light bias. The full cell area was illuminated.

It can be seen from Figure 6 that there are two problems with Spire's measurements. First, the data cannot be fit by the model from 380 to 600 nm. Second, when the parameters derived by fitting the rest of the curve are used to calculate diffusion saturation current, the result is less than half the measured value of 8×10^{-20} A/cm². (The diffusion saturation current calculations include heavy doping effects and experimental values of minority-carrier mobility in the emitter [11].) SERI's data, on the other hand, can be fit over the whole spectrum by Hovel's model. The calculated diffusion saturation current of 7×10^{-20} A/cm² is also in close agreement with the measured value. SERI's data are therefore more consistent with our modeling of both short-circuit current and open-circuit voltage. Suspecting a problem with our absolute QE reference photodiode, we compared it directly to the NIST detector reference package and to several other calibrated silicon photodiodes from Optronics Laboratories in our laboratory; no discrepancies were found. To check for a light-intensity dependence of spectral response, SERI measured a cell with and without a one-sun light bias, but found no significant difference. We can therefore see no error in our measurement, as long as the NIST reference is accurate. If the Spire data are accurate, then modifications to the model are needed.

A second issue relates to modeling of the photon recycling process in solar cells. Photon recycling is a strong effect in double heterostructures used for PL decay measurements [7] and we have evidence that it is also operative in DH solar cells. For example, the fit to the quantum efficiency curve in Figure 7 gives a base diffusion length of 7.5 microns, corresponding to a minority-carrier lifetime of 87 ns. This is significantly higher than the radiative recombination lifetime of 33 ns calculated for a doping of 1.5×10^{17} cm⁻³. The discrepancy can be qualitatively explained by photon recycling. In the emitter, on the other hand, the fit value of 2.1 microns for diffusion length is in good agreement with the calculated radiative-lifetime limit of 2.2 microns. The difference between the emitter and base is expected because photon recycling is a strongly increasing function of layer thickness. A practical theoretical model of photon recycling in solar cell structures is therefore needed but not available at present. It should be noted that photon recycling can increase the limiting efficiency for GaAs cells by raising the upper limit of effective minority-carrier lifetimes.

PROJECTIONS FOR THE FUTURE

Based on earlier loss analyses, we have shown that present cells achieve only about 80% of their theoretical efficiency, and have projected one-sun AM1.5 efficiencies of 26.5% with near-term improvements [5]. This analysis is updated in Table 3 to reflect our most recent cell. We still believe that short-circuit current can be improved substantially by reducing extrinsic losses, particularly grid shadow (larger cell sizes), and by reduced emitter recombination. One promising approach in this direction is the use of GaInP₂ in place of AlGaAs for the window layer. Very low interface recombination velocities have been demonstrated with this approach [13], and one-sun efficiencies of 25.1% have been demonstrated [14].

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Table 3. Comparison of present and projected GaAs cells to theoretical limits. Conditions: One sun, AM1.5 Global, 25°C.

Parameter	Theoretical Limit	Present Cells		Projected Cells	
		Value	(% of Limit)	Value	(% of Limit)
V _{oc} (V)	1.095	1.029	(94.0)	1.050	(96.0)
J _{sc} (ma/cm ²)	31.55	27.89	(88.4)	29.0	(91.9)
FF (%)	89.1	86.43	(97.0)	87.0	(97.6)
Eff (%)	30.8	24.8	(80.5)	26.5	(86.0)

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EXPERIMENTAL STUDY OF SOLAR CELL PERFORMANCE VERSUS DISLOCATION DENSITY

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ABSTRACT

Lattice-mismatched semiconductor materials are an important part of many of today's advanced high-efficiency solar cell designs. This paper reports the results of an experimental study of solar cell performance and material properties as a function of dislocation density. Buffer layers of $\text{GaAs}_{1-y}\text{P}_y$ ($y = 0-0.32$) have been used to controllably introduce dislocations into GaAs-on-GaAs cells. Bulk space-charge recombination is found to be the dominant mechanism operating at high defect densities. Our experimental results indicate that a dislocation density $\leq 5 \times 10^5 \text{ cm}^{-2}$ is needed for the production of high-efficiency GaAs-on-Si solar cells. Our results to date have yielded concentrator cells with AM1.5 efficiencies of up to 20% at 210 suns in GaAs-on-Si layers containing 1×10^7 dislocations/ cm^2 , as compared with GaAs homoepitaxial cells that are 29% efficient under concentrated sunlight.

INTRODUCTION

In many of today's state-of-the-art solar cell designs, lattice-mismatched layers are common, as researchers attempt to utilize novel material combinations for high-efficiency tandem structures or single-junction cells on low-weight, low-cost, high-strength substrates. In many of these cases, a large number of crystalline defects, typically dislocations, are introduced by the lattice parameter mismatch. Much effort has been and is currently being expended on reducing the dislocation density in order to improve the solar cell performance. While some theoretical work on cell performance versus defect density has been published [1-4], very little experimental data in this area exists. Therefore, we have performed an experimental study of GaAs solar cell performance and material properties as a function of defect density over a wide range, namely 10^4 to 10^8 cm^{-2} . The methods and results of this study are described below.

EXPERIMENTAL

The basic approach utilized is to study GaAs-on-GaAs solar cells having a wide range of dislocation densities; a lattice-mismatched $\text{GaAs}_{1-y}\text{P}_y$ buffer layer (2 to 4 μm thick) is interposed between the GaAs substrate and the GaAs active layers in order to controllably introduce dislocations into the device. The

composition, y , of the GaAsP buffer is the major factor determining the defect density in the device layers, and y values of 0 to 0.32 have been used here to cover a defect density range of approximately 10^4 to 10^8 cm^{-2} . Data from GaAs-on-Si experiments are also included.

All semiconductor layers are deposited by metalorganic chemical vapor deposition (MOCVD) using a SPI-MO CVDTM 450 reactor. The GaAsP buffer layers are grown at low-pressure (76 torr) conditions for optimum uniformity, while the active device layers are grown at 760 torr. The reagents used include trimethylgallium, trimethylaluminum, arsine, and phosphine, with dilute silane and dimethylzinc being the dopant gases for n- and p-type layers, respectively.

Figure 1 shows the structure of the GaAs cells fabricated and tested; the detailed cell-layer specifications have been published previously [5]. In addition, minority-carrier lifetime has been measured by a photoluminescence (PL) decay method on double-heterostructure (DH) devices which utilize a 4- μm -thick GaAs layer sandwiched between two $\text{Ga}_{0.7}\text{Al}_{0.3}\text{As}$ layers, as described previously [6]. For the GaAs-on-Si samples, the two-step growth method [7] is utilized, with defect reduction achieved by incorporating strained-layer and thermal-cycle growth methods [8].

Figure 1. Test Structure used to Study GaAs Cell Performance vs. Dislocation Density.

The GaAs and GaAsP layers are characterized by a number of techniques including Nomarski microscopy, transmission electron microscopy (TEM), electron-beam-induced current (EBIC), PL, PL-decay, and solar cell device modelling.

RESULTS

Figure 2 shows Nomarski micrographs of several typical GaAs DH samples on $\text{GaAs}_{1-y}\text{P}_y$ buffer layers.

The surface roughness increases with increasing y values, and cross-hatch features (due to the lattice mismatch) are clearly visible for all samples where $y > 0.02$. The defect structure of GaAs-GaAsP samples has been studied by EBIC and TEM techniques, and typical micrographs are shown in Figures 3 and 4. The EBIC method works well for defect densities up to 10^6 cm^{-2} , while TEM is the best method for use in a defect range of $> 10^7 \text{ cm}^{-2}$. The results of defect density versus buffer composition are shown in Figure 5.

Figure 2. Nomarski Micrographs of GaAs DH Samples Grown on $\text{GaAs}_{1-y}\text{P}_y$ Buffer Layers on GaAs Substrates.

Figure 3. EBIC Micrographs of $\text{GaAs}_{1-y}\text{P}_y$ Buffer Layers.

Figure 4. Cross-sectional TEM Photographs of GaAs-GaAs_{1-y}P_y Structures.

Figure 5. Dislocation Density in the GaAs Device Layers, Measured by EBIC and Planview TEM, as a Function of Composition of the GaAs_{1-y}P_y Buffer Layer.

Figure 6 shows how the individual solar cell parameters vary with defect density; all cell testing was done at 1-sun, AM1.5 conditions. Table 1 relates buffer composition and cell performance; percentage of mismatch can be obtained by multiplying y by 3.575.

Figure 6. Efficiency Parameters as Functions of Dislocation Density for GaAs Cells Grown on GaAsP Buffer Layers (a) Open-circuit Voltage, (b) Short-circuit Current, (c) Fill Factor.

Table 1. Dislocation Densities and AM1.5 Efficiencies Measured at SERI for GaAs Cells with Different Composition GaAsP Buffer Layers. The last two dislocation densities were measured by TEM; the others by EBC.

Wafer	y in GaAs _{1-y} P _y	Dislocation Density (cm ⁻²)	Base L _h (μm)	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff (%)
1512-1	0.00	< 10 ⁴	4.32	1.028	27.1	86.3	24.1
1513-1	0.00	8 × 10 ³	4.16	1.033	27.0	84.3	23.5
1511-3	0.02	3 × 10 ⁴	3.86	1.032	26.7	85.4	23.7
1511-1	0.05	3.3 × 10 ⁵	3.45	1.015	26.6	84.0	22.7
1513-4	0.07	5 × 10 ⁵	3.49	1.014	26.7	83.2	22.6
1512-4	0.08	4 × 10 ⁵	3.24	1.009	26.9	82.5	22.4
1512-2	0.18	1.5 × 10 ⁷	1.64	0.844	25.3	78.1	16.7
1511-5	0.27	7.3 × 10 ⁷	1.16	0.787	24.6	76.9	14.9

While J_{sc} and FF decrease at roughly constant rates with mismatch, V_{oc} shows only minimal losses below 0.3% mismatch and a large drop between 0.3 and 0.6%. The log I-V curves in Figure 7 can be used to explain this behavior. The major effect of mismatch is to increase the n = 2 component of dark current. Because the fill factor is controlled by n = 2 current, it is sensitive to all levels of mismatch. The V_{oc}, however, is largely controlled by the n = 1 current for GaAs cells, and small amounts of mismatch appear to have little effect on the n = 1 current. The small decreases in V_{oc} below 0.4% mismatch are due to the increasing importance of the n = 2 current, but the n = 1 current is still significant. Above 0.6% mismatch, the n = 1 current is completely swamped by the n = 2 current, and so V_{oc} drops sharply. Figure 8 shows the dependence of the n = 1 and n = 2 saturation currents on lattice mismatch.

Figure 7. Log I-V Curves for GaAs Cells with Different Amounts of Buffer Lattice Mismatch.

Figure 8. Dependence of Diffusion Saturation Current (J_{o1}) and Space-charge-Recombination Saturation Current (J_{o2}) on Buffer Lattice Mismatch.

The log I-V results also give us information about bulk vs. surface space-charge recombination currents. We have previously determined that the n = 2 current for GaAs cells is dominated by surface space-charge recombination. It scales with the junction perimeter and changes with time as the unpassivated GaAs surface changes. In this lot we saw the value of J_{o2} increase by a factor of 2 over a period of 3 weeks for the GaAs control cells. However, the value of J_{o2} did not change for cells with more than 0.1% lattice mismatch.

The cells with more mismatch also had slightly lower n-values, closer to 1.85 than 2.0. Both the n-value and temporal invariance point to bulk space-charge recombination as the dominant mechanism in cells with significant mismatch. Presumably the dislocations caused by lattice mismatch are acting as recombination centers in the junction space-charge layer. To summarize, the major effect of lattice mismatch on V_{oc} and FF is from increased n = 2 current attributed to bulk space-charge recombination.

The cause of the short-circuit current decrease can be seen in the quantum efficiency curves of Figure 9. For large mismatch ($>0.5\%$), there is a noticeable decrease in the red response caused by lower base diffusion length. For small mismatch, the effects are more subtle. Reduced collection from both the emitter and base layers can be deduced from quantum efficiency modeling. Base diffusion lengths were included in Table 1.

Figure 9. Internal Quantum Efficiency Curves for GaAs Cells with Different Amounts of Buffer Lattice Mismatch.

To summarize the results, there appear to be two regions of lattice mismatch effects. For mismatch less than approximately 0.5%, there are small decreases in V_{oc} , FF, and J_{sc} attributed to crystal defects. Above 0.5% mismatch there is a large drop in V_{oc} caused by high $n=2$ currents. The short circuit current is also affected significantly by reduced minority carrier diffusion lengths. Coincident with these changes is a noticeable degradation in surface morphology of the layers.

The effects of intentional mismatch are very similar to results for GaAs-on-Si solar cells, as seen in Figure 10. Here we compare GaAs-on-Si results reported by Spire and the two groups at NTT [2,3,9] to the present experiment. Also shown is a theoretical curve from Dr. Yamaguchi's group at NTT, based on dislocation effects, which fits their data [2]. Note that the efficiency results of Spire and the other group at NTT are shifted upward, probably because of better cell processing technology, but follow the same general trend. The results support our previous conclusion that dislocations from lattice mismatch are the major problem with present GaAs-on-Si cells. Reducing the dislocations to the equivalent of 0.3% mismatch ($1 \times 10^6 \text{ cm}^{-2}$) should give efficiencies within 10% (relative) of GaAs-on-GaAs cells, and a density of $5 \times 10^5 \text{ cm}^{-2}$ should yield cells comparable to homoepitaxial values.

Figure 10. AM1.5 Efficiency as a Function of Dislocation Density for GaAs Cells Grown on GaAsP Buffer Layers. Also shown for comparison are Spire and NTT results for GaAs-on-Si cells.

NTT's model includes a reduction in minority carrier diffusion length and lifetime due to recombination at dislocations. It is assumed that the dislocations are randomly spaced and that they act as perfect sinks of carriers. The diffusion length of holes is expressed as:

$$L_p^{-2} = L_0^{-2} + 3 \times 10^{-11} n + \pi^3 N_d / 4$$

where L_p is the hole diffusion length, L_0 is the intrinsic hole diffusion length at low doping levels, n is the doping concentration, and N_d is the dislocation density. The second term reflects an empirical reduction in diffusion length with doping in low-dislocation GaAs, and the third term is the dislocation effect. The model curve in Figure 11 uses a value of 10.5 microns for L_0 to match the low-dislocation results, but has no other adjustable parameters. The model shows good agreement to the measured data for low dislocation densities, but tends to underestimate the diffusion length for greater than 10^7 cm^{-2} dislocations. This is probably because of the dislocation counting method and the random-spacing assumption of the model. In heavily-dislocated material the dislocations interact and are clumped, not randomly spaced. TEM, used for high densities, counts the individual dislocations. Densities measured by TEM are typically higher than by EBIC, CL, or etch pit methods, which cannot resolve the clumped dislocations. Dislocation densities counted by one of these other methods, which correspond more closely to the assumptions of the model, would show better agreement.

Figure 11. Base Diffusion Length as a Function of Dislocation Density.

Concentrator Solar Cells

Our best GaAs-on-Si cell results to date have a concentrated AM1.5D (210 suns) efficiency value of 19.9% measured at Sandia; the cell performance data include a V_{OC} of 1.04V, a J_{SC} (1-sun) of 24.9 mA/cm², and a fill factor of 0.768. For comparison, our best GaAs concentrator cell has a 200-suns, AM1.5D efficiency of 28.7% (Sandia data) as previously reported [5]. The parameters for this cell include a V_{OC} of 1.139V, a J_{SC} of 29.75 mA/cm² (1-sun), and a fill factor of 0.875. The GaAs on Si cell has a dislocation density of approximately 1×10^7 cm⁻²; to significantly improve the solar cell performance, work is presently underway to reduce the defect density to about 5×10^5 cm⁻². The primary defect-reduction techniques being pursued include the use of strained layers, TCG, and nucleation by atomic layer epitaxy [8].

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SECTION 6.0
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APPENDIX A

"Ultra Long Lifetime Epitaxial GaAs by Photon Recycling," by R.K. Ahrenkiel, D.J. Dunlavy, Brian Keyes, S.M. Vernon, T.M. Dixon, S.P. Tobin, K.L. Miller and R.E. Hayes.

Ultra Long Lifetime Epitaxial GaAs by Photon Recycling

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ABSTRACT

The minority-carrier lifetime has been measured by time resolved photoluminescence in epitaxial films of GaAs grown by metal organic chemical vapor deposition. The measured lifetimes in thicker devices are 4 to 6 times the theoretical or radiative lifetime. These long lifetimes are the result of photon recycling or self-generation of the self-absorbed radiation.

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Introduction

High quality epitaxial GaAs is of importance for a large family of photovoltaic and optoelectronic devices. Optimized minority carrier properties are especially important for both classes of devices. For example, the photovoltaic device efficiency is directly related to minority carrier lifetime. Here we use time-resolved photoluminescence to measure the minority-carrier lifetime in isotype double heterostructures.

In device modeling, the upper limit on minority carrier lifetime in GaAs is assumed to be the radiative lifetime. The radiative lifetime τ_R has been calculated for band-to-band transitions in terms of the B coefficient where N is the majority carrier density in cm^{-3} .

$$\tau_R = (B N)^{-1} \quad 1)$$

For GaAs¹, $B \sim 2 \times 10^{-10} \text{ cm}^{-3} \text{ s}^{-1}$ over an appreciable concentration range. Thus for example at $N = 1 \times 10^{17} \text{ cm}^{-3}$, the radiative lifetime is 50 ns and is assumed to be the upper limit for minority carrier lifetime in a linear model of the device.

The isotype double heterostructure(DH) has long been used as a diagnostic device^{2,3,4} for materials in the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ family of devices. The DH confines minority carriers to the GaAs active region and the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ interface has a much smaller recombination velocity than the free GaAs surface. Also the analysis of the DH device can be used to model the recombination processes in other $\text{Al}_x\text{Ga}_{1-x}\text{As}$ passivated GaAs devices. The samples used in our study are shown schematically in Fig. 1. They were fabricated by metal-organic chemical vapor deposition(MOCVD) at a variety of growth temperatures in a SPI-MO CVD TM 450 system built at Spire Corporation. Here we attempted to find processing techniques which optimize the minority-carrier lifetime. The DH device is excited by short pulses of light from a laser and the photoluminescence is time-resolved to deduce the photoluminescence lifetime. This measurement technique using a pulsed dye laser and time-correlated single photon counting to analyze DH devices have been described elsewhere⁵. Structures similar to that of Fig. 1 were fabricated with active layer thicknesses of 0.5, 1, 4 and 8 μm . Growing a buffer layer seems⁶ to increase the quality of the material and the interface.

An approximate expression for the photoluminescence lifetime of the device of Fig. 1 is:

$$\frac{1}{\tau_{PL}} = \frac{1}{\tau_R} + \frac{1}{\tau_{nR}} + \frac{2S}{d} \quad 2)$$

Here τ_{PL} is the photoluminescence lifetime, τ_{nR} is the bulk Shockley-Read-Hall(SRH) lifetime, S is the interface recombination velocity and d is the thickness of the active region. This simple expression approximates the decay rate at times $t \gg d^2/2D$ which is the diffusion transit time. Here D is the minority carrier diffusivity. The nonexponential decay seen at $t \ll d^2/2D$ is produced by increasing self-absorption as the minority carriers diffuse within the potential well. The initial ($t=0$) minority carrier distribution is simply given by Beers law. These effects will be described below in detail. In the limit of $S \sim 0$ and τ_{nR} approaching infinity(negligible SRH recombination), then $\tau_{PL} \sim \tau_R$.

Early work by Ettenberg and Kressel⁷ showed that the lifetime increased with active layer thickness for devices with an n-GaAs($1 \times 10^{18} \text{ cm}^{-3}$) active layer. Their data was interpreted by interface recombination effects of Eq. 1. However, the as-measured PL lifetime was five times larger than the calculated radiative lifetime of 4.1 ns at $N = 1.2 \times 10^{18} \text{ cm}^{-3}$ for $d > 10 \text{ } \mu\text{m}$. Later calculations by Asbeck⁸ offered an alternative explanation using the photon recycling model which to explain the anomalous lifetime. Several other workers^{9,10,11} had proposed similar effects. In the photon recycling model, self-absorption of the bulk photoluminescence efficiently generates excess minority carriers. This effect becomes large in structures which are more than 1 or 2 microns(μm) thick. Later work by Ettenberg used a special diagnostic device with a buried AlGaAs layer designed to test the photon recycling effect. The results from that experiment indicated that the photon recycling effect is small.

According to the theory of Asbeck⁸, the bulk lifetime of a device can be written in terms of a photon recycling factor ϕ as:

$$\frac{1}{\tau_B} = \frac{1}{\tau_{nR}} + \frac{1}{\phi \tau_R} \quad 3)$$

where τ_B is the bulk minority carrier lifetime. The recycling factor ϕ was calculated for AlGaAs/GaAs DH structure and increases with the active layer thickness d . The photoluminescence lifetime of a DH structure can then be written as:

$$\frac{1}{\tau_{PL}} = \frac{1}{\tau_{nR}} + \frac{1}{\phi \tau_R} + \frac{2S}{d} \quad 4)$$

A simplification of Eq. 4 has been suggested for high quality epitaxial GaAs. A recent review¹² has suggested that the bulk Shockley-Read-Hall recombination is negligible in epitaxial GaAs and the photoluminescence lifetime can be written:

$$\frac{1}{\tau_{PL}} = \frac{1}{\phi \tau_R} + \frac{2S}{d} \quad 5)$$

One can easily see that for high quality interfaces, that the PL lifetime can exceed the radiative lifetime. Such is the case when S/d is small :

$$\frac{S}{d} < \frac{(\phi - 1)}{2\phi \tau_R} \quad 6)$$

For thicker devices, the theory shows that $\phi \gg 1$ and this condition(Eq. 6) might be observed if S/d is sufficiently small. The devices in this study are all doped n-type to about $1 \times 10^{17} \text{ cm}^{-3}$. At that doping level, τ_R is 50 ns as shown above. For $d=4 \text{ } \mu\text{m}$, the theory⁸ shows that $\phi \sim 6$ and therefore $S < 3600 \text{ cm/s}$ would satisfy Eq. 6. Thus one would expect PL lifetimes greater than the radiative lifetime in such devices.

The dynamical effects of minority carrier transport including the self-absorption of the photoluminescence has been described recently¹³. The PL

decay process is given¹⁴ by the expression.

$$I_{PL}(t) = \frac{1}{\tau_R} \sum_{n=1}^{\infty} A_n e^{-\beta_n t} e^{-t/\tau_B} \quad 7)$$

where A_n is a function of S , d , the absorption coefficient of the incident light and the self-absorption coefficient of the monitored photoluminescence. The coefficients β_n are eigenvalues of the transient diffusion equation. The PL-decay time at $t \gg d^2/2D$ is then approximated by

$$\frac{1}{\tau_{PL}} = \frac{1}{\tau_B} + \left(\frac{d^2}{\pi^2 D} + \frac{d}{2S} \right)^{-1} \quad 8)$$

Here τ_B is replaced by $\phi \tau_R$ in our analysis.

Diagnostic devices of the type described above were grown by MOCVD using several growth techniques. The growth process included both interrupted and continuous growth of the interface. The growth temperatures used are 700, 740, 775 and 800 °C. Many runs were made to produce two or more devices at each temperature with all parameters being the same except the active layer thickness d . The majority carrier density was determined by capacitance-voltage measurements with a Polaron profiler (Bio-Rad Polaron PN4200).

Our measurements show that the PL lifetime of most of devices grown at 740 °C and above is greater than the radiative lifetime. The PL decay data of several typical DH devices is shown in Fig. 2. These devices were grown by the intermittent procedure at 800 °C. The active-layer thicknesses of devices A and B are 4 and 8 μm , respectively. The long-term decay times are 150.0 and 188.5 ns, respectively. The nonexponential component for $0 < t < 50$ ns is obvious in the 8 μm device B. The nonexponential behavior is more pronounced for the thick devices as the diffusion transit time ($d^2/2D$) is four

times larger than that of the 4 μm devices. By Polaron profiling, we find that the majority-carrier concentrations in devices A and B are $1.0 \times 10^{17} \text{ cm}^{-3}$ and $1.3 \times 10^{17} \text{ cm}^{-3}$, respectively. The radiative lifetimes are A(50.0 ns) and B(38.5 ns), respectively. Thus, we find that the PL lifetimes are greater than the radiative lifetimes by factors of 3.05(device A) and 4.94(device B).

An analysis of this structure, including the effects of self-absorption and subsequent internal carrier generation, was performed using a numerical technique similar to that of Kuriyama¹⁰ and coworkers. Our calculations used the formalism of Kuriyama included a detailed analysis of our particular devices. The recycling factor as a function of active layer thickness is shown in Fig. 3. Here we find that $\phi = 8.395$ at $d = 4.0 \mu\text{m}$ and $\phi = 13.55$ at $d = 8.0 \mu\text{m}$. Thus the effective radiative lifetimes at $N = 1.0 \times 10^{17} \text{ cm}^{-3}$ are 417.5 ns($d=4.0 \mu\text{m}$) and 640 ns($d=8.0 \mu\text{m}$). Using the calculated ϕ and Eq. 3, we are able to fit the data by choosing an appropriate value of S . Some of these results are shown in Fig. 4 with S as a parameter.

For growth temperatures above 740 $^{\circ}\text{C}$, we can fit the most of the data with values of $S < 2000 \text{ cm/s}$. A few devices grown at the higher temperatures indicate values of $S \approx 500 \text{ cm/s}$. A recent 4- μm device grown at 775 $^{\circ}\text{C}$ ($N = 1 \times 10^{17} \text{ cm}^{-3}$) shows a lifetime of 216 ns as seen in Fig. 4. Applying Eq. 5, we calculate a recombination velocity S of 447 cm/s. The devices grown at 700 $^{\circ}\text{C}$ show lifetimes that are many times smaller. We fit the data by assuming a much larger range of S values. For many of these devices, the effective S values range from 2×10^4 to $4 \times 10^4 \text{ cm/s}$. We believe that the higher growth temperatures mainly improve the AlGaAs and the interface rather than the bulk properties of the GaAs. Thus, dominant nonradiative recombination at the interface appears to produce the best model as expressed by Eq. 5.

In conclusion, we find that bulk minority carrier lifetimes may be much larger than the calculated radiative lifetime in $1 \times 10^{17} \text{ cm}^{-3}$ GaAs. This effect occurs only in DH devices grown at temperatures above 740 °C. The latter appear to greatly reduce the AlGaAs/GaAs interface recombination velocity. The origin of this anomaly is clearly self-generation or photon recycling as shown by the agreement of model calculations with our data.

Figure Captions

Fig. 1. Schematic of the isotype double heterostructure used in these studies.

Fig. 2. Representative data from two typical devices grown as indicated in text.

Device A: $d = 4 \mu\text{m}$. Device B: $d = 8 \mu\text{m}$.

Fig. 3. Calculated photon recycling factor ϕ as a function of active layer thickness d .

Fig. 4. Photoluminescence lifetime in ns for three different devices grown at the indicated temperatures. Solid curves are a plot of Eq. 5 with S as a parameter.

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APPENDIX B

"Assessment of MOCVD- and MBE-Grown GaAs for High-Efficiency Solar Cell Applications," by S.P. Tobin, S.M. Vernon, C. Bajgar, S.J. Wojtczuk, M.R. Melloch, A. Keshavarzi, T.B. Stellwag, S. Venkatensan, M.S. Lundstrom, and K.A. Emery, submitted to IEEE Transactions on Electron Devices for special issue on photovoltaics (February 1990).

Assessment of MOCVD- and MBE-Grown GaAs for
High-Efficiency Solar Cell Applications**

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ABSTRACT

A critical assessment of the photovoltaic quality of epitaxial GaAs grown by metal-organic chemical vapor deposition (MOCVD) and by molecular beam epitaxy (MBE) is reported. Epitaxial films of nominally identical structure were grown by the two techniques and were fabricated into p/n heteroface solar cells. The 0.5 cm by 0.5 cm cells were then characterized and compared. The MOCVD-grown films produced independently-verified record efficiency cells of 24.8% under one-sun AM1.5 global conditions while the MBE-grown films produced similarly high efficiencies of 23.8%. The

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material quality of the two films in terms of minority carrier diffusion lengths and surface recombination velocities were quite comparable. These results demonstrate that the quality of MBE-grown films can be quite comparable to the best MOCVD-grown films and that they are suitable for high-efficiency solar cells.

I. INTRODUCTION

The efficiency of GaAs solar cells continues to rise as device designs are optimized, material quality improves, and device processing improves [1-3]. To date, the best performance has been achieved for cells fabricated on films grown by metal-organic chemical vapor deposition (MOCVD), but molecular beam epitaxy (MBE) has also been used in research [4,5]. MBE is a useful tool for advanced cell research because of the relative ease with which sophisticated heterostructures can be grown. It has also proven useful for basic studies of minority carrier injection, transport, and recombination in GaAs-based cells [6,7]. The efficiencies obtained from cells using MBE-grown films, however, has been considerably less than that for MOCVD-grown films. For example, the highest reported AM1.5 global efficiency for an MBE cell is 15.7% (projected to 21% with an anti-reflection coating) [5], while MOCVD-grown cells have achieved efficiencies of 24.5% [1]. As a result, there is a concern that research results obtained from MBE-grown films might not be applicable to the more widely used MOCVD technology.

Our purpose in this paper is to critically assess the performance of high-efficiency solar cells fabricated on MBE-grown epitaxial films. MOCVD- and MBE-grown films were processed together into high-efficiency 0.5 cm by 0.5 cm solar cells (see Figure 1). We found that the important cell parameters (i.e., emitter and base diffusion lengths and heteroface recombination velocity) are quite comparable for the two technologies. The

24.8% efficiencies achieved in this study for the MOCVD-grown cells are the highest reported under one-sun AM1.5 conditions for any single junction cell. The MBE-grown films produced a slightly lower, 23.8%, efficiency which is, however, a record for MBE-grown films.

II. EXPERIMENTAL METHODS

A. Molecular Beam Epitaxy System Preparation and Growth Procedure

The MBE films were grown in a new 3-inch modular Varian GEN II MBE at Purdue University. (This MBE system has already produced extremely high-electron-mobility modulation-doped heterojunctions [8]). The growth chamber, without source furnaces, was baked at 200°C for three days. The source furnaces, and then the furnaces with their pyrolytic boron nitride crucibles, were baked in a separate vacuum chamber before placement into the growth chamber. The furnaces were then baked in the growth chamber followed by loading of source material. The arsenic source was a 99.99999% purity arsenic slug, the gallium source was 99.999999% pure, the aluminum source was 99.9999% pure, the beryllium source was 99.999% pure, and the silicon source came from a high-purity crystalline wafer. The MBE system was baked for 3 days at 200°C after loading sources.

Following the initial loading of source material, thirty-two films were grown before the two MBE films used in this work. One film was grown on a two-inch n^+ GaAs liquid-encapsulated-Czochralski (LEC) wafer (film # 120988A), while the other film was grown on a two-inch n^+ GaAs horizontal Bridgman wafer (film # 121588B). The wafers were degreased, etched for one minute in a 60°C solution of 5:1:1 $H_2SO_4:H_2O_2:H_2O$, rinsed in deionized H_2O , and placed in a non-indium wafer mount. The samples were then loaded on their carrying trolley and placed into the entry chamber of the MBE system, where they were outgassed for two hours at 200°C. The trolley was then placed into

the buffer chamber where the samples were outgassed on a heater station at 300°C for one hour immediately prior to being introduced into the growth chamber. Liquid nitrogen was circulated through the cryoshrouds starting about two hours before initiating growth. (Note the source furnaces are maintained at 200°C except for the arsenic source which is maintained at 100°C when the MBE system is idle.)

All the MBE layers were grown at a substrate temperature of 600°C (580°C is the oxide desorption temperature) and the wafers were rotated at five revolutions per minute during most of the film growth. The film growth rates were determined from monitoring the intensity of the specular spot of the reflection high energy electron diffraction pattern [9]. All layers were grown at a rate of 1.0 micron/hour except for part of the back surface field (BSF) layer (see Figure 1). At a GaAs growth rate of 1 micron/hour, the As_4 to Ga beam equivalent pressure was 20 as determined by an ion gauge placed in the substrate growth position. The BSF layer consisted of a 20 period superlattice of 28Å $Al_{0.36}Ga_{0.64}As$ barriers and 27Å GaAs wells. (The $Al_{0.36}Ga_{0.64}As$ barriers were grown at a rate of 1.0 micron/hour and the GaAs wells at 0.64 micron/hour.) The BSF field layer acts as a barrier to minority carrier holes in the n-GaAs region which increases the probability of their collection across the p-n junction. A superlattice was used for this purpose rather than just a thick AlGaAs region since, in MBE, a GaAs region grown on a superlattice exhibits a better electrical interface than when a GaAs region is grown on a thick AlGaAs region [10,11].

B. Metal Organic Chemical Vapor Deposition Growth Procedure

The MOCVD films were grown in a Spire Corporation SPI-MO CVDTM 450 epitaxial reactor at Spire Corporation. This is a vertical-geometry barrel-type reactor operating at atmospheric pressure. Five two-inch n^+ GaAs horizontal Bridgman substrate wafers were

used in each deposition run. Trimethylgallium, trimethylaluminum, and arsine were the source gases, with silane and dimethylzinc diluted in hydrogen used for n and p type dopants. In the first run (# 15271), the active layers were grown at 740°C, and in the second run (# 15523), the active layers were grown at 775°C. In both cases, the growth temperature was lowered to 700°C in the GaAs cap layer to achieve a high p^+ doping level for low-resistance non-alloyed contacts (see Figure 1). The GaAs and AlGaAs layers were grown at a rate of 4 microns/hour. The group V to group III flow ratios were 15 at 740°C and 20 at 775°C.

The structure of the MOCVD cells was nominally the same as that of the MBE cells except for the BSF layer. The MOCVD cells used a 1-micron layer of $Al_{0.3}Ga_{0.7}As$ instead of a superlattice.

C. Device Processing

Two MOCVD and two MBE wafers were processed together as a batch. The post-growth device processing sequence has been described previously [12] and was briefly as follows. First, the wafer front was coated with SiO_2 . Next a thin AuGe back ohmic contact layer was evaporated and alloyed, followed by an evaporated Au back metallization. Image-reversal photolithography was used to form a pattern for front grid metallization [13]. After etching SiO_2 in the grid openings, Cr and Au were evaporated for front contacts. The photoresist was dissolved to lift off excess metal, then the contacts were sintered. Photolithography was used to define a pattern for mesa etch (0.5 cm by 0.5 cm junctions), then a phosphoric acid-based etchant was used to form the mesa. All remaining SiO_2 was removed just prior to a selective cap removal etch (ammonium hydroxide-hydrogen peroxide system). The etch removed the GaAs cap layer everywhere except under the grid lines and exposed the AlGaAs window layer. Finally, a double-layer antireflection coating of ZnS and MgF_2 was thermally evaporated.

D. Device Characterization

The solar cell conversion efficiency was measured at Spire Corporation under AM1.5 global conditions using a Spectrolab X-25 solar simulator and a silicon reference cell calibrated by the Solar Energy Research Institute (SERI). A spectral mismatch correction on the order of 1 percent was applied. The short circuit current value was verified by integrating the measured absolute external quantum efficiency with the reference AM1.5 global spectrum [14]. Efficiency measurements were verified by SERI using standard test procedures [15].

Absolute spectral response and specular reflectance measurements were made simultaneously using a monochromator system from Optronic Laboratories. An NBS-traceable calibrated silicon photodiode was used as the spectral response standard and a clean silicon wafer was used as the reflectance standard. Measurements were made under dc conditions with no light bias. The measured cell reflectance was corrected for grid reflectance to give the reflectance R of the non-metallized surface. The internal quantum efficiency was then determined by dividing the external quantum efficiency by $(1-R)(1-S)$, where S is the grid shadow, defined as the ratio of metallized area to total cell area.

The forward dark log I-V characteristics and the $\log I_{sc} - V_{oc}$ characteristics were measured using a current source, voltmeter, and an ELH lamp with a variable power supply.

Doping profiles in the epitaxial wafers were measured by electrochemical C-V profiling [16]. Doping concentrations on the n-side were also measured by junction capacitance and on the p-side by sheet resistance using the transmission line method. Thicknesses of the cap, window, and antireflection coating layers and compositions of the AlGaAs window layers were measured by optical reflectance spectroscopy [17].

III. RESULTS

A. Structural Characterization

The dopings and thicknesses of the epitaxial layers were close to the target values for both growth techniques. Structural characterization results are summarized in Table I. In the table, optical reflectance spectroscopy (ORS) was used to determine the window thickness and composition. The other values were determined from electrochemical C-V (ECV) profiling. Excellent agreement (less than 100 angstroms difference) was observed between ORS and ECV thicknesses of the cap and window layers. The ECV dopings and thicknesses of the cap and emitter layers were also consistent with the sheet resistances of these layers.

Growth defects were readily observed with an optical microscope in the as-grown MBE material. Oval defects of types A and B [18] were both present with total densities of 500 cm^{-2} in wafer 120988A and 1000 cm^{-2} in wafer 121588B. Stacking faults at a density of $1 \times 10^4 \text{ cm}^{-2}$ were observed only in wafer 120988A. Their size indicated that they originated near the substrate/epitaxial layer interface. These types of defects were not present in MOCVD-grown films.

B. Conversion Efficiency

Table 2 summarizes the efficiency averages and standard deviations for each of the four wafers. The statistics include all processed cells on the wafers. Removing one or two low-efficiency cells from each wafer lowered the standard deviation of efficiency to 1.4 and 1.2 percent of the mean for the MOCVD wafers, and to 1.7 and 4.7 percent of the mean for the MBE wafers. The uniformity of efficiency was therefore excellent across the wafers in most cases. Wafer maps of efficiency are shown in Figures 2 and 3. For the MBE films, half of each wafer was used for solar cell processing and half for diagnostic measurements. For the MOCVD films, a full wafer was used for solar cells and another wafer from the same growth run was used for diagnostics. It can be seen that both

growth techniques produced very high efficiency cells, with 25.1% for the best MOCVD cell and 23.7% for the best MBE cell. Confirming measurements at SERI were in good agreement, with 24.8% for the best MOCVD cell and 23.8% for the best MBE cell. SERI's measurements are summarized in Table 3, and the I-V curve of the best cell is shown in Figure 4. SERI also measured the best cells under AM0 conditions (see Table 3), with the best efficiency being 21.7%.

C. Optical Characterization

The internal quantum efficiencies for one cell on each wafer are shown in Figure 5. Peak internal quantum efficiencies are nearly 1, within our measurement accuracy, for both types of cells, indicating long minority-carrier diffusion lengths and very good AlGaAs-GaAs interfaces. The long-wavelength response is similar for all cells, indicating similar diffusion lengths in the n-type base layer. The response of the MBE cells at wavelengths below 550 nm is a little lower than that of the MOCVD cells because the windows are a little thicker and the AlAs fraction (x) in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ is lower. Reflectance curves for each of the cells and our resulting analysis of the AR and window layer thicknesses using ORS are shown in Figure 6. As a point of reference, the theoretically optimum AR thicknesses are roughly 1000 angstroms for MgF_2 and 500 angstroms for ZnS. The MgF_2 thicknesses were off from the target value by about 15% for wafers 15523 and 120988A, but this only gives about a 0.15 mA/cm^2 loss in short-circuit current density relative to the optimum AR. The other two wafers were much closer to the ideal case. Grid shadow was 4.9% in all cases.

D. Junction Characterization

Figure 7 compares the forward log J-V characteristics of one cell from each wafer. (The $J_{\text{sc}}-V_{\text{oc}}$ characteristics are plotted, to avoid series resistance effects at the

highest current levels. Below $1 \times 10^{-2} \text{ A/cm}^2$, the dark J-V characteristics coincided with $J_{sc} - V_{oc}$.) At current levels corresponding to one sun illumination, all cells are limited by diffusion current with ideality factor $n = 1$. At lower current levels, the MOCVD cells are limited by $n = 2$ space-charge recombination current while the MBE cells are limited by a non-ideal leakage current with $2.1 \leq n \leq 2.6$. The higher excess current in the MBE cells is responsible for their lower fill factors relative to the MOCVD cells. Results of fitting the log J-V characteristics to the standard double-exponential model,

$$J = J_{o1}(\exp[qV/kT]-1) + J_{o2}(\exp[qV/n_2kT]-1), \quad (1)$$

are listed in Table 4. For the MOCVD cells, a 2-parameter fit (J_{o1} and J_{o2}) with $n_2 = 2.0$ gave a very good fit to the data, while the MBE cells required a 3-parameter fit (J_{o1} , J_{o2} , and n_2) with $n_2 > 2.0$. Similar diffusion saturation currents (J_{o1}) were found for MOCVD and MBE cells, indicating similar minority carrier diffusion lengths and interface recombination velocities. The lowest diffusion saturation currents were from MOCVD run # 15523.

A series of mesa-isolated diodes with areas ranging from $2.5 \times 10^{-5} \text{ cm}^2$ to 0.01 cm^2 was fabricated on the same wafers as the solar cells. Of the MBE diodes, only a few of the largest 0.01 cm^2 diodes exhibited the $n > 2$ shunt leakage exhibited by all of the 0.25 cm^2 MBE solar cells. The correlation between the $n > 2$ leakage current and diode area indicates that the leakage is due to isolated defects.

The $n = 2$ dark current of GaAs solar cells is comprised of components due to recombination in the bulk space-charge region and within the space-charge region exposed

at the perimeter of the mesa. Writing the $n = 2$ saturation current as

$$I_{o2} = J_{o2B}A + J_{o2P}P, \quad (2)$$

where J_{o2B} is the bulk component (A/cm^2), J_{o2P} the perimeter component (A/cm), A the area, and P the perimeter, shows that the bulk and perimeter components can be extracted by plotting I_{o2}/A versus perimeter-to-area ratio. The series of mesa-isolated diodes described above had P/A ratios varying from 40 to 800 cm^{-1} . From the measured dark current-voltage characteristic, the $n = 2$ current was extracted by curve fitting to (1), and the results are plotted in Figure 8.

The results displayed in Figure 8 confirm an earlier analysis which demonstrated that the dominant $n = 2$ current component arose from perimeter recombination [19]. The fact that the bulk current component is very small for both films indicates that bulk space-charge-recombination lifetimes of both the MOCVD- and MBE-grown films are high. Figure 8 shows a somewhat lower $n = 2$ bulk component (J_{o2} -axis intercept) for the MOCVD film, suggesting that the recombination lifetime may be higher for this material. However, not enough measurements were made to form a definite conclusion.

The $n = 2$ perimeter current density can be expressed as [20]

$$J_{o2P} = q n_i (S_{SCR} L_s) \quad A/cm, \quad (3)$$

where S_{SCR} is the surface recombination velocity in the exposed space-charge region, and L_s is the so-called surface diffusion length [20]. Using n_i (26°C) from Blakemore [21] and the data plotted in Figure 8, we find $(S_{SCR} L_s) = 1.2\text{ cm}^2/\text{sec}$ for both the MOCVD-grown film # 15523 and for the MBE-grown film # 121588B. This value is consistent with ref. 20

for freshly-prepared surfaces. For the MOCVD-grown, 0.5 cm x 0.5 cm solar cells, the measured $n = 2$ saturation current was quite close to the 0.7×10^{-12} A predicted from (3), n_i at 25°C, and the measured $S_{SCR} L_s$ product. This indicates that even for 0.25 cm² cells the perimeter current is dominant over the bulk. At 25°C, the average measured values were 0.98×10^{-12} A, measured 5 days after the processing was completed, and 1.3×10^{-12} A, measured 38 days later. These data are representative of time-dependent increases in the $n = 2$ current of 0.5 cm x 0.5 cm cells, which are attributed to changes in the surface condition of the GaAs. Such changes were also observed in ref. 20. Changes in the $n = 2$ current produce small changes in the fill factor of 0.5 cm x 0.5 cm cells, but should be less important in large-area one-sun cells where the perimeter is less important or in concentrator cells operated at high intensities where the $n = 1$ current is dominant.

Deep Level Transient Spectroscopy (DLTS) measurements were made on small diodes from each wafer. The MOCVD wafers showed a single deep level, tentatively identified as EL2, at concentrations of 5.8×10^{13} cm⁻³ for wafer 15271 and 4.2×10^{13} cm⁻³ for wafer 15523. No deep levels were detected in the MBE material, with a detection limit of 1×10^{13} cm⁻³.

IV. DISCUSSION

A. Comparison of Growth Methods

Because the solar cell structure and device processing steps were nominally identical for both growth methods, a comparison of device results can be used to compare the material quality of MOCVD and MBE epitaxial layers. The conversion efficiencies of cells grown by both methods were very high. Both types of materials therefore have very

high quality; the similarities outweigh the differences. However, there were some differences responsible for the one percentage point efficiency difference between MOCVD and MBE cells, as pointed out in the following discussion.

The biggest difference between the MBE and MOCVD cells was in fill factor. The fill factors of the MBE cells were lowered by non-ideal dark currents with $n > 2$ (see Figure 7); series resistances, however, were the same for both types of material. The excess leakage current appears to be related to discrete growth defects in the MBE films. Oval defects appear to be the most likely cause because they were present in both MBE wafers but not in MOCVD wafers and their density was higher in the wafer with higher excess leakage currents. The fact that the $n > 2$ leakage was observed on all of the large-area MBE-grown cells but only sporadically in small-area diodes supports this hypothesis.

We note that oval defects in MBE films can have their origins in contaminants on the starting substrate or can be introduced by the MBE system [18,22]. The wafers used in this work were cleaned in a different building than the one containing the MBE system, for reasons of expediency during construction of a new laboratory. Although as much care as possible was taken to maintain a clean substrate, the majority of the oval defects are attributable to the starting substrate condition. Based on the work of others [18,22], we expect that the oval defect density can be greatly reduced in the near future when class 100 clean-room conditions are employed for preparing the substrates.

Open-circuit voltages were limited almost entirely by bulk diffusion current for both materials, as seen in Figure 7. The diffusion saturation currents, given in Table 4, were similar for MBE and MOCVD materials. This implies that the minority carrier

recombination properties, namely bulk lifetime and heteroface recombination velocities, which determine the diffusion saturation current, were similar for the two materials. Open-circuit voltages were slightly lower on average for the MBE cells, although the best MBE cells were as good as the best MOCVD cells from wafer 15271. The $n > 2$ leakage current which limited the fill factor also accounts for a small V_{oc} loss.

The MBE-cell short-circuit currents are just slightly lower than those for MOCVD cells. Similar spectral response curves indicate comparable (and very good) diffusion lengths and recombination velocities in both materials. The small difference in short-circuit current is attributed mostly to losses in the AlGaAs window layer, which was somewhat thicker and of a lower composition (lower band gap) for the MBE cells.

In terms of uniformity and yield, MBE wafer 121588B had a higher spread in values across the wafer and a larger number of defective cells than the other three. We believe this to be caused by substrate-related growth defects. The other wafers, both MBE- and MOCVD-grown, demonstrated excellent uniformity in device characteristics across the two-inch wafers and nearly 100% yield of good devices.

In summary, the only significant difference between the two growth methods was the presence of isolated growth defects in the MBE material which increase the p-n junction leakage. The defects have not been thoroughly investigated, but the majority are attributable to the starting substrate cleanliness and should be easily eliminated as discussed above. Small differences in the thickness and composition of the AlGaAs window layer could easily be corrected in future work.

B. Effect of MOCVD Growth Temperature

The two MOCVD wafers compared different growth temperatures. Although the efficiencies were similar, there were differences favoring the higher growth

temperature. The short-circuit current was marginally higher for the cells grown at 775°C, and would have been even better with an antireflection coating identical to that of the cells grown at 740°C. The long wavelength response was higher for the cell grown at 775°C, suggesting a higher base diffusion length, although the thicker emitter and base layers for this sample were also a factor. The $n = 1$ diffusion saturation current was also lower, giving higher V_{oc} (see Figure 7). Both results suggest higher diffusion lengths in the n-type Si-doped GaAs base layer when grown at higher temperatures. The DLTS data indicated a lower deep level concentration in the sample grown at the higher temperature, although not enough measurements were taken to be sure of the statistical significance of this.

V. CONCLUSIONS

We have found that comparable materials quality for photovoltaic applications can be achieved with state-of-the-art MBE- and MOCVD-grown GaAs solar cell structures. Very high efficiency cells have been fabricated on both types of materials. The best MOCVD cells have the highest independently confirmed efficiency (24.8%) ever reported for a single-junction solar cell at one-sun terrestrial conditions. These are also the highest efficiency (23.8%) MBE-grown GaAs cells on record. The fill factors and efficiencies of the MBE-grown cells were limited somewhat by growth defects which introduced junction leakage. However, the minority-carrier transport properties were very similar for the two materials, showing that experimental results from MBE-grown cells should be applicable to the more widely used MOCVD technology.

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Figure captions

1. Nominal GaAs solar cell structure.
2. Efficiency maps (AM1.5 global, 1 sun, 25°C) for the two MBE wafers.
3. Efficiency maps (AM1.5 global, 1 sun, 25°C) for the two MOCVD wafers.
4. AM1.5 efficiency curve measured by SERI for the 24.8% efficient GaAs cell.
5. Comparison of internal quantum efficiencies for MBE and MOCVD solar cells.
6. Comparison of specular surface reflectances (no grid lines) for MBE and MOCVD solar cells.
7. Comparison of log J-V characteristics for MBE and MOCVD solar cells.
8. Plot of the extracted J_{o2} current component versus perimeter to area ratio for diodes fabricated on MOCVD-grown (# 15523) and MBE-grown (# 121588B) films. The measurement temperature was 26°C.

Wafer	Cap Thick. Doping		Al _x Ga _{1-x} As Window Thick. Doping x			Emitter Thick. Doping		Base Thick Doping	
Target Values	0.35	4x10 ¹⁹	0.03	1x10 ¹⁸	0.80	0.50	4x10 ¹⁸	3.0	2x10 ¹⁷
15271	0.35	4x10 ¹⁹	0.027	4x10 ¹⁸	0.81	0.56	4x10 ¹⁸	3.0	1.7x10 ¹⁷
15523	0.38	4x10 ¹⁹	0.030	1x10 ¹⁸	0.83	0.66	3x10 ¹⁸	3.6	2.0x10 ¹⁷
120988A	0.37	1x10 ¹⁹	0.036	5x10 ¹⁸	0.72	0.52	3x10 ¹⁸	3.0	1.5x10 ¹⁷
121588B	0.39	-	0.034	-	0.69	-	-	3.0	1.4x10 ¹⁷

Growth Technique	Wafer ID	Voc (V)	Jsc (mA/cm ²)	FF (%)	Eff (%)	# of Cells
MOVCD	15271	1.024 (0.002)	27.56 (0.25)	86.3 (1.2)	24.34 (0.43)	39
MOCVD	15523	1.027 (0.024)	27.62 (0.17)	86.0 (1.5)	24.40 (0.93)	40
MBE	120988A	1.019 (0.005)	27.41 (0.13)	82.9 (1.4)	23.14 (0.42)	15
MBE	121588B	0.987 (0.059)	27.40 (0.34)	81.4 (2.0)	22.03 (1.57)	24

Growth Method	Wafer #	Cell #	Test Conditions	Voc (V)	Jsc (mA/cm ²)	FF (%)	Eff (%)
MOCVD	15271	18	AM1.5	1.021	27.67	86.36	24.4
MOCVD	15523	5	AM1.5	1.029	27.89	86.43	24.8
MBE	120988A	14	AM1.5	1.026	27.12	84.62	23.5
MBE	121588B	22	AM1.5	1.018	27.56	84.65	23.8
MOCVD	15523	5	AMO	1.033	33.11	86.70	21.7
MBE	121588B	22	AMO	1.022	32.79	84.67	20.8

Growth Method	Cell #	J_{o1} (A/cm ²)	J_{o2} (A/cm ²)	n_2
MOCVD	15271-18	1.13×10^{-19}	5.82×10^{-12}	2.00
MOCVD	15523-5	7.98×10^{-20}	6.22×10^{-12}	2.00
MBE	120988A-14	9.30×10^{-20}	3.77×10^{-11}	2.12
MBE	121588B-22	1.32×10^{-19}	6.96×10^{-10}	2.54

Cr/Au		
p ⁺ GaAs	A.R. Coating	
p Al _{0.8} Ga _{0.2} As		0.03 μm
p GaAs	$4 \times 10^{18} \text{ cm}^{-3}$	0.50 μm
n GaAs	$2 \times 10^{17} \text{ cm}^{-3}$	3.00 μm
n ⁺ B.S.F.		
n ⁺ GaAs Buffer Layer	$1 \times 10^{18} \text{ cm}^{-3}$	
n ⁺ GaAs Substrate		
Au:Ge/Au Back Contact

Wafer 120988A

Average = 23.1%

Std. Dev. = 0.4%

Wafer 121588B

Average = 22.0%

Std. Dev. = 1.6%

2 cm

Fig. 2

Wafer 15271

Average = 24.3%

Std. Dev. = 0.4%

Wafer 15523

Average = 24.4%

Std. Dev. = 0.9%

2 cm

Fig. 3

Spire, GaAs, global, 1000W/m²

Sample: 1552-3-5

Temperature = 25.0°C

Mar. 6, 1989 3:49 pm

Area = 0.250 cm²

SERIO

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