Silicon-Film™ Photovoltaic Manufacturing Technology

Annual Subcontract Report 15 January 1992 – 15 November 1992

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Executive Summary

Introduction

AstroPower started the first phase of a three year, phased effort to upgrade its facility to produce 1.22m² Silicon-Film™ PV modules with an output of 170 Wp. In this program AstroPower will establish a baseline capability for growth of Silicon-Film™ wafers by optimizing present equipment, improving productivity of the Silicon-Film™ machine, improving solar cell performance while decreasing materials consumption, integrating and mechanizing the fabrication process for solar cells, scaling-up solar cell and module equipment for fabricating larger cells, and minimizing waste stream loads by assessing potential for waste reduction. The key contract milestones during the first year's phase are: demonstrate wafer machine productivity rate of 400 kW/year with a material use efficiency of 75% and demonstration of this capability on 675 cm² substrates.

Approach

The Silicon-Film™ Process is a method for fabricating solar cells by direct growth of a solar cell quality, polycrystalline silicon layer on a low-cost, supporting substrate. This process is designed to significantly reduce silicon cost while retaining the physical and power output characteristics of single crystal silicon. The focus for the Phase I PVMaT-2A project is on establishing the baseline process capability and optimizing the performance of the present machine.

Results

Phase I of this project has accelerated the advance of Silicon-Film™ manufacturing technology in several important ways. First, the project has led directly to our plans to make an early introduction of a large solar cell product. The successful fabrication of 646 cm² wafers and solar cells showed the way for dramatically increasing the power output per solar cell. The examination of tooling and manufacturing issues showed that the jump from 100 cm² product to 225 cm² product was a logical initial step to capture the manufacturing cost advantages of a larger product. The 225 cm² product and module based on it will meet the initial requirements which we see for a utility scale module. This product is scheduled for introduction in the summer of 1993.

Another important acceleration of Silicon-Film™ manufacturing Technology has been the establishment of a basis for the design and construction of a 2.4 MW/year wafer machine. The establishment of a baseline capability of 0.48 MW/year and an operations database during the first phase is now leading directly to our plans for developing a prototype of this machine.

Putting in place of QA/QC criteria for process steps, particularly in wafer raw material feedstock acceptance and preparation, was carried out much faster than we initially thought. These QA/QC criteria are proving crucial for us for meeting our productivity and cost goals.

A fourth important contribution to developing the technology by the PVMaT project was the determination of the importance of H⁺ implantation processes for polycrystalline silicon technologies. Cooperative work with National Renewable Energy Laboratory is proving valuable in quickly assessing the benefits to be gained by Kaufman ion sources and other material enhancement processes.

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Introduction

Project Overview

The goal of AstroPower's PVMaT-2A project is to develop an advanced, low cost manufacturing process for a new utility scale flat plate module based on thin active layers of polycrystalline silicon on a low cost substrate. This is called the Silicon-Film™ process. This new power module is based on a new large solar cell that is 675 cm² in area. Eighteen of these solar cells form a 170 watt module. Twelve of these modules form a 2 kW array. The module, array and solar cells have the features shown in Table 1.

Table 1. Utility Scale Silicon-Film Product Features

Solar Cell Size	675	cm ²
Solar Cell Power	9.45	watts
Module Size	1.23	m ²
Module Power	170	watts
Array Power	2041	watts

The program has three components:

1. Development of a Silicon-Film™ wafer machine that is capable of manufacturing wafers that are 675 cm² in size with a total product cost reduction of 70%.
2. Development of an advanced solar cell manufacturing process that is capable of turning the Silicon-Film™ wafer into a 14% efficient solar cell.
3. Development of an advanced module design based on these large area, efficient silicon solar cells with an average power of 170 watts.

The completion of these three tasks will lead to a new power module which will be designed for utility and other power applications with a substantially lower cost. The module assembly labor cost is significantly reduced because only 18 solar cells are required for a 170 watt module in contrast to 36 solar cells for a 53 watt module.

Silicon Film Technology

The Silicon-Film™ Process is a method for fabricating solar cells by direct growth of a solar cell quality polycrystalline silicon layer on a low-cost, electrically conductive, supporting substrate. The Silicon-Film™ Process is designed to significantly reduce the silicon cost while retaining the physical and power output characteristics of single crystal silicon.

A drawing of a Silicon-Film™ solar cell is shown in Figure 1.

Figure 1. Silicon-Film™ solar cell.

Silicon cost is determined by silicon quality, wafer thickness, kerf loss during sawing and wafer breakage. With the Silicon-Film™ process, a reduction in silicon consumption and processing cost in wafer fabrication is achieved while maintaining the potential for solar energy conversion efficiencies as high as standard crystalline silicon wafers.

In the Silicon-Film™ process, cost reduction begins with designed-in limits on the consumption of costly high quality silicon. Additional reductions come from the elimination of most sawing steps, the use of thinner active silicon layers, a lower cost supporting substrate, and the utilization of high yield continuous manufacturing technology. The continuous manufacturing process produces the volume to reduce the per wafer cost of capital equipment and labor while improving process control.

The photovoltaic effect in Silicon-Film™ grown on a low cost, coated steel substrate was first observed at AstroPower in August 1984 [1]. The energy conversion efficiencies of these micro-sized devices (less than one square millimeter) increased to 9.6%, without an antireflection coating, by October 1985 [2]. Larger area devices were plagued by shunts which were eventually attributed to stress caused by the thermal expansion differences between the steel and the silicon. The impact of this stress was reduced by adding a fairly thick ceramic coating to the steel which led to a 12 square millimeter, 9.6% solar cell as measured by SERI in November 1986 [3]. This thick ceramic coating led to the abandonment of steel in favor of a thermal expansion matched ceramic in January 1987. One square centimeter, 10.2% efficient solar cells were measured by Sandia in June 1987 [4]. Continued development of this approach led to the achievement of a 15.7% Silicon-Film™ solar cell measured by Sandia in December 1988 [5]. All of the above results were achieved with active silicon layers approximately 100 microns thick. Light trapping was not employed for these initial solar cells.

A series of commercial-size, 100 cm² solar cells was measured by Sandia in September 1989 with a median efficiency of 10% [6]. These results led to a focus on the development of the Pilot Scale manufacturing machine. This Pilot Scale machine was operated for eight months in a batch mode, while the data was collected and the design rules were developed for the first manufacturing machine. Present material has demonstrated efficiencies in excess of 10%.

Expected efficiency improvements are based on the product development and optimization approach utilized at AstroPower. Following are the key steps:

1. Develop a process that yields an acceptable and reproducible morphology. The key material quality test is minority carrier diffusion length.

2. Demonstrate 25 mA/cm² in a 0.1 cm² structure with a diffusion length greater than 20 microns.
3. Improve voltage and fill factor through emitter and base doping and contact optimization.
4. Improve current through diffusion length improvement using phosphorus gettering and hydrogen passivation[7].
5. Maximize performance with the addition of surface passivation and grid optimization.

Figure 2 shows the progress that has been made with the development of Silicon-Film technology during the last five years. The key progress step that has been made during the course of this project has been the demonstration of a utility scale product.

Figure 2. Progress in total area efficiency for Silicon-Film™ solar cells.

PVMaT Project Goals

AstroPower is upgrading its facility to produce 1.22 m² Silicon-Film photovoltaic modules with an output of 170 Wp. At a production rate of 19 MW/year a 70% cost benefit would be realized from the current level. AstroPower will work toward these goals by improving its manufacturing line. Table 2 shows the manufacturing technology milestones for the three phases of the project.

Table 2. Silicon-Film™ Manufacturing Technology Milestones

	Phase I	Phase II	Phase III
Wafer Machine			
Production Rate	400 kW/year	1.3 MW/year	3.0 MW/year
Material Use Efficiency	75%	85%	90%
Solar Cell Efficiency	11.0%	12.5%	14.0%
Solar Cell Size a)	100 cm ²		
b)	675 cm ²	675 cm ²	675 cm ²
Solar Cell Grid Area Coverage	9%	7%	6%
Module	130 W	150 W	170 W

Areas of focus that will enable meeting these goals include process improvements in wafer formation, solar cell fabrication and module assembly. Specifically, AstroPower will accelerate improvement in production rate and material quality of Silicon-Film fabrication machines; accelerate improvements in solar cell efficiency from 11% to 14%; and utilize large area solar cells and modules to improve parts handling efficiency. These efforts will significantly reduce materials and labor costs. In addition, AstroPower will establish the capability for increased production capacity by increasing wafer machine production rates; automating solar cell processing to accommodate larger wafers; and automating circuit formation to reduce labor costs. AstroPower will also assure that the processes developed for scale-up will minimize the generation of waste streams and minimize environmental impact.

Approach

During the first yearly phase of the project, AstroPower addressed improvements to a significant portion of its module manufacturing process. Areas of focus included improving the productivity of the Silicon-Film machine. This effort began by establishing a baseline capability for the growth of Silicon-Film by optimizing present equipment. AstroPower also improved the solar cell performance of devices made from the Silicon-Film machine while decreasing the materials consumption of the cell processing portion of the manufacturing line. In addition, AstroPower worked to decrease module costs through the integration and mechanization of the fabrication process for cells and modules while scaling-up cell and module manufacturing equipment to handle larger sizes. Plans were evaluated for parts of the line to be automated, including surface preparation, diffusion, PSG removal etch and contact printing. We evaluated the processes to assess the potential for waste reduction.

Key Results

This project has accelerated the advance of our technology:

- Led directly to the early introduction of 225 cm² Silicon-Film™ solar cell product. To be introduced in 1993.
- Prepared us for development of a continuous, 0.6 MW/shift machine
- QA driver for every step: raw material, wafer, solar cell, module
- Introduced Al back contact early into process
- Showed importance of H⁺ ion implantation

Wafer Machine Performance Benchmarks

Table 3 shows the accomplishments for wafer machine production rate in this project. The material production rate, Mr, is defined in detail and described in a later section. It is a direct measure of the productivity of the wafer machine in useful wafer area. The demonstration machine rate, DMR, is a measure of the machine productivity in terms of useful silicon generated on a continuous operation basis in MW/year. We have met the project goals for this measure both for 100 cm² and for 600 cm² size substrates. In fact, for 100 cm² substrates we have shown 0.48 MW/year rates based on machine operating rates and on the 1.1 watt solar cell made using this process. The substantial progress made during phase 1 has opened the way for early introduction of a large area solar cell product.

Table 3. Wafer Machine Production Rate, Progress and Achievements

Parameter	Jan. 1992	Sept. 1992	Nov. 1992	
	Pre-PVMaT		(1)	(2)
Mr, m ² /hr	0.14	0.57	0.57	0.64
Cell area, cm ²	100	100	100	600
Power, watt ^[1]	0.68	0.97	1.10	4.9
DMR, MW/yr	0.07	0.43	0.48	0.39

[1] Measured at AstroPower and waiting to confirm values

Another key measure of progress is the Material Use Efficiency, MUE which measures the yield of useful wafer product in terms of input silicon raw material. This yield is more explicitly defined in a later section. The goal for phase one of this project was to demonstrate a MUE of 75%. This was achieved, in effect, for 100 cm² wafers during several production runs during September.

Table 4. Wafer Machine Material Utilization Yield, Progress and Achievements

Parameter	Jan. 1992	Sept. 1992	Nov. 1992
	Pre-PVMaT		(1)
Cell area, cm ²	100	100	600
Y _a	0.95	0.99	0.99
Y _g	0.65	0.70	
Y _{VM}	0.80	0.97	
MUE, best	0.50	0.74	
MUE, monthly	0.35	0.64	0.30 - 0.35

Solar Cell Efficiency Achievements

Figures 3 and 4 shows the current-voltage characteristics for a 1.1 watt 100 cm² and a 4.8 watt 646 cm² Silicon-Film solar cell. These solar cells demonstrate substantial progress in meeting our goals for high efficiency Silicon-Film solar cells.

Figure 3. 1.1 watt, 10 cm x 10 cm Silicon-Film™ solar cell

Figure 4. 4.8 watt, 15 cm x 40 cm Silicon-Film™ solar cell

Module Assembly Achievements

An important benchmark for Silicon-Film technology is the demonstration of modules assembled from strings of large area solar cells. Figure 5 shows the current-voltage characteristic for a sub-module assembled from a string of six Silicon-Film solar cells, each of area 646 cm^2 .

Figure 5. 20 watt, 15 cm x 40 cm Silicon-Film™ sub-module

Wafer Manufacturing Process Research

Process Capability

The capability of the Si-Film Product I process is described in this section. The wafer formation process is briefly presented followed by calculations describing the areal generation rate and material use efficiency planned and achieved with the present machine. Finally, a discussion of the details of yield and machine operation are presented.

Wafer Formation Process

The process steps employed to fabricate Si-Film Product I wafers are given in Table 5. The as-received materials employed in the substrate are in bulk form. These materials are sized and suitably classified using a milling procedure. The size of the granular material is a critical parameter. The silicon material is doped using a granular doping source.

Table 5. Wafer Formation Process Sequence

Process Step	
1)	Substrate preparation
2)	Active Layer Application
3)	Active Layer Growth
4)	Wafer Separation
5)	Wafer Sizing

A setter is used as a support apparatus for the transportation of the substrate material through the active layer application and growth process. The active layer material is applied to the setter in granular form. The setters are deployed in a matter that permits the continuous growth of the active layer. Figure 6 shows a sheet of the Si-Film Product I material that is 275 cm long and 11 cm wide. The length of the Si-Film sheet is limited by the present equipment design.

Figure 6. Photograph of 275 cm x 11 cm Silicon-Film™ plank.

The growth of the active layer is accomplished in a system purged with an inert gas to reduce the effects of oxidation. The linear sheet speed, gaseous ambient and axial and transverse thermal profiles are critical parameters in achieving the proper sheet material. The process zone of the growth furnace includes three zones each requiring a tailored thermal profile. In the first zone, the liquid growth solution is created followed by a growth zone, and finally a stress relief zone.

Once formed and cooled to less than 200°C, the sheet is readily removed from the setter to be subsequently sized into a wafer. The Si-Film Product I technology permits a large degree of flexibility regarding the size wafer that can be prepared. Figure 7 is a picture of a wafer that is 15.5 cm wide and 40 cm long prepared for this contract. Figure 8 is a picture of a 15.5 cm x 15.5 cm wafer.

Figure 7. Photograph of 15 cm x 40 cm Silicon-Film™ wafers.

Figure 8. Photograph of 15 cm x 15 cm Silicon-Film™ wafers.

There are two key performance benchmarks for this project: wafer machine rate and material use efficiency. The goal for these benchmarks is to show a material use efficiency of 75% and a wafer machine operating rate of 400 kW/year. In the following paragraphs, we describe the assumptions and measurements made to meet these benchmarks and the progress made so far in meeting them. We have made substantial progress in meeting these benchmarks for both 100 cm² and 675 cm² wafers as a result of work carried out under this program.

Wafer Machine Rate Calculation

The machine rate goal for the project is to demonstrate a production rate of 0.40 MW/year for 675 cm² wafers. We have demonstrated this production rate for 100 cm² wafers. Figure 9 illustrates the geometry for a Silicon-Film sheet on the setter. The demonstration is based on the following assumptions and measurements. The demonstration machine rate is the product of the following set of factors: the areal machine growth rate, Mr, in m²/hr, the number of operating hours per year, No, and the solar cell efficiency, Eff.

Figure 9. Sheet geometry.

The equation for the definition of the demonstration machine rate is:

$$\text{DMR} = \text{Mr} * \text{N}_0 * \text{Eff} * 10^{-5},$$

where

DMR	=	the demonstration machine rate, MW/year
Mr	=	machine rate m ² /hr
N ₀	=	number of production hours per year
Eff	=	resultant solar cell efficiency, %.

The solar cell efficiency is based on the measurement of a solar cell at AstroPower which was fabricated during a 0.57 m²/hour run. This solar cell was measured at 0.97 watt. The number of hours per year is assumed to be 8000 hrs/yr, based on continuous operation of the machine. Under these assumptions and measured values we obtain a machine rate of 0.42 MW/yr. The areal generation rate is based on finished wafer area generated per hour as shown in Figure 10.

Figure 10. Measurement of machine rate.

Significant progress has been made in machine rate as a result of work carried out under this program. Specific process improvements have been: the introduction of two planks per run per setter which double the actual rate and a two-fold increase in the linear process rate.

Material Use Efficiency Calculation

The material use efficiency measures the amount of active layer silicon which ends up in the finished wafer compared to the amount of active layer silicon introduced to the beginning of the wafer formation process. Figure 11 shows the relevant geometric considerations for the calculation of the material use efficiency.

$$\begin{aligned}
 L_c &= 10.3 \text{ cm} \\
 W_c &= 10.3 \text{ cm} \\
 N &= 24 \\
 L_n &= 275 \text{ cm} \\
 W_n &= 11.5 \text{ cm} \\
 L_e &= 5.0 \text{ cm} \\
 W_e &= 0.7 \text{ cm} \\
 L_k &= 0.2 \text{ cm} \\
 Y_g &= \frac{24 \times 10.3 \times 10.3}{275 \times 11.5} = \frac{2546}{3007} = 0.81
 \end{aligned}$$

Figure 11. Measurement of plank geometric yield.

This efficiency depends on the details of the wafer formation process and can be resolved into the product of three factors: the applicator yield, Y_a , the edge trimming and kerf yield, Y_g , and the wafer visual and mechanical yield, Y_{vm} : e.g.

The equation which defines the material use efficiency is

$$MUE = Y_a * Y_g * Y_{vm},$$

where

$$\begin{aligned}
 MUE &= \text{material use efficiency} \\
 Y_a &= \text{application yield} \\
 Y_g &= \text{geometric yield} \\
 Y_{vm} &= \text{visual and mechanical yield.}
 \end{aligned}$$

The applicator yield measures the amount of silicon material applied against the amount that is moved into the growth zone. The applicator yield during the month of September was 99%. The edge trimming and kerf yield is based on comparing the number of wafers that could be obtained from the as-grown planks to the amount of material applied. For the case of two planks of 11.5 cm width grown on a 275 cm setter, the ideal yield calculated from geometric considerations is 81%. This result also depends on details of the sawing process to a minor extent. This yield during September was 82%. The visual and mechanical yield accounts for the losses of wafers due to a variety of defects as well as to mechanical breakage. The visual and mechanical yield during September was 79%. For September, the cumulative material use efficiency was 64%.

We have carried out several runs of planks, which could yield 40 wafers per run, where the material use efficiency was 73-74%. In these runs the application yield was 99%, the kerf and trimming yield was 77%

and the visual and mechanical yield was 97% , (39 good wafers out of 40 made). During September a material use efficiency value of 73% was obtained for one day's production.

Yield and Machine Operation Details

Table 6 shows the format for reporting monthly yields and downtime of the production Silicon-Film wafer machine, SF-2. The operating data shown is for the month of September. The SF-2 machine was operated in production mode for most of the month.

**Table 6. Example of Monthly Wafer Machine Operation Analysis
Shown for the Month of September**

Yield Calculation:			
	<u>Yield</u>	<u>Step</u>	
	99%	Applicator yield	
	82%	Edge trimming & kerf yield	
	<u>79%</u>	Visual & mechanical yield	
	64%	Cume. SF machine process yield, MUE	
Downtime Analysis			
	<u>Hours</u>	<u>Percent</u>	<u>Activity</u>
	115	58%	Actual run time
	34	17%	Batch load, unload time
	<u>21</u>	<u>11%</u>	System start-up, shut-down time
	170	85%	Total up time
	14	7%	Silicon-Film machine downtime
	5	3%	Downtime due to support equip. or processes
	<u>11</u>	<u>6%</u>	Scheduled preventive maintenance
	30	15%	Total downtime
	200	100%	Total scheduled operation hours for September

Visual and mechanical yields in September were limited by growth defects on the surface and wafer warping. The primary cause for the growth defects was isolated and resolved during the month resulting in a large positive yield impact toward month end. During the month a wafer warping problem was identified which was temporarily minimized by making a small increase in wafer thickness. The root causes of the warping were mechanical non-uniformities and high wear rates in the reusable setter materials. These problems were eliminated with the employment of new setter reprocessing techniques.

Table 7 shows the set of collateral benchmarks that have been achieved which demonstrate process capability for the present Silicon-Film wafer machine with respect to productivity and large area wafers and solar cells. The benchmark for machine rate productivity meets the original design specification of the machine. Although the machine was designed to run 2 to 11.5 cm wide sheets, machine modification was necessary to achieve the result. Further process development was required to realize sheet lengths of 275 cm.

Achieving 16 cm wide sheets required the adjustment of the transverse thermal profile to minimize thermal stresses, which are proportional to the square of the sheet width.

Table 7. Collateral Benchmarks Indicating Process Potential

Collateral Benchmarks	Demonstrated	Units
Upgraded Process - Machine Rate Capability	1.09	MW/year
Large Area Wafer Capability	275 cm x 16 cm	sheets
Large Area Wafer Capability	2@ 275 cm x 11 cm	sheets
Large Area Wafer Capability	15 cm x 45 cm	wafers
Large Area Solar Cell Capability	15 cm x 45 cm	cells

Wafer Machine Development

Central to the achievement of the Si-Film solar cell is the development of the wafer machine. The development of a wafer process capable of manufacturing depends on establishing control of the key process variables. There are two process variable areas being addressed dealing with environmental, and thermal considerations in the system. A discussion of the impact of these process areas on the quality of the Si-Film Product I wafer is presented in the following sections.

Environment Control

The environmental variables are the gases that are present during the product formation. The sources of these gases are those that are intentionally introduced, and those that are generated during processing. The intentionally introduced gas is argon, chosen to inhibit the formation of silicon oxide during the growth process. The presence of oxides is deleterious to the growth process, and introduces unwanted structural defects in the grown active layer of silicon. Several gases are presently being monitored; growth is not commenced unless the oxygen content in the wafer machine is less than 500 ppm.

The two sources of gases generated during processing are from the machine surfaces and the product being formed. Gases evolved from the machine surfaces diminish as the machine is run continually in its controlled environment. Procedures have been developed to minimize exposure of the machine surfaces to the outside atmosphere. The wafer machine has been modified to include a chamber located ahead of the growth zone to capture unwanted volatile constituents from the product materials.

In collaboration with the Dow Chemical Company, an in-situ quadrupole mass spectrometer was used to analyze the chemical composition of the argon atmospheres in the two wafer machines, SF-2 and SF-3. In general, the argon was found to be quite clean. Only expected gases were seen: H₂O, O₂, N₂, CO₂, H₂ (CO could not be resolved from N₂). O₂ and N₂ were about at the detection limits. Trace amounts of CO₂ and CO are expected. Thermo-gravimetric analysis with mass spectrometry, TGA-MS, of some of the process materials showed that desorption of CO₂ and H₂O could also be significant. H₂ is an expected by-product from H₂O oxidation of Si. It was seen in SF-3, but not in SF-2. There is some evidence that gases can concentrate in the argon recycle stream (e.g. CO₂, H₂). Controlling water vapor content is the main process gas concern. An on-line gas chromatograph is being constructed to monitor all of the gas species detected.

Thermal Control

Thermal control of the process is necessary to achieve the temperature ramp-up of materials prior to growth, to control the active layer growth, and to minimize defects that can occur during the temperature ramp-down of the grown layer. The achievement of prescribed axial and transverse thermal profiles are

required in both the growth and annealing zones. Detailed management of the details of energy transfer are necessary to assure the desired film growth rate.

Once the active layer has been formed it is necessary to ramp down the temperature of the solidified layer in a manner that prevents the formation of crystalline defects. Dislocations are a major defect that can occur to relieve stresses arising from improper temperature gradients during temperature ramp down. Like grain boundaries these dislocation defects can reduce the minority carrier diffusion length. It is generally found polycrystalline materials that the defect density of dislocations should be less than 10^6 cm^{-2} , and preferably less than 10^4 cm^{-2} .

Figure 12 illustrates the etch pit densities for two layers grown under different conditions, which depended on the axial thermal profile employed during annealing temperature ramp-down. For the layer prepared in Figure 12a the axial thermal profile had a steep gradient directly after complete solidification of the grown layer resulting in a dislocation density of $1.4 \times 10^6 \text{ cm}^{-2}$. A layer grown under normal run conditions is shown in Figure 12b. This layer exhibited a dislocation density of $4 \times 10^5 \text{ cm}^{-2}$.

Figure 12. Dislocation etch pit density for two thermal profile cases

The focus of the defect density reduction effort centered on profiling the Silicon-Film growth and anneal chambers. Although it is not possible to directly measure the temperature of the Silicon-Film surface in these regions we have developed a technique to measure the top surface of the moving setter with a thermocouple, which we believe roughly correlates to the wafer surface temperature. Data taken to date have shown non-idealities in both the axial and transverse temperature gradients. By adjusting process parameters, we have been able to impact the temperature profiles somewhat predictably, but we have not yet been able to optimize the profiles. Interpretation of the data collected is also non-trivial.

Machine Productivity

The productivity of the Si-Film wafer process is determined by the square meters produced per hour (throughput) that meet the product performance specification. The critical element in determining the productivity of the present wafer manufacturing line is the active layer formation step. The throughput problem for the active layer formation step is related to the area generation rate, specifically the linear

process speed and the width of the process. The following section describes the present productivity status of the Si-Film wafer machine including the issue of material use efficiency.

Linear Process Rate

The present sheet fabrication machine was designed to run in the linear speed range of 2 to 10 cm/min as determined by the thermal design of the furnace. This range was selected to encompass the range of growth regimes observed with the process, and for the purpose of gathering process control data for the construction of a machine with higher throughput. Subsequent designs will call for sheet speeds of between 10 and 30 cm/min.

An optimization of the SF-2 run parameters was employed to determine the correlation between linear process speed and device efficiency using a mesa diode loop process to prepare 0.2 cm^2 devices. The mesa loop was employed to quickly evaluate new materials, and provided many devices (~25) for statistically improved sampling. In the range of values within the design specification for the machine (2 to 10 cm/min), no significant correlation was established. Through another experimental matrix, we have determined that by increasing the resistivity from 0.3 - 1 ohm-cm to 2-5 ohm-cm, we can significantly improve J_{sc} , without a significant loss in V_{oc} .

Process Length and Width

An important step in improving process continuity and yield was made by increasing the Silicon-Film sheet length from 45 cm to 275 cm (sheet width = 11 cm). Improvements to setter preparation and transport were critical to this success. This process change was immediately implemented on our production Silicon-Film machine (SF-2). The present machine is running two 11.5 cm wide sheets in parallel yielding a productivity of 46 to 230 cm^2/min for this machine design.

Large Area Wafers

The present wafer machine is also capable of generating single wide sheets up to 17 cm wide. This capability provides the opportunity for designing solar cells having a minimum areal dimension corresponding to the width of the sheet. For the present contractual work wafers with areal dimensions of 15.5 cm x 45 cm were fabricated. The length of the solar cell could even be greater if there were any design advantages. An optimal design size based on solar cell and module performance, process yield and module cost is now being considered.

Material Usage Efficiency

At the beginning of this project typical values for material use efficiency were <35%, with the best runs in the range of 50%. As a result of effort under the PVMaT-2A project significant improvements in this operating parameter have been obtained. Specific improvements include: introduction of an in-line applicator, increase in effective growth width by employing two planks per setter per run, detection and elimination of impurities which cause visual and mechanical defects, improvements in setter construction and refurbishment and reduction of water vapor in the argon ambient which caused visual defects in the wafer surface.

Figure 13 shows the increase in material use efficiency that was realized with the improvement in setter construction. Prior to this development the areal yield of product was strongly influenced by the growth

commencement and termination zone. These zones comprised a significant portion of the 45 cm sheet length that was determined by the setter design. Modifications to the design have led to the achievement of 275 cm long sheets. Further increases in material utilization efficiency are achieved with the use of wider sheets as illustrated in Figure 13.

Figure 13. Increase in MUE due to employment of longer and wider sheets.

Wafer Quality Requirements

The most important electrical parameter determining the level of quality of the Si-Film active layer is minority carrier diffusion length. Both the magnitude of the minority carrier diffusion length and its spatial uniformity are important in establishing the utility of any photovoltaic material. This section describes the level of solar cell performance achieved and planned with present Si-Film material, indicates the causes that limit performance in this material, and demonstrates the high degree of spatial uniformity achieved in material and device parameters.

Performance

As we learn to better operate and control the wafer machine, the performance of solar cells fabricated with the material continues to improve. The best measure of potential solar cell performance is minority carrier diffusion length. Figure 14 summarizes the predicted power from the nominal 100 cm² Si-Film solar cell as a function of diffusion length and current density for the present solar cell design and an advanced solar cell design. The case for the present design includes no passivation, a grid coverage of 94%, an emitter sheet resistance of 80 ohms/sq., an open circuit voltage of 0.56 volts and fill factor of 0.72. The advanced

solar cell design incorporates a grid shading of 3.2% , surface passivation leading to a 4% increase in current and a voltage increase to 0.60 volts, and a fill factor increase to 0.74.

Figure 14. Predicted efficiency as a function of Ln

Si-Film Product I material, prepared with recent process parameters, achieves a minority carrier diffusion length of 20 microns. Reference to the predicted performance curve in Figure 14 indicates that this material leads to a solar cell with power of 1.05 watts and short circuit current of 2.7 amps; these values are close to those indicated in the solar cell data shown in Figure 3.

Causes Limiting Performance

Determining the causes that limit the minority carrier diffusion has been the focus of an ongoing program to improve the Si-Film material. There are three major areas that are being examined: impurities, defects and residual stress. The following sections will discuss each of these areas, and indicate the extent to which it they may be operative in limiting minority carrier diffusion in the present material.

Impurities

There are several ways that the presence of chemical impurities can deleteriously affect the quality of the material. The impurity may introduce an energy level in the vicinity of the midgap where it acts as a minority carrier trap, reducing minority carrier diffusion length. Alternatively, the impurity may introduce an energy level in the vicinity close to the conduction-band or the valence-band where it may act as an acceptor or donor, respectively , thereby controlling the conductivity of the material. The nature of the energy level introduced by the impurity is dependent on its location within the lattice (as a substitutional or interstitial). Furthermore, some impurities are subject to removal, or deactivation, as the consequence of subsequent processing, for example by gettering or hydrogen passivation. Impurities may also interact with structural defects, or cause structural defects by precipitation. Recent developments employing hydrogenation of Si-Film material have led to significant improvements in device performance, and will be discussed in a later section.

There are two sources of impurities, and owing to the method of growth, a means for purifying the material during sheet growth. The two sources of impurities in the final sheet material are those introduced with the starting material, and those introduced from the growth system during layer growth.

In collaboration with the Dow Chemical Company, a detailed chemical impurity analysis of the Silicon-Film process was performed. The ICP techniques were the method of choice for analysis of incoming Silicon-Film raw materials, however detection limits may not be adequate for resolving electrically active impurities in the grown wafers. To complement the ICP data, wafer samples were sent to an outside vendor for SIMS profiling.

Most of the metallic impurities appear to be coming in with the current supply of silicon (Fe, Ti, W, Cr, Ni). Some impurities are added in the material preparation process (Al, Ba, Ca, Mg, Sr). These impurities correlate well with expected contaminants. However, they are expected to cause minimal photovoltaic degradation, since they are probably tied up as relatively benign alumina inclusions after wafer formation. The material application process steps do not add significant impurities.

The distribution of the impurities in the finished active layer was investigated. Results from SIMS depth profiling of our as-grown Silicon-Film wafers, performed by an outside vendor through the Dow Chemical Company, indicate evidence for concentration of several transition metals to the top surface of the wafer, as expected because of segregation during crystal growth. The impurities are removed in the solar cell fabrication process by the hot NaOH etch during surface preparation before diffusion.

EDAX analysis of dendritic growth surface defects on Silicon-Film wafers found Fe and Cr precipitates at the grain boundaries. Several sources of metallic contamination in the preparation of the active layer silicon were identified and resolved. The frequency of dendritic growth defects has been dramatically reduced since these process modifications.

Defects

Crystalline defects can be the source electrically active regions in the crystalline lattice, regions that can deleteriously affect the minority carrier diffusion length. The three major categories of crystalline defects include planar defects (e.g. grain boundaries), line defects (e.g. dislocations) and point defects (e.g. silicon vacancies and interstitials). Since the grain size of Si-Film material is in the range of 150 to 1000 microns, and the minority carrier diffusion length is 20 microns, it is not likely that grain size is the present limit to diffusion length. However, it is generally accepted that it is preferable to achieve a dislocation density of less than 10^4 cm^{-2} in order to realize minority carrier diffusion length in excess of 100 microns. Again as in the case with grain boundaries, not all dislocations are necessarily electrically active in a way to deleteriously affect minority carrier diffusion.

An area of major focus in this project has been dislocation density characterization and reduction. We established a process for etch delineation of crystal dislocations and etch pit counting. A chemical polish procedures were developed which allowed us to defect etch the as-grown wafer surface, to defect etch in cross-section, and to defect etch small area mesa devices. Refinements were required to improve the counting technique, reduce noise in the data, and to resolve slight discrepancies between EPD measured in cross-section, on-mesa, and off-mesa. Figure 15 shows a photograph of the decorated defects on a 0.1 mm^2 circular mesa, and in the vicinity directly adjacent to the mesa structure. The dislocation density is $3.3 \times 10^5 \text{ cm}^{-2}$ on the mesa device, and $5.7 \times 10^5 \text{ cm}^{-2}$ in the off-mesa vicinity.

Figure 15. On mesa/off mesa defect density, Area = 0.1 cm²

By improving etch pit density (EPD) counting and averaging procedures, and by upgrading both our spectral response hardware and software, we were finally able to establish a correlation between minority carrier diffusion length (L_n) and dislocation density for intentionally defected control structures. However, we have not been able to establish this correlation for Silicon-Film™ Product I structures. The natural variation in EPD across the mesa device area measured by spectral response is much larger than the EPD variation from sample to sample. This results in very noisy data. The solution is either to shrink the area of the mesa, or to use another technique, such as LBIC or EBIC, to improve the resolution of the diffusion length measurement. Since shrinking the mesa device area will require significant development, we are not pursuing that option. We are currently developing a simple LBIC scanning system. Eventually we hope to be able to extract spatially resolved diffusion length data by scanning with multiple laser wavelengths.

Residual Stress

At temperatures above 600°C thermal stresses, that occur as the consequence of non-linear thermal profiles, can be relieved by plastic deformation in solid silicon. Plastic deformation of the crystal lattice results in the generation of dislocations. At temperatures above 1200°C dislocation generation is the main mechanism for thermal stress relief. At lower temperatures stress can also be partially relieved by warping. Thermal stress not relieved by dislocations or warping will result in residual mechanical stress. Residual mechanical stress can also be the source degradation of electrical properties of the crystalline material.

The present as-grown Si-Film material is quite flat as removed from the growth furnace and contains on the order of $1 - 10 \times 10^5 \text{ cm}^{-2}$ dislocations. Thinner sheets of the material do exhibit some measure of warp suggesting the need to further tune the sheet annealing temperature profile. It is further anticipated that there are also residual stresses present in the material. We are investigating methods for measuring these residual stresses.

Spatial Uniformity

The fabrication of large area photovoltaic solar cells requires the availability of large areas of material that possess uniform electrical and optical properties. Moreover, it is necessary to accomplish spatial uniformity with all subsequent processing of the material on its way to becoming an active device. This section describes the spatial uniformity of the material resistivity and device response achieved with the present Si-Film process.

Material Properties

Figure 16 shows a plot of the resistivity as a function of the position along the 275 cm long sheet. The target resistivity for this sheet was 0.65 ohm-cm. Figure 17 shows three SIMS depth profiles for boron in the sheet and indicates that the concentration level to be quite uniform up to the three microns measured for each of the concentrations. The resistivities are 0.3, 0.5 and 1.0 ohm-cm for the high, middle and low boron concentrations, respectively.

Figure 16. Resistivity profile along plank

Figure 17. Boron depth profile in silicon active layer

Device Properties

Figure 18 shows the spatial dependence of the minority carrier diffusion length for a recently optimized Si-Film material and device process. [10] These data are the result of the analysis and development of a technique by Paul Basore and Paul Schanwald at Sandia. The technique involves the measurement of absolute responsivity for high-resolution laser scans at two separate wavelengths; these data are used to compute the diffusion length in the material as a function of position. Figure 19 shows an expanded 5 mm region of the data shown in Figure 18. In Figure 19 the entire data set falls between 9 and 30 microns, with no gross boundary effects evident. This indicates a relatively smooth and constant diffusion length as a function of position. The resolution of the curves is evidenced by the sharp edges seen for the gridlines in Figure 19.

Figure 18. Diffusion length from multi-wavelength LBIC scan of Silicon-Film solar cell

Figure 19. Expanded scale multi-wavelength LBIC scan of Silicon-Film solar cell

Figure 20 shows an EBIC scan of an unoptimized Si-Film junction. [11] The data show the EBIC linescan, the scan position and the Y-modulated EBIC map that details the grains in the material. These data indicate that there may be up to 50% reduction in response at some grain boundaries in this unoptimized process.

Figure 20. EBIC Scan of Silicon-Film Solar Cell

Statistical Process Control

As a preliminary step toward developing statistical process control for the wafer fabrication process, three attributes of the material stream resulting in the wafer product were identified and pertinent data were gathered and analyzed. .

A measurement and sampling procedure for silicon powder bulk density was developed, data were collected for 22 lots, and Xbar and R control charts were generated. Although variation from the mean value was small (+/- 2%), the control charts showed that bulk density was slightly out-of-control, indicating there is some non-random variation in milling process or incoming raw material. This non-random variation was investigated, and an assignable cause was established and corrected. This measurement is presently being employed as a statistical process control monitor.

A method for measuring active layer silicon material particle size distribution was developed, and daily data are being collected as part of the procedure for establishing this parameter as a process control monitor.

A sampling procedure was also developed for Silicon-Film wafer weight. Xbar and R control charts have been generated, an example of which is shown in Figure 21. Although wafer weight is in statistical process control, indicating the process variation is random, the process is not yet capable of meeting the process specification at 100% yield (i.e. $C_p < 1$). These control charts for wafer weight are being implemented as SPC monitors.

Table 8. Process Parameters Selected for SPC Treatment

Parameter	Type
Silicon Powder Density	Input
Silicon Powder Size Distribution	Input
Silicon Powder Resistivity	Input
Finished Wafer Weight	Output

Figure 21. Wafer weight control charts showing in-control process parameter

Solar Cell Process Research

The goal of this task was to identify and implement processes to improve solar cell efficiency. Areas of focus included diffusion, fine line metallization, in-line hydrogenation and AR coating and gettering. The efficiency goal for this task was an 11% Silicon-Film™ solar cell process.

Baseline Solar Cell Process Sequence

Work focused on refining the baseline process sequence. We conducted a series of experiments to optimize the firing time and temperature for the emitter junction. These experiments were combined with diffusion experiments targeted at increased blue response for the final diffusion step. A low cost all aluminum back contact process was prototyped and evaluated.

Four process sequence variations which compared the standard process diffusion to a 'gettering' diffusion were conducted. The objective was to determine the influence of surface treatment and sequence of processes on obtaining optimal electrical properties and electrical contact integrity. Comparison of the measured parameters of electrical performance and mechanical yield for the four process sequences showed one of the sequences to be superior, shown below in Table 9.

Table 9. Baseline Solar Cell Process Sequence

	Process Step
1)	Surface Preparation
2)	Gettering Diffusion
3)	Etch Gettered Junction
4)	Standard Shallow Junction Diffusion
5)	PSG Removal
6)	Print/Dry Back Contact
7)	Print/Fire Front Contact
8)	H+ Passivation
9)	AR Coating
10)	Contact Burnishing
11)	Test

Process Development Research

PECVD Hydrogen Passivation

A hot wall PECVD tube reactor for hydrogenation and Si₃N₄ deposition was brought on-line for production as well as for process improvement studies. The goal of the process studies was to characterize the hydrogenation and AR coating processes to be able to specify an in-line process which combines these two steps in a sequence. RF power, wafer temperature, gas flows and process time were varied to determine the minimum time necessary for acceptable solar cell performance.,

A full-factorial experimental design exploring hydrogenation times and RF power levels was developed using the ECHIP™ software. The purpose of this experiment was to find optimum system conditions (to

maximize percentage gain, and minimize process time) for Product I wafers, and to begin defining the conditions for in-line processing.

The first experiments were conducted to determine the range of hydrogenation time and RF power levels. Twenty-five Product I wafers from the standard process sequence were included for each trial in the experimental design. The percentage gains in open-circuit voltage and maximum power were used as response variables.

The data were analyzed using a factorial model by the ECHIP software. Figures 22a and 22b show the performance output contour maps as a function of process variables. The parameters determined for the model indicate that process time has the most significant effect on both Voc and Pmax, with RF power having a slight effect. For process development purposes, the contour plots confirm that the "standard" process yields acceptable electrical performance improvement.

Figure 22. Contour plots of percentage changes in Voc and Pmax, For Hydrogenation Times (minutes) and RF Power, (percentage of Maximum).

Kaufman Ion Source Hydrogenation Studies

The PECVD process studies described in the previous section showed improvements in the range of 30-35% in Pmax for some of the early wafer material fabricated. These improvements resulted from increases in current, voltage and fill factor. As the wafer formation process developed, the amount of enhancement derived from H^+ treatment decreased to the range of 15%, with current improvements in the range of 5%. The reason for this decrease may be related to the differences in thermal post processing of the wafer. In any case, we sought evidence that improvements could be gained by other H^+ methods since we did not see increases in final diffusion length as the wafer process evolved.

Information gained from the Second Workshop in the Role of Point Defect/Defect Complexes in Silicon Device Applications in August 1992, sponsored by the National Renewable Energy Laboratory, showed that employment of Kaufman ion sources was a more reliable method to obtain H^+ enhancement if the

material responded to hydrogenation at all. We arranged to treat samples of Silicon-Film wafers at NREL with the collaboration of B. Soporì. [12] Table 11 compares mesa diode, short circuit current results of the two hydrogenation methods to untreated material. It is clear that substantial current gains can be obtained by employment of the Kaufman ion source.

Table 10. Comparison of Hydrogenation Methods on Mesa Samples

Sample	Jsc (ma/cm ²)	Improvement (%)
As-Grown	16.51±0.42	-
PECVD H ⁺ Process	17.36±0.67	5.1
Kaufman Ion Process	19.39±0.12	17.4

As a result of this work we have started the acquisition of a Kaufman ion source for studies at AstroPower.

Si₃N₄ AR Coating Process

Screening experiments using mechanical substrates were conducted exploring RF power and deposition time effects on process uniformity. The deposition rate was observed to be linear with respect to RF power; i.e., for a 2x increase in RF power, the time needed to deposit an AR coating was cut by half. No significant change in uniformity either on-boat or on-wafer was evident.

Combined PECVD Processes: Hydrogenation and AR Coating

An important saving in process cost is obtained by combining the H⁺ passivation step and the Si₃N₄ AR coating step into one operation sequence, rather than in two separate steps requiring separate vacuum entry/exit pump/purge cycles.

A full-factorial experimental design exploring hydrogenation time and RF power for the combination H⁺/AR process was conducted. The experimental space was determined by the results of initial screening experiments. Based on the results of the experimental matrix a combined sequence was developed and implemented in production.

Solar Cell Characterization

Quantum efficiency measurements of Silicon-Film™ solar cells have been performed, demonstrating blue response typical of standard production solar cells. Improvement of blue quantum efficiency to a level seen in high-performance solar cells is considered to be an area for improvement needed to achieve project performance goals. Figure 23 shows quantum efficiency data, measured at the Photovoltaic Device Measurement Laboratory at Sandia National Laboratories, for the Silicon-Film™ solar cell shown in Figure 4. [13]

**Figure 23. Quantum efficiency of a Silicon Film solar cell,
 (measured at Sandia National Laboratories)**

The solar cell modeling program, PC-1D, has been employed to model and characterize both the optical properties of the $\text{Si}_3\text{N}_4/\text{SiO}_x$ over Si coatings, and the electrical properties of the high-performance junction. PC-1D results suggest that with a high-quality junction and a thin (less than 200 Angstroms) oxide layer, the internal quantum efficiency at 400 nm will be near 95%, with a minimal change in global reflection as compared to a Si_3N_4 AR directly over Si.

Modifications to the production line CVD system to deposit SiO_x were implemented in the PECVD system. PC-1D modeling along with reflectance measurement techniques was used to optimize the deposition characteristics of the SiO_x and Si_3N_4 layers to maximize short-circuit current. These results were employed to develop the $\text{H}^+/\text{SiO}_x/\text{Si}_3\text{N}_4$ CVD process presently used in production.

Fabrication of 15 cm x 45 cm Solar Cells

Development of larger solar cell processing capability was carried out in two phases during the course of the work. The first phase was devoted to assessing the requirements for scale-up by fabricating solar cells on a bench scale. The second phase was aimed at fabricating a significant number of large solar cells using production scale equipment.

15 cm x 45 cm Solar Cell Prototyping

In the first phase we fabricated the largest possible solar cells using the available equipment set with the addition of prototype or bench scale equipment at certain steps to accommodate solar cells at least as large as 15 cm x 45 cm.

Smooth, mechanically strong wafers, 15 x 45 cm, were fabricated in the SF-2 production machine. Little modification from 10 cm x 10 cm tooling was required. The wafers met the flatness specification of the 10 cm x 10 cm wafers normally produced. Large solar cells were successfully fabricated from these wafers using a modified process sequence. The solar cell fabrication process tools were identical to standard 10 cm x 10 cm production tools for all processes except for printing and AR coating. A hand operated screen print station for printing the front pattern was employed to print the contacts. The contact pattern screen was identical to the one which will be employed in the automatic printer to be developed later in the program. Print resolution and quality met the requirements for present product. A metal oxide AR coating was applied at a hand operated coating station employing a process used on the single crystal silicon solar cell production line.

The solar cells produced were mechanically strong and readily able to survive four high temperature processes: standard diffusion, back contact firing, front contact firing and spray pyrolysis AR coating.

The gettering and H^+ passivation steps were not employed in this initial effort. The Silicon-Film, polysilicon active layer material requires both the use of gettering and the use of the H^+ and Si_3N_4 AR coating process steps to obtain optimal currents and fill factor. These steps, in the proper combined sequence, produce significant passivation of defects in the bulk and at surfaces as well as efficient optical coupling of the incident radiation as described previously. The simpler metal oxide, spray pyrolysis CVD process was employed because the process tooling could readily accommodate the large solar cell at that time.

The results of this task to this point established the ability to process large wafers into completed solar cells with a minimum of difficulty. The issues for automation of the processes for large solar cells appear to be reduced to mechanization of current, known processes.

15 cm x 45 cm Solar Cell Prototype Production

The aim of the next phase of large solar cell fabrication was to fabricate solar cells on the order of 650 cm² using all of the baseline processing steps and which could be assembled into modules. We determined that the largest solar cell that could be laminated in a string into a 43 cm² by 90 cm² structure was about 15.6 cm by 41.6 cm². The laminate structure was dictated by lamination capacity, as discussed in a later section. This solar cell size is within 6% of the cell area goal for the project. These dimensions also had the virtue of allowing us to fabricate the solar cell using all of the baseline process sequence, on available equipment, at rates that were useful.

Enough runs of 275 cm by 16.2 cm planks were made on the Silicon-Film production wafer machine to be equivalent to 240 finished wafers. As shown in Table 4, the net yield of wafers was in the range of 32%. One key contribution to the low wafer yield was the employment of a diamond scribe and break process to convert sheets into wafers. This process has an intrinsically lower yield than the sawing process. Plans are being implemented for upgrading the saw to handle larger wafers. It should be noted that early production runs of 10 cm x 10 cm wafers experienced similar yields. These yields dramatically improved as a result of learning to control the wafer production process. We expect similar improvement with large wafer fabrication.

77 wafers were introduced to solar cell processing. Two processes were employed. The first process was the baseline process which uses a screen printed front and back contact. The second process was the same as the baseline process except for the use of electroplated front contacts. The purpose for using the electroplated front contact was to assess the best device performance of the material. The screen print front contact process has required a lot of tuning for optimization, particularly for the large solar cells. It was believed that more consistent results for material evaluation can be obtained with the front contact electroplate process.

A total of 41 wafers were completed. The mechanical losses primarily occurred at three steps: diffusion, screen printing and contact firing. The causes of breakage appear to arise from two sources. The first is lack of adequate flatness. The second is stress induced by thermal processing. Standard production Silicon-Film wafers, 10 cm x 10 cm, have much higher mechanical yields, through the solar cell fabrication process.

The solar cells were tested both in sunlight and inside on a modified test set. The indoor testing was difficult because of light source non-uniformity and difficulty of contacting to the back plane. The outdoor tests were conducted by tabbing each solar cell on the front. Better results could be obtained by tabbing the back. A special fixture was fabricated for the large solar cells to hold them and to make the back contact. Test results for the outdoor tests of some of the better solar cells are summarized in Table 12. These results are corrected to 25° C from the measured data using the change in Voc as an indicator of the change in temperature of the junction.

Table 11. 15 cm x 42 cm Solar Cell Performance

Parameter	high	average
Voc, volts	0.526	0.509
Isc, amps	14.20	12.48
Pmax, watts	4.84	3.86

These are the largest known solar cells that have ever been fabricated, with an area of 647 cm². The current densities for the best solar cells were on the order of 22 ma/cm², which is about 10% less than the current densities seen for the best 10 cm x 10 cm solar cells. This result shows that the sheet formation and solar cell fabrication processes are sufficiently uniform to support the production of large solar cells. We expect that with modest improvements in the process sequence that the large solar cells will be equivalent in performance to present production.

The results of this fabrication effort were important for directing our future effort. They can be summarized as follows:

- we determined requirement for wafer flatness for large solar cells

- the process is scale-able
- the results are predictable from 100 cm² solar cell process.

The results of fabricating these solar cells into modules are described in a later section.

Waste Impact/Cost Minimization Report

The goal of this task was to assess opportunities to reduce the amount of hazardous materials used and waste materials generated by the solar cell fabrication processes. The approach was first to measure the materials used and generated by the processes and second to evaluate opportunities for reduction or elimination of waste material generation.

A process audit was conducted for the baseline Product I process to determine its waste load. There are two primary streams of interest: the effluent stream from the various wafer etch and cleaning processes and the silver paste clean-up stream from cleaning printing screens. A third stream is the air exhausts from the furnace and CVD processes, which are relatively minor.

Using the results obtained in our survey, we found two opportunities for significant reductions in waste stream generation: reduction of sodium hydroxide etch waste and sodium hydroxide regeneration.

NaOH Etch Process

A solution of sodium hydroxide is used as part of the process sequence to prepare the front surface of the silicon active layer before diffusion. In the conventional Cz and polycrystalline silicon technologies, silicon substrates are formed from ingots by sawing. Sodium hydroxide is employed to remove the saw damaged layer which is on the order of 60 to 70 microns thick. This etch process generates a waste stream of sodium silicate in water. We found that the preparation of the Silicon-Film wafer for diffusion requires substantially less etching for two reasons. The first is that there is no saw damage to remove. The second is that only a thin layer on the surface needs to be removed. This is because impurity segregation during the active layer formation concentrates some of the transition elements in this layer. As described in the previous section on beneficial segregation of impurities, we found that the deleterious elements concentrated in a 5 micron layer on the surface.

Sodium hydroxide etch time experiments were conducted to evaluate the time required to remove surface layer impurities before diffusion. The results for Voc and Isc for mesas diodes as a function of etch time in seconds are shown in Figure 26. This data shows that removal of impurities occurs within 15 seconds. This time corresponds to removal of 10 microns.

Figure 24. Sodium hydroxide etch time mesa results

The sodium hydroxide etch process time was reduced from 2.5 minutes to 15 seconds, a ten-fold decrease. This reduced the waste stream generation rate for sodium silicate by a factor of ten.

NaOH Regeneration

A concept was developed for the reduction of sodium silicate in the waste stream load based on the regeneration of sodium hydroxide. This concept is being reviewed for patentability.

Advanced Module and Panel Design

The goal of this task is to evaluate alternatives for solar cell, module and panel designs and then to prototype the solar cell and module designs. The result of successful completion of this task will be specifications and designs which will minimize cost of manufacture and optimize product performance. The focus of this task is to implement designs which employ large solar cells in large modules. The baseline module design is to employ 18 15 cm x 45 cm solar cells in a 2 x 9 series arrangement. Another important objective is to match solar cell and module manufacturing process techniques to assure a high performance, high reliability product.

Module Assembly and Process Development

We established a module fabrication process development and test capability. A baseline process sequence was determined as shown in Table 13. The primary goals was to evaluate alternative assembly processes, to establish process yields for module manufacture using Product I solar cells and to fabricate prototype modules.

Table 12. Baseline Module Assembly Sequence

	Process Step
1)	Tab solar cells
2)	String Circuit
3)	Lay-up Laminate
4)	Vacuum laminate
5)	Electrical test laminate
6)	Frame
7)	Mount termination box
8)	Electrical leakage test

Front and Back Contact Interconnection Process Development

During the course of the project several variations in the solar cell process sequence have been assessed. These variations have had significant impact on process development for module assembly.

The base-line process developed for solar cell fabrication added an etch step after the gettering diffusion process. Solar cells produced by the base-line process were used in assembling modules to evaluate issues in module manufacture, particularly at the front contact process. As expected, contact pull strengths for the front contact were found to increase by the use of a gettering etch after the gettering diffusion step. The solar cell performance and contact pull strength were optimized by varying the contact firing conditions. High pull strength bonds to the front contact have been consistently achieved.

All Aluminum and Gridded Silver Back Contact Systems

A new all aluminum, screen printed back contact process was developed which offers significant potential for cost reduction, while improving the solar cell electrical output. It has been our intent for some time to replace the all silver back contact with a modified back contact which would reduce or eliminate the use of silver. The back contact under development eliminates the use of silver which is expensive and which generates a minor waste stream of silver particles. Work in the advanced module development focused on

developing a technique for bonding the solder coated ribbon interconnect to the solar cell back contact. Three basic techniques were investigated for the interconnect bonding process: use of conductive adhesives, welding, and direct solder attachment.

Conductive adhesives did not prove to be capable of meeting the performance requirements. Bond strength was poor and contact resistances were too high. Extensive experiments were conducted with welding processes using a Hughes parallel gap resistance welder. Bonding could be achieved with low contact resistance, but the pull strength of the tab bonds was too low. The failure mode appeared to be thermal stress failure in the silicon as evidenced by the failure of the bond in the silicon layer with conchoidal fracture. We were not able to obtain a process window which produced a good bond to the silver/glass contact while not damaging the underlying silicon layer.

An interim process for direct solder attachment was developed. This process required an additional process step to prepare the aluminum for soldering. A cost/performance comparison with gridded silver backs was conducted. We found for the present, that the lowest cost, highest performance option was the employment of gridded silver back contacts.

Solar Cell and Module Design

The contact pattern employed for the first phase 15 cm x 45 cm solar cell was based on the same pattern employed in the standard 10 cm x 10 cm Silicon-Film™ solar cell: 0.15 cm spacing between grid lines and 5 cm spacing between bus-bars. These parameters result in a 9 bus-bar pattern with 46 grid lines, yielding a shading loss of 10.5%. A detailed analysis of the front contact design was conducted to determine an optimal pattern. A better design was produced using present values for printing parameters and electrical characteristics. This design employs 7 bus-bars and 36 grid lines, yielding a shading loss of 8.9%. The difference in pattern coverage is shown in Figure 27. This result is important because it helps determine the complexity of the tabbing and stringing operation. Clearly, the fewer the bus-bars the fewer front to back interconnect ribbons. The 7 bus-bar design was employed for the second phase of large solar cell fabrication.

Nine Bus-Bar Design

Seven Bus-Bar Design

Figure 25. Seven bus-bar pattern vs. nine bus-bar pattern for large area solar cell

Design and Prototyping of Large Modules

The baseline process was reviewed to determine the steps requiring modification to accommodate 15 cm x 45 cm solar cells. A solar cell and module design for 15.7 cm x 41.6 cm solar cells in an 18 cell and a 6 cell module configuration was completed. The six solar cell configuration was chosen to enable us to fabricate a large cell module while a larger laminator was being fabricated.

Conclusions

We have demonstrated the first level of Silicon-Film wafer machine capability required for high volume production. Based on these results we are preparing for development of next level semi-works production machine. The material use efficiency for the silicon feed-stock of 74% is substantially higher than that for other technologies and can be improved to about 95% by incorporating a continuous fabrication process. Solar cell power over 1.1 watt marks an important productivity threshold. We have demonstrated the capability to fabricate large area solar cells and to incorporate them into modules. Performance improvement of the solar cell process sequence will be obtained by optimizing the uniformity of the diffusion, front contact formation and AR coating processes. Significant improvements in hydrogenation gains may be obtained by employing Kaufman hydrogen ion sources. The large solar cell results obtained substantiate the assumptions for the cost reduction advantages for large solar cell production.

Key Conclusions

We have accomplished the goals of the first phase of the project by:

- Significant improvements in performance and productivity
- Larger size solar cell direction was validated
- Directions for future improvement well defined

Effect on Product Introduction

The program has accelerated the advance of our technology:

- Led directly to the early introduction of 225 cm² Silicon-Film™ solar cell product. To be introduced in 1993
- Prepared us for development of a continuous, 0.6 MW/shift machine
- QA driver for every step: raw material, wafer, solar cell, module
- Introduced Al back contact early into process
- Showed importance of H⁺ ion implantation

Plans for Phase II

- Improve productivity of Silicon-Film machine
- Explore wafer process boundary conditions
- Develop a Silicon-Film Wafer machine with improved performance
- Improve solar cell performance
- Integrate solar cell and module line processes

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