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Silicon-FilmTM on Ceramic Solar Cells

Final Report

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ABSTRACT

The Silicon-Film™ design achieves high performance through the use of a thin silicon layer. Optimally designed thin crystalline solar cells (<50 microns thick) have performance advantages over conventional thick devices. The enhancement in performance requires the incorporation of back-surface passivation and light trapping. The high-performance Silicon-Film™ design employs a metallurgical barrier between the low-cost substrate and the thin silicon layer. The properties of the metallurgical barrier must be engineered to implement specific device requirements, such as high back-surface reflectivity. Recent advances in process development are described here.

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1 Introduction

This report covers contract work for the period from October 1988 to July 1990. The Silicon-FilmTM Process is being developed with the objective of achieving a high-performance, low-cost, crystalline silicon solar cell for terrestrial power applications. The approach is being guided by device modeling to achieve a high-performance solar cell structure based on imperfect materials. The specific technical approach involves the deposition of thin silicon layers on a rigid ceramic substrate. The commercial feasibility of this approach has been demonstrated by the recent achievement of a 100-cm², 10.9% commercial-size solar cell. The potential of this approach is further established by the achievement of a 1.0-cm², 15.7% Silicon-FilmTM solar cell.

The development of the Silicon-FilmTM Process has generated a family of three products, as pictured in **Figure 1**. Product I, being developed for production now, utilizes a 100- μ m thick active layer of silicon on a low-cost supporting substrate. There is no barrier layer between the active layer and the substrate, and no light-trapping features are designed in the structure. A recent review of the production development of Product I [1] reported an efficiency range of 6.8% to 10.9% in an initial series of solar cells. In that series, 87% had energy conversion efficiencies greater than 8%, and 48% tested greater than 10%.

Light trapping is incorporated into the Product II design shown in **Figure 1**. Product II differs from Product I by the presence of a metallurgical barrier layer, and by the reduction in thickness of the active silicon layer to 30 μ m. There are performance and cost advantages to using a thin silicon structure as opposed to a thick conventional device. These advantages are 1) improved V_{OC} , 2) reduced dependence on diffusion length (and therefore less stringent material purity and quality requirements), and 3) reduced cost through the use of less silicon. Since long wavelength light (wavelength range 0.9 μ m to 1.1 μ m) is weakly absorbed in crystalline silicon, light trapping must be incorporated into a thin device structure. The design, modeling, and fabrication of the Product II device are reviewed in this work.

Figure 1. *The Silicon-Film™ product families.*

Product III utilizes the Silicon-Film™ process developed for Product II, therefore enjoying the performance and cost benefits of the thin-silicon light-trapping design. The active silicon layer is configured into a monolithically integrated high-voltage structure. This structure allows all electrical contacting to be made on the back of the device, thereby simplifying module assembly. The high-voltage, low-current configurations possible with such a device minimize contact resistance problems and avoid front surface shadowing by current carrying metallic bus bars. The Product III design allows the use of the large ceramic substrates (10 cm x 60 cm)[1] generated by the Silicon-Film™ Process.

1.1 Contract Objectives

The primary objective was to demonstrate that the high-efficiency potential of crystalline silicon can be preserved while using an inexpensive growth process. Specific tasks addressed critical device parameters, such as back-surface recombination velocity, light trapping, and barrier-layer conductivity. Efforts were directed to the study of each of the above device parameters, as well as the fabrication of test structures when appropriate. An efficiency goal of 12% was established for 1.0-cm² cells fabricated with silicon-film layers no greater than 50 μ m thick. Goals for demonstration of spatial uniformity were set as well (10-cm² devices, η =10%). Finally, an investigation into the possibilities of automated interconnection on a single substrate was initiated.

1.2 Summary of the Results

The capability of the Silicon-FilmTM Process was demonstrated with the fabrication of 100-cm² structures. These structures contained a silicon layer that was 100 micrometer thick, and was formed on a ceramic substrate with a metallurgical barrier. Silicon deposition uniformity was demonstrated over 100-cm² areas.

Preferred surface morphology was demonstrated in 50-cm² samples showing excellent grain structure. With a silicon layer thickness of 100 micrometers, grain aspect ratios exceeding 10 have been achieved.

Test structures were fabricated to test certain critical light-trapping design elements. Extensive optical modeling revealed that a metallurgical barrier of low index-of-refraction material (compared with silicon), combined with a textured surface, would result in a reflective barrier with high degrees of light trapping. This model was tested with thin silicon layers deposited on single-crystal silicon substrates with intervening metallurgical barrier layers. High levels of barrier reflection were demonstrated.

A high-voltage, low-current, monolithically interconnected Product III design was established. The capability for the use of large-area ceramic supporting substrates makes the monolithic interconnection scheme viable. The Product III design is shown to be compatible with the Product II process in development.

2 Device Modeling

The effects of light trapping and back-surface passivation are critical to realizing the high-efficiency potential of the thin silicon films. The effects of these variables on overall device efficiency are shown in **Figure 2**. Values of back-surface recombination of 10^6 cm/sec (no passivation) and 10^3 cm/sec (passivated) are used. An analytical model (e.g. [2]) was used for calculation of J_{SC} and J_0 . A one-diode model (diode ideality factor = 1) was used to compute open-circuit voltages. This assumption eliminates any dependence of fill factor on changes in doping and diffusion length. A value of 0.82 for the fill factor was used for all the efficiency calculations in **Figure 2**. A "non-ideal" relationship between doping and minority-carrier lifetime was used to determine the diffusion-length dependence on doping. Lifetime values predicted for single-crystal silicon (values taken from PC-1D [3]) were reduced by a factor of 5 to reflect the non-ideal nature of the Silicon-FilmTM material. This modeling method highlights the limited dependence of the Silicon-FilmTM devices on material quality and minority-carrier diffusion length.

Figure 2 shows that the efficiency of a 35- μ m-thick device with both light trapping and back-surface passivation is superior to that of a conventional device at all doping levels of interest. Peak efficiencies for the thin device are predicted for doping levels in the range of $N_a=2 \times 10^{17}$ cm⁻³ to 5×10^{17} cm⁻³. These doping levels correspond to diffusion lengths in the range of 40 micrometers to 80 micrometers. The efficiencies of the thin devices are predicted to decrease as base doping is decreased (and diffusion length is increased). This is a result of the decrease in V_{SC} that occurs at lower doping levels. The same effect occurs in the conventional device; however, current increases offset the lower V_{OC} values, and efficiency remains constant.

The limited dependence on diffusion length allows the thin device to use higher base doping levels and therefore achieve high V_{OC} . This option is not available to thick conventional devices as long diffusion lengths are required to collect minority carriers generated deep in the base layer. The long diffusion length requirement in conventional devices allows high efficiency to be obtained only with high-quality, relatively expensive silicon wafers.

Model Parameters		S_{BACK}	Optical Path Length
A -	400 μ m Thick Conventional Device	10^6 cm/s	$Z = 1$
B -	35 μ m Thick Conventional Device	10^6 cm/s	$Z = 1$
C -	35 μ m Thick Device with Back Surface Passivation	10^3 cm/s	$Z = 1$
D -	35 μ m Thick Device with Light-trapping	10^6 cm/s	$Z = 20$
E -	35 μ m Thick Device with Light-trapping and Back-Surface Passivation	10^3 cm/s	$Z = 20$

Figure 2. Predicted conversion efficiency (AM1.5G) as a function of base doping. Diffusion lengths are adjusted to be consistent with doping levels.

3 Device Fabrication and Test Results

3.1 Metallurgical Barrier Layer

The metallurgical barrier (MB) layer plays a critical role in the thin-device design. As **Figure 2** shows, recombination at the back surface is critical to the overall device efficiency. This recombination will be influenced by the Silicon-FilmTM/MB interface. An effective light-trapping design also requires that the interface be reflective to confined light. Light-trapping device designs are reviewed in the next section. Additionally, the metallurgical barrier must have the mechanical strength to withstand the silicon deposition process, and it must not be a source for impurities that may have a deleterious effect on device performance.

To passivate the interface, coatings of dielectric material, such as SiO₂, could be used. Other means of limiting recombination include H⁺ passivation and back-surface fields (BSF). Due to the high temperatures involved in the Silicon-FilmTM fabrication process, H⁺ passivation would not be effective. A design using a BSF would require a difference in doping on the order of 10³ between the base and BSF region. Such a difference is not practical since the optimal base doping level is already in the 5x10¹⁷ cm⁻³ range.

To satisfy the above requirements, barrier layers are formed with combinations of materials including dielectric compounds. The barrier layers are deposited in production-type low-cost processes. Present barrier layers have been effective at mechanically protecting the Silicon-FilmTM layer from the ceramic. Aspect ratios (grain height to thickness) greater than 10 have been achieved. A cross section of a Silicon-FilmTM/metallurgical barrier/ceramic structure is shown in **Figure 3**. The Silicon-FilmTM layer is approximately 70 μm thick. The barrier has successfully kept the Silicon-FilmTM layer from interacting with the ceramic below.

The reflectivity of the barrier-coated ceramics was tested. Reflectance is measured from an air/barrier interface. Since the final device requires high reflectivity from a silicon/barrier interface, reflectivity in the final device may be lower than values measured with the test structure. **Figure 4** shows the tested reflectivity of the bare ceramic and of the ceramic coated

with barrier material. The high level of reflectivity results from the material quality of the barrier and random nature of the interfaces involved.

Figure 3. *Cross section of a Silicon-FilmTM/metallurgical barrier/textured ceramic substrate structure.*

Figure 4. *Measured reflectivity of bare ceramic and ceramic coated with metallurgical-barrier material.*

3.2 Light-Trapping Properties and Test Structures

The back surface of the active Silicon-FilmTM layer must be reflective to internally confined light to effectively light trap. In conventional thick devices, this high reflectivity can be obtained by the application of metallic layers on the back surface. The high temperatures involved in the processing of the Silicon-FilmTM solar cells do not readily accommodate the use of metallic reflectors. The second requirement on the back surface is that it be a low-recombination interface. Such interfaces can be obtained by a silicon/dielectric interface. One approach satisfying both requirements is based on material properties alone, and was discussed in the previous section (Figure 4). A second method, discussed here, utilizes intentional texturing and dielectric-barrier materials.

A back-surface textured structure was modeled that will generate high levels of light trapping with only the use of a back-surface dielectric coating [4]. A schematic of the modeled device is shown in Figure 5. Such a device can be made to rely solely on total internal

reflection (on both front and back surfaces) to achieve long optical path lengths. It was shown that an efficient light-trapping structure can be formed using a back surface textured with slats of angles of 23° to 40° to the horizontal. The index of refraction of the metallurgical barrier must be significantly different from that of silicon to insure total internal reflection.

Texturing Period, $2W$

Average Active Layer Thickness, H

Texturing Angle, Φ

Figure 5. *Schematic of the device structure used in modeling light-trapping properties.*

An example of the ray-tracing analysis used is shown in **Figure 6**. Textured slats were modeled (on the back surface in this example) allowing a two-dimensional analysis to be used. All textured features were large relative to the wavelength of the light in question, allowing the use of geometric optics.

If transparent materials are used in the barrier layer, interference effects need to be accounted for. **Figure 7** shows the results of the analysis for back-surface textured samples with varying thicknesses of SiO_2 as the metallurgical barrier. The substrate was modeled to be single-crystal silicon. No initial front-surface reflection losses were modeled. The collection efficiency of photogenerated carriers was assumed to be unity.

Similar analyses were performed for front-surface textured devices, as well as devices with single-layer and double-layer anti-reflection coatings. Randomly textured surfaces were modeled as well. Reflected light from a randomly textured surface was assumed to follow a Lambertian distribution. The use of transparent dielectric coatings and randomly textured surfaces results in high levels of light being transmitted through the barrier. Total internal reflection cannot be engineered to occur at each back-surface interaction. A summary of the results for front- and back-surface texturing, as well as random texturing, is shown in **Figure 8**. All devices in **Figure 8** are modeled with a SiO_2 back-surface coating and a double-layer anti-reflection coating.

Figure 6. *Example of ray tracing for back-surface slat angles of 35° indicating back-surface interference effects.*

Figure 7. Effects of back-surface texturing on predicted J_{SC} (AM1.5) for different thicknesses of SiO_2 back-surface coatings.

Experimental test structures were formed with (110) single-crystal silicon wafers. Anisotropic etches were used to reveal the slow etching (111) planes, which are 35° to the wafer surface. The resulting textured slat configuration is near optimal for back surface texturing. The texture etched surfaces of a (100) wafer and a (110) wafer are shown in Figure 9. The (100) wafer has slats that are 54° off the horizontal, while the (110) wafer features are 35° from the horizontal. Referring to Figures 7 and 8, the 35° slat angle will give near-optimal light-trapping properties.

The light-trapping properties of (110) silicon were demonstrated with absorption measurements. Test structures were made from 100-micrometer-thick wafers, with double-layer anti-reflection coatings applied front and back. The results of the absorption testing are shown in Figure 10. Experimental and theoretical data are presented for both polished and textured surfaces. In both cases the experimental data agrees well with the ray-tracing based computer simulation. The textured surface increases the absorption of 1000-nanometer light from 60% (polished surface) to 95% (textured surface). An equivalent optical thickness of approximately 700 micrometers (7 times the physical thickness, $Z=7$) is indicated.

Figure 8. Comparison of the effects of back (BST), front (FST), and random surface texturing. All devices were modeled with double-layer antireflection coating and 0.1-micrometer thick SiO₂ coatings.

Silicon-Film™ layers 30 micrometers thick were deposited on the textured wafers shown in **Figure 9(b)**. Intervening layers of SiO₂ were used as a metallurgical barrier. The resulting devices revealed enhanced absorption and carrier collection at the long wavelengths. Cross sections of devices fabricated with planar- and textured-back surfaces are shown in **Figure 11**. Openings have been made in the barrier layer to allow for electrical contact to the substrate. The non-textured sample was selectively etched to highlight the SiO₂ barrier layer.

Photovoltaic devices were fabricated on the material shown in **Figure 11**. Conventional processing included phosphorus diffusion, Ti-Pd-Ag emitter contacts, evaporated-Al back contact, and plasma isolation to 1.0 cm² areas. A ZnS/MgF double-layer anti-reflection coating was applied to the best samples. A summary of the I-V characteristics is shown in **Table I**.

Figure 9. *Texture etched surfaces of (a) 100 wafer, and (b) 110 wafer coatings.*

Figure 10. *Experimental measurements of absorption for 100 micrometer thick (110) wafers with and without a texture etched surface. Good agreement with theory is shown. A $Z=7$ is indicated in the enhanced long wavelength absorption of the texture etched wafer.*

The short-circuit current of the (110) slat textured samples was superior to both random and planar samples. This increase in current can be attributed to the enhanced light-trapping properties of the textured surface. The interpretation of the light-trapping characteristics is difficult due to the via openings in the barrier layers. In the via regions, long wavelength light is absorbed in the substrate; the resulting minority carrier can either recombine or diffuse to the emitter and be collected. Comparisons of planar and textured samples are still valid, as both contain approximately equal percentages of via areas. The low-minority carrier diffusion length of the deposited film (as discussed below) has lowered the overall conversion efficiencies of the devices to less than 10%.

Figure 11. Cross section for a 30 micrometer thick silicon film deposited on (a) a textured (110) wafer, and (b) a planar wafer.

Table I. Summary of the best thin film devices fabricated on single-crystal substrates.

	V_{oc} mV	J_{sc} mA/cm ²	FF	R_s Ω	Eff
#31-3 Planar Back Surface	523	21.7	.69	0.7	7.8
#30-2 Random Back Surface Texture	533	22.3	.63	0.9	7.5
#33-1 (110) Back Surface Texture	513	26.2	.70	1.7	9.4

Analysis of the best devices reveals the parameters shown in Table II. The minority-carrier diffusion length (L) was calculated by analysis of the $1/\alpha$ vs. $1/QE$ data (where α is the absorption coefficient of silicon, and QE is the internal quantum efficiency). The resulting data reveals two linear regions. One region is associated with light absorbed primarily on the first pass through the device ($1/\alpha < 20$ micrometers). The minority-carrier diffusion length derived from this region is associated with the material quality of the deposited layer. The second linear region for long wavelength measurements ($1/\alpha > 100$ micrometers) is attributed to light-trapping properties. Table II shows that the long wavelength measurement (L_{eff}) is approximately three times longer for the textured versus the planar samples. A relatively high level of barrier reflection is indicated. The presence of vias, and their contribution to the long wavelength photoresponse, complicates more detailed analysis of the light-trapping characteristics.

Table II. *Summary of calculated device parameters.*

	J_0 (pA/cm ²)	L_{EFF} short λ	N_2 (cm ⁻³)	L_{EFF} long λ
31-3 Planar	29	9.5 μ m	2.5e16	12.6 μ m
30-2 Poly Tex	20	7.1 μ m	4.4e16	19.6 μ m
33-1 (110) Tex	54	9.7 μ m	1.4e16	33.8 μ m

3.3 Optical Measurements on Product II Structures

The light-trapping work discussed in the previous section can be applied to the Product II structure. As the ceramic substrate used in Product II is fabricated "in-house" for this single purpose, custom surfaces can be engineered. **Figure 12** shows a cross section of a ceramic that was fabricated for enhanced light trapping. This textured surface was fabricated with the use of a custom mold. The angle of the slat texturing was chosen to be approximately 30° in order to maximize back-surface reflection and light-trapping effects.

Figure 12. *A cross section of a ceramic wafer with a textured surface designed for light trapping.*

Standard ceramic processing (without custom molds) generates a randomly textured Silicon-FilmTM/ceramic interface. This random texture was investigated in full Product II structures. Reflectance measurements made on a 100-cm² Silicon-FilmTM/metallurgical barrier/ceramic structure is shown in **Figure 13**. The data reveals a higher sub-bandgap reflection than expected for a bare silicon surface. This enhanced reflection is due to light being initially coupled into the Silicon-FilmTM layer, then later escaping from the front surface on subsequent

internal reflections. The exact value of the barrier reflection cannot be determined, as the reflectivity of both the front and back surfaces to internally confined light are unknown. Assumptions regarding the reflectivity of the front surface can be made. For the data shown in **Figure 13** the internal reflectivity of the front surface cannot be less than approximately 29% due to reasons of symmetry. A maximum value can be estimated to be the reflection exhibited by a Lambertian distribution of internally confined light. Such a reflectivity would be 92% [5]. Using those limits for the internal front-surface reflectivity, a range of values for the back-surface reflectivity can be calculated [3]. For the sample data in **Figure 13**, the back-surface reflectivity would be between 20% and 65%. This level of reflectivity from a silicon/dielectric barrier/ceramic interface indicates a high degree of random texturing at the ceramic surface.

Figure 13. Reflectance of a full PII Silicon-Film™/metallurgical barrier/textured ceramic device.

3.4 I-V Device Results on Laboratory-Scale Devices

Photovoltaic device measurements were extensively utilized as feedback to the material fabrication effort. A one-day processing sequence was implemented to provide small-area (0.10 cm²) solar cell fabrication and testing in an 8-hour day. The process sequence for this "mesa" process is shown in Table III.

Table III. *Process sequence for small-area devices.*

Surface Etch	30 sec chemical polish etch (HNO ₃ /HF/CH ₃ COOH; 15:2:5)
Pre-Diffusion Clean	H ₂ SO ₄ /H ₂ O ₂ ; 1:1 @ 110°C HF strip, DI Rinse H ₂ O/H ₂ O ₂ /HCL; 1:1 @ 90-100°C HF strip, DI Rinse
Diffusion	PH ₃ source 850°C, 15 minutes resulting R _{sheet} = 45-60 Ω/square
Apply Isolation Mask	Hot Wax
Isolation Etch	90 sec chemical polish 5 minute DI H ₂ O rinse
Remove Mask	Organic solvents
Back Contact	Al/Ag paste, 880 °C, 60 seconds

All processing was preceded by a surface etch. The etch step eliminates the effects of surface oxides or impurities. Although useful for insuring repeatable device results, the surface etch was not a required step. Non-surface etched samples of Silicon-Film™ on ceramic generated device results comparable to surface-etched controls. A relatively heavy diffusion sequence is utilized to allow the emitter surface to be probed by bare metal probes. This eliminates the need for front contact metals and further simplifies the process sequence. A wax

is used to define the mesa size and mask the isolation etch. Small circles of wax are formed on the emitter surface, approximately 0.4 cm in diameter. Approximately 5 mesas were formed on each sample. The isolation etch removes the n-type emitter from all areas of the device except those protected by the wax. The final step is the application of an Al-Ag paste. Samples are fired in an open-air belt furnace.

Testing of mesa samples included light and dark I-V, capacitance (for measurement of resistivity), and spectral response. For the daily processing sequence, all samples were light I-V tested, and a representative sample tested for spectral response. The minority-carrier diffusion length was extracted from the quantum efficiency data. The internal quantum efficiency was calculated using reflection measurements previously obtained on smaller material, thereby eliminating the need to measure reflection on every sample.

The small-area "mesa" processing sequence was capable of generating significant device results on 1 to 10 samples per day. This provided timely feedback to the material fabricating team. Analysis of the mesa process data was utilized to resolve ceramic compatibility and gross impurity problems, and to assist in the evaluation of metallurgical-barrier candidate materials. A thermally compatible ceramic was developed that remained flat after Silicon-Film™ layer formation. A metallurgical barrier was developed after many candidates were evaluated and ruled out. The majority of candidates failed due to a high level of interaction with the silicon layer, resulting in gross impurity problems and poor device results. After significant experimentation, a ceramic/barrier system was developed that met all the design criteria.

With a substrate well developed, focus shifted to optimizing the Silicon-Film™ growth process. Relatively low minority-carrier diffusion lengths were measured throughout the ceramic/barrier evolution, typically in the range of 3 to 9 μm . This was attributed to the limitations of the small-grain material being deposited (grain size of 50 to 100 μm).

The recombination characteristics of the back surface are an important element in obtaining high efficiency in a thin, light-trapping silicon-film device. It was anticipated that device analysis would include a detailed investigation of the back-surface recombination properties through analysis of solar cell data and special test structure fabrication. As the minority-carrier diffusion length has remained much smaller than the device thickness, a detailed investigation of the back-surface recombination characteristics has not been possible.

As the Silicon-Film™ growth process was improved, grain sizes and aspect ratios increased. Presently, grain sizes are on the order of millimeters and aspect ratios (the grain size over the layer thickness) exceed 10. Device performance on the large grain material is modest at present, with diffusion lengths rarely exceeding 10 μm . The best device parameters measured on a 0.1-cm² device are as follows:

$$\begin{array}{lll} V_{OC} & = & 525 \text{ mV} \\ J_{SC} & = & 20.7 \text{ mA/cm}^2 \\ FF & = & 0.66 \end{array}$$

As the grain size exceeds the measured diffusion length in the latest material, poor minority-carrier properties are no longer attributed to the small grain size. Sources of intra-grain defects are presently being investigated. These include:

1. Thermal stress introduced during the growth process.
2. Impurity contamination from the ceramic, the barrier, or the Si-Film deposition process.

4 Designs for Monolithically Interconnected Devices

An initial analysis was undertaken to identify ways in which solar cells fabricated using the Silicon-Film™ approach can be connected in series on a single substrate, using a potentially low-cost process. The analysis indicates that a monolithically integrated polycrystalline silicon solar cell can significantly reduce module costs by a factor of 2 through decreased device and assembly costs.

The present technology of silicon module assembly involves wiring together 36 individual elements (i.e., solar cells). The proposed work will lead to the reduction of assembly costs in two areas: first, there will be fewer elements, each one being larger and more efficient; and second, all contacting will be limited to the backs (or edges) of each element. The length of these elements will coincide with one dimension of the module, therefore limiting device contacts to two edges of the module. The contacting of the illuminated side of the device during module assembly will be completely eliminated from the new design. Module assembly will be reduced to contacting the backs (or edges) of 9 or fewer elements.

The Silicon-Film™ Process presently under development will be utilized in the fabrication of the monolithically integrated Product III. With the exception of the isolating and contacting step, the process sequence is the same for Products II device already under development.

A key feature of this new module design is the ability to isolate areas of the element (i.e., Silicon-Film™ solar cells) into segments. A device schematic is pictures in Figure 14. Isolation is possible because the active device is only 20 to 50 microns thick and is supported by an insulating substrate. A contacting scheme has been developed to retrieve the generated power in any I-V configuration. All inter-segment or inter-cell electrical contacts are made on the top of the device. All interconnections to the module will be made on the edges or backs of the elements. The metallization trenches can be formed by etching, laser scribing, or dicing. The interconnect metal can be applied by a screen printing method or by electroplating. Electrically, the submodule pictured represents 36 diodes in series. This interconnection occurs on a rigid

ceramic substrate (i.e., monolithically). The module in **Figure 14** is formed from 8 individual elements. The contacting metal can be wrapped around to the back of the insulating ceramic for back contact.

Figure 14. *Silicon-Film™ Product III device structure.*

The V_{OC} of a module is determined by the number of cells on a submodule. The J_{SC} of a module is determined by the area of the cell and the number of submodules. Each of the elements is wired in parallel in the module requiring only electrical connections along the sides of the module.

A schematic of a Product III module configuration is shown in **Figure 15**. The example shown was configured to deliver I-V characteristics similar to the existing industry standard module. The isolation and contact scheme, however, allows for virtually any configuration that may be required. If a higher voltage, lower current configuration is required, the number of cells per submodule can be increased. This can be done without affecting the process by which the Silicon-Film™ wafer is fabricated; all that needs to be altered is the isolation and metallization steps.

Figure 15. Silicon-Film™ Product III module, submodule, and element.

5 Conclusion

The Silicon-Film™ process is being developed with the objective of achieving a high-performance, low-cost solar cell for terrestrial power applications. Modeling of 35- μm thick Silicon-Film™ devices with both light-trapping and back-surface passivation is presented. Unlike conventional devices, thin devices have only a limited dependence on minority-carrier diffusion length. Modeling results show that the thin devices are capable of higher efficiency than conventional devices at all doping levels of interest.

Device development work has focused on the role of the metallurgical barrier, providing a mechanical barrier between the active Silicon-Film™ layer and the low-cost ceramic, as well as high reflectivity for light trapping. Barrier layers have been developed that allow the growth of Silicon-Film™ layers less than 100 micrometers thick on ceramic substrates with grain aspect ratios of over 10.

A light-trapping device design was developed that will allow the use of dielectric materials as the back-surface coating. A Silicon-Film™/dielectric interface is required to insure low recombination at the back surface of the device. By texturing the back surface, high reflectivity through total internal reflection can be achieved. Test structures formed on single-crystal silicon have shown enhanced long-wavelength absorption. Silicon-Film™/dielectric barrier/ceramic (PII) structures have shown significant levels of back-surface reflectivity.

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