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U. S. DEPARTMENT OF COMMERCE
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
FINAL REPORT for U.S. DEPARTMENT OF ENERGY
INTERAGENCY AGREEMENT NUMBER DE-AI05-91ER40616

Data Acquisition Systems

Sponsored by Department of Energy Division of High Energy Physics

Work on this project is continuing under Interagency Agreement Number DE-AI02-93ER40778.A0001.

1. Objective

Development and maintenance of fast and flexible modular data acquisition and control systems by the NIM Committee to meet the needs of the high energy physics community.

2. Program

The program has included continued extension and maintenance of the specifications for data acquisition systems for high energy physics applications. Work continued on the study, development and specification of the FASTBUS system and of other systems to meet the changing needs of the community. The approach has maximized the use of available, technology, systems, subsystems, and components. Work on a version of FASTBUS optimized for accelerator and experiment control applications, and interfaces to other busses has been examined to see to what extent existing systems can be utilized. Processing of the revised editions the ANSI/IEEE standards was be pursued so that they can be published in 1994. This applies also to the corresponding international standards of the International Electrotechnical Commission (IEC) though the international processing is expected to take somewhat longer. The project provides a clearing house for data acquisition system information and maintains liaison with and collaborates with the ESONE Committee of European Laboratories and national and international laboratories involved with data acquisition and control systems for high energy and nuclear physics.

3. Description of System

The FASTBUS design is based on a 32-bit modular system of autonomous segments that can communicate with each other as well as with a central computer. This provision for simultaneous parallel processing makes for flexible system architecture, a fast

pre-processing capability and a very high system throughput capability. To optimize data transfer band-width without excessive bus lines, address and data lines are multiplexed. This makes a full 32 bits available for address in the address mode and for data in the data mode.

The devices are of three basic types; slaves, masters and interconnects. Masters are capable of controlling the segment in which they reside or of the entire system or bus. A high speed priority arbitration scheme is therefore provided to make efficient allocation of bus segment mastership. Other features include high speed block transfers and broadcast commands for simultaneous access to either the entire system or selective parts of the system. The devices are designed so that they can be connected to a cable segment or to a "backplane" (or crate) segment that is part of a crate that houses a multiplicity of devices. The modules that can be accommodated in the crate come in single-unit or multiple-unit widths.

Particular attention has been paid to flexible addressing to attain large device and segment addressing capability. Block transfers in both handshake and non-handshake modes are accommodated. Ground rules are spelled out for the segment interconnects (SIs) while permitting considerable leeway for the system designer. The hardware design has taken into account software considerations and has proceeded with the active participation of software specialists.

4. Progress

Draft revisions of the FASTBUS hardware and software standards, ANSI/IEEE Std 960 and ANSI/IEEE Std 1177, were prepared and reviewed. They are currently being processed and it is anticipated that they will be published in 1994. Similarly, a corresponding revision of the international FASTBUS publication IEC 935 of the International Electrotechnical Commission is underway. Requests were filled for FASTBUS information and documents. Work has continued on a monolithic chip for cable segment transceivers though difficulties have been encountered in dealing with chip manufacturers where the potential market for the chips is not immense. More fruitful has been the development of hybrid receivers that maintain compatibility with existing implementations. Protocol chips for FASTBUS Slaves have also been developed. The mechanical design of a version of FASTBUS optimized for accelerator and experiment control has progressed though it is intended to examine the extent to which existing systems and components can be utilized.

5. Recent Publications

Numerous papers regarding FASTBUS or systems utilizing FASTBUS have been published in the Conference Record of the 1992

IEEE Nuclear Science Symposium, October 25-31, 1992 and in the IEEE Transactions on Nuclear Science. Additional FASTBUS and related papers were presented at the 1993 IEEE Conference on Real-Time Computer Applications in Nuclear, Particle and Plasma Physics, June 8-11, and at the 1993 IEEE Nuclear Science Symposium, November 1-5. These papers will also be published in IEEE Conference Records and some in the IEEE Transactions on Nuclear Science.

6. Honors

The Principal Investigator, Louis Costrell of the National Institute of Standards and Technology, was honored as the recipient of the 1993 Computer Application in Nuclear and Plasma Sciences Award. This award of the Nuclear and Plasma Sciences Society of the Institute of Electrical and Electronics Engineers reads:

In appreciation for his many years of leadership in the creation, implementation and use of standards in data acquisition and control systems

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