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INSTRUMENTS

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**TRANSISTORIZATION OF NUCLEAR COUNTING
CIRCUITS**

By
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TRANSISTORIZATION OF NUCLEAR COUNTING CIRCUITS

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R. T. Graveson
H. SadowskiABSTRACT

The advantages of long operational life, low power drain and miniaturization may be realized in nuclear counting circuits through the use of transistors. The disadvantage of instability, due to the effects of temperature change in the transistor, may be minimized in counting circuit designs. The predominant effects are a change in the grounded emitter current gain (Beta) and a variation of the leakage current through the transistor (I_{co}). The binary circuit is analyzed for stability criteria, and may be tested conveniently through a simulation of I_{co} for the maximum operating temperature.

Representative circuits of a binary stage, amplitude discriminator, one shot multivibrator, and ratemeters are included. These were designed using the criteria of a minimum Beta and a maximum I_{co} .

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Introduction

Nuclear counting circuits are used to record the rate of arrival of ionizing events in a detector. For this purpose a scaler or a count rate-meter may be used. Scaling refers to the storage of each event in a circuit to determine the number of events during a measured time interval. A rate-meter system uses an integrating circuit to develop a voltage which is proportional to the count rate. The advantage of the scaling system is stability, since each event is recorded in stages which primarily have two states, "on" or "off". The ratemeter system has the advantage of simplicity, and for this reason is commonly used for portable equipment.

Many of the advantages of the transistor are applicable to these counting systems. Long life, low voltage power supplies and the absence of filament power simplify design and maintenance. Miniaturization by printed circuit techniques, and again the absence of filament supplies, are particularly useful when designing portable equipment.

The transistor must be viewed as an active or amplifying element, whose characteristics are temperature dependent. The major effects of temperature, from the viewpoint of the designer, appear as the change in Beta (the grounded emitter current gain) and the variation of the leakage current. The gain change is relatively small. However the leakage current component varies over several orders of magnitude for the temperature extremes normally encountered. The circuits described herein have been designed from equations which include the effects of temperature on the transistor in order that their operation can be predicted over the desired temperature range.

Binary Design

The binary stage is a basic unit of the scaler. However, the stability criteria developed for this type of circuit are applicable to the one shot multivibrator circuits used for ratemeters. Figure 1a shows a basic binary circuit in which one side, and only one side, may be "on" at any given time. One may determine the negative resistance characteristic of this system analytically as well as experimentally. The loop is opened at some convenient point, such as the collector of one transistor. This point and ground become two terminals of a "black box" for which the input current as a function of applied voltage can be determined. See figure 1b.

In the analysis to follow, the transistors are assumed to be ideal switches, that is short circuits when "on" and open circuits when "off". However, to account for the effects of collector cut-off current, a constant current generator equal to the collector current with the emitter circuit open (I_{co}) is connected between collector and base of each transistor as in figure 1b.⁽¹⁾ This represents the temperature dependent part of cut-off current. Normally each I_{co} generator has a small conductance across it which allows an additional current to leak out of the base. This component varies as the collector to base voltage, but since the leakage conductance is small, the effect is slight for voltages well below collector breakdown. Hence, this leakage conductance is neglected. Furthermore, the base input resistance of each transistor is assumed to be so low that the base to emitter voltage drop developed across it is considered negligible at all times. This effectively puts the base at ground potential, which means that the external base resistor R_b can be neglected for the purposes of this analysis.

(1) Lo, Enders, Zawels, Waldhauer and Cheng, "Transistor Electronics", pp 137-140

Fig. 1 (a) basic binary circuit
 (b) Circuit used for analysis
 (c) Idealized negative resistance characteristic

In one of the stable regions, T_1 is "on" and acts as a low impedance across the input terminals resulting in an effective short circuit at the input. This can be approximated by the equation:

$$E_1 = 0 \quad (1)$$

In the transition region the operation is described by the following equations:

Considering Node 1 in figure 1b,

$$I_1 = I_{o1} + I_{b2} \quad (2)$$

$$I_{o1} = B_1(I_{b1} + I_{oo1}) + I_{co1} \quad (3)$$

$$E_1 = I_{b2} R_o \quad (4)$$

Considering Node 2

$$I_2 = I_{o2} + I_{b1} \quad (5)$$

$$I_{o2} = B_2(I_{b2} + I_{oo2}) + I_{co2} \quad (6)$$

$$E_{oo} = I_2 R_L + I_{b1} R_o \quad (7)$$

Rearranging and substituting reduces equations (2) through (7) to the describing equation:

$$I_1 = \left[1 - \frac{B_1 B_2 R_L}{R_L + R_o} \right] \frac{E_1}{R_o} + \frac{B_1 R_L}{R_L + R_o} \left[\frac{E_{oo}}{R_L} - I_{oo2}(1 + B_2) \right] + I_{co1}(1 + B_1) \quad (8)$$

Finally, the other stable region, which occurs with T_1 "off" and T_2 "on", is defined by:

$$I_1 = \frac{E_1}{R_o} + I_{co1}(1 + B_1) \quad (9)$$

The negative resistance region is bounded by the inflection points, E_A , I_A and E_B , I_B . The intersection of the curves defined by equations (1) and (8) determines the point E_A , I_A as

$$E_A = 0$$

$$I_A = \frac{B_1 R_L}{R_L + R_o} \left[\frac{E_{oo}}{R_L} - I_{oo2}(1 + B_2) \right] + I_{co1}(1 + B_1) \quad (10)$$

while the common point defined by equations (8) and (9) is

$$\begin{aligned} E_B &= \frac{R_o E_{cc}}{B_2 R_L} - \frac{R_o}{B_2} I_{co2}(1 + B_2) \\ I_B &= \frac{E_{cc}}{B_2 R_L} - \frac{I_{co2}(1 + B_2)}{B_2} + I_{co1}(1 + B_1) \end{aligned} \quad (11)$$

For bistable operation the load line must intersect the negative resistance plot in three points as shown in Figure 1c, resulting in two stable operating points, E_k, I_k and E_L, I_L separated by a transition region. This requires the slope of the load line to be less than that of the negative resistance characteristic which is expressed as:

$$-\frac{1}{R_L} < \frac{1 - \frac{B_1 B_2 R_L}{R_L + R_o}}{R_o}$$

which leads to the requirement that

$$B_1 B_2 > \left[\frac{R_L + R_o}{R_L} \right]^2 \quad (12)$$

The two stable points are given by

$$E_k = 0 \quad I_k = \frac{E_{cc}}{R_L} \quad (13)$$

and

$$\begin{aligned} E_L &= \frac{R_o E_{cc}}{R_o + R_L} - \frac{R_o R_L}{R_o + R_L} I_{co1}(1 + B_1) \\ I_L &= \frac{E_{cc}}{R_o + R_L} + \frac{R_o}{R_o + R_L} I_{co1}(1 + B_1) \end{aligned} \quad (14)$$

Hence, the criteria for bistable operation can also be expressed as

$$E_L > E_B : I_k < I_A \quad (15)$$

if the external loading of this circuit is considered to exist from a collector to ground as indicated by R_o in Figure 1b the load line is modified as shown in Figure 1c. The current axis intercept remains unchanged since the short circuit current is still $\frac{E_{cc}}{R_L}$, but the slope is modified to $\frac{R_L R_o}{R_L + R_o}$

because of the parallel loading effect. The minimum value of R_o (maximum loading) for bistable operation is one that causes the load line to pass through the point B. At that point the maximum available external load current is

$$\frac{E_B}{R_o} = I_{\max} = \frac{E_{oc} - E_B}{R_L} - \frac{E_B}{R_o} - I_{co_1}(1 + B_1) \quad (16)$$

If the transistors are chosen so that $B_1 = B_2$ and I_{co_1} and I_{co_2} are negligible at the highest temperature encountered, the above relations reduce to the following; (2)

Stable Region with T_1 "on"

$$E_1 = 0 \quad (1a)$$

Transition Region

$$I_1 = \left[1 - \frac{B^2 R_L}{R_L + R_o} \right] \frac{E_1}{R_o} + \frac{B E_{oc}}{R_L + R_o} \quad (8a)$$

The other stable region with T_1 "off"

$$I_1 = \frac{E_1}{R_o} \quad (9a)$$

Inflection points

$$E_A = 0 ; I_A = \frac{B E_{oc}}{R_o + R_L} \quad (10a)$$

$$E_B = \frac{R_o E_{oc}}{B R_L} ; I_B = \frac{E_{oc}}{B R_L} \quad (11a)$$

Bistable operation criteria

$$B > \frac{R_L + R_o}{R_L} \quad (12a)$$

The two stable quiescent points

$$E_K = 0 ; I_K = \frac{E_{oc}}{R_L} \quad (13a)$$

$$E_L = \frac{R_o E_{oc}}{R_o + R_L} ; I_L = \frac{E_{oc}}{R_o + R_L} \quad (14a)$$

The maximum load current is

$$I_{\max} = \frac{E_{oc} - E_B}{R_L} - \frac{E_B}{R_o} \quad (16a)$$

(2) T.P. Bothwell, "Junction Transistor Flip-Flop Design Methods for Computer Applications", A.I.E.E., Winter General Meeting, New York, Feb. 1955.

It is convenient to physically remove the collector load and supply voltage from one transistor as in Figure 2a. The voltage applied to these terminals may be used to provide horizontal deflection (proportional to collector voltage) on an oscilloscope, while the current into this "black box", measured as a voltage across a small resistor in series with the terminals, provides the vertical deflection (proportional to collector current) on the same oscilloscope. An ordinary oscilloscope having a D.C. input can be used in conjunction with a camera to obtain a picture of the trace if the applied voltage is say 60 cycles A.C. However, we have found it particularly convenient to use a memory oscilloscope and vary the applied voltage manually to obtain this negative resistance plot.

After having obtained the negative resistance characteristic, the load line trace may be superimposed by connecting the oscilloscope to display collector current and voltage of the opposite transistor as indicated in Figure 2a. The horizontal and vertical deflection sensitivities are maintained for both plots in order to make the scales compatible. This requires accurately matched resistors across which the current indication is taken.

The effect of temperature in a transistor appears mainly as a change in Beta and as an increase in the cut-off current (I_{co}). For most transistors over a region from 0° to 55° C, the Beta change is approximately 20%. This change must not reduce the total current gain below that required by equation (12) or (12a). The cut-off current, I_{co} , approximately doubles for each 10° C temperature increase, and appears in the base circuit. Thus, it is amplified and appears as a shift in operating point in the collector circuit. The doubling 'rule of thumb' allows the designer to estimate the I_{co} value for the maximum operating temperature from the value measured at room temperature. Since it appears in the base collector circuit, it may be simulated by a

- A -

- B -

Fig. 2 (a) Circuit used to plot negative resistance characteristic and load line

(b) Method of simulating the increase in I_{co} at high temperature

constant current source as shown in Figure 2b. One need only calculate the value of I_{co} at the highest operating temperature, using the above rule of thumb; subtract from this the value of I_{co} at room temperature to obtain the increment in cut-off current, I_{co} , which must be supplied from the constant current source in order that operating conditions at the high temperature be simulated.

The effect of this increase in I_{co} on the negative resistance characteristic of the binary shown in Figure 3a. Figure 3b shows the effect of variations in Beta.

The binary stage illustrated in Figure 4 has been designed for a minimum Beta of 20. The load line slope has been selected to be $1/2$ the negative resistance slope for this minimum Beta condition.

Pulse Steering in Cascaded Binary Stages

Pulse steering insures the proper coupling between cascaded binary stages. Only the alternate pulses are transferred to the following stage. The circuit in Figure 3 has illustrated the output from the binary stage before and after differentiation. The following stage must be connected to "fire" on a unidirectional pulse. It must also reject the alternate, opposite polarity, pulses. The scheme illustrated uses the collector swing to bias "on" one diode and to "back" bias the alternate diode. A negative input pulse is not transmitted through the "back" bias diode, but is coupled through the "on" bias unit to the "off" transistor, turning it "on". This circuit will operate at better than 100 KC over a temperature range from 0° to 50° C. Transistors were selected from among the medium frequency types to obtain the advantages of low price.

Discriminator Trigger

Figure 5a shows the output pulses from typical nuclear detector presented as a function of time. The discriminator circuit in Figure 5b rejects

Fig. 3 (a) Variation of negative resistance characteristic using Raytheon 2N63 transistors as I_{co} changes with temperature.
(b) Variation of characteristic as β changes

TRANSISTORS TESTED
RCA 2N139, 2N140
RAYTHEON 2N63, 2N64

Fig. 4 - Completed transistor binary stage.

all pulses below its preset level. When coupled to the trigger circuit, a one shot multivibrator, it gives an output of constant amplitude and width for each pulse which exceeds the preset input level. The transistor in this stage is back biased to an off condition and no output occurs until the pulse at the input causes the voltage at the base to exceed the back bias on the emitter. Since no emitter current flows normally, there is no amplification of the temperature dependent base current, I_{co} , in the emitter circuit. However, the I_{co} that does flow through the base, creates a voltage drop across R_1 that tends to reduce the back bias, hence the discriminating level. Once the acceptable limits of variation at a given discrimination level are decided upon, the input resistor R_1 can be chosen low enough so that its I_R drop variation, for a given temperature range, is within these limits. From 0° to 55° C, this particular discriminator shows less than 80 millivolt variation in discriminator level.

The one shot multivibrator, Figure 5c, is derived from the basic binary stage by removing one of the coupling resistors. Thus, the circuit has a transient two point stability, but only one steady state stable condition. The pulse width is controlled by condenser C. The trigger circuit illustrated will develop a $1\frac{1}{4}$ microsecond output pulse of 10 volts amplitude and is stable from 0 to 55° C.

Ratemeter Circuits

The trigger circuit described is used to drive the input binary stage in a scaler. It also may be used with an integrating circuit, to measure the rate of arrival of pulses directly. Since the pulse out of the trigger has constant amplitude and width, it will contain a constant amount of charge. A Zener diode has been added in Figure 6 to clip the amplitude of this pulse which effectively removes any dependence on the supply voltage. This pulse

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-A-

-B-

-C-

Fig. 5 (a) Typical waveform from nuclear detector
(b) Discriminator circuit and typical output waveform
(c) Univibrator or trigger circuit and typical output waveform

Fig. 6 - Ratemeter Circuit

is current amplified in an emitter follower circuit to provide power gain and then integrated in an RC section. The voltage developed across the condenser is given by the equation: $e_o = E_n RC$. (3)

Figure 7 shows a form of the ratemeter circuit which is particularly suited to portable equipment. A complementary pair of transistors (PNP-NPN) is used to form the trigger stage. Both are normally off except during the "flipped" condition. The output is clipped by a Zener diode to remove dependence on the supply voltage, and in this case the output is stable to within 2%, as the supply voltage is varied from 6 to 4 volts. The resulting pulse is integrated in the collector circuit of the following amplifier. The feedback resistor, R_f , controls the gain of this stage and may be used as a calibration control. The basic calibration depends on the coupling capacitor in the trigger, and thus the pulse width. A current is inserted through R_z to buck out the collector zero signal current. The total drain of this unit is less than one milliamperere. When used in portable equipment, considerable saving in battery size and weight can be realized.

Summary

The criteria of minimum beta and maximum I_{co} have been used in the equations to design the circuits. The temperature range has been assumed to be from 0 to 50° C since this fulfills all laboratory and most field requirements. The transistor gain is always assumed at a value well below the minimum encountered throughout the temperature range and as well below that encountered in the usual production run of a specified transistor type. Thus the selection of transistors during production is not required. Also in the above circuits relatively inexpensive easily available transistor types have been used, to minimize the cost of the completed units.

(3) Elmore & Sands, "Electronics", pp 250-253, McGraw-Hill

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