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Author(s): G. J. Arnone and C. L. Hollas

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Data Acquisition System Developed for the Resonance Absorption Project*

G. J. Arnone and C. L. Hollas
Los Alamos National Laboratory, Los Alamos, New Mexico 87545

Abstract

Minimizing signal errors and losses in high-rate gamma-ray imaging systems places demands on the signal-processing and data acquisition electronics. We will describe the data acquisition system developed for the resonance absorption project and techniques used to minimize dead-time and data losses. The data acquisition system acquires pulse-height spectra from an array of gamma-ray detectors and is made available to multiple processors by using the VMEbus standard to provide concurrent data analysis. A SUN workstation is used to develop the application software and also provides the user interface. We have developed a pulse-height-analysis board that has been optimized for low dead time. By incorporating an independent, high-speed signal channel for each detector, we are able to improve performance over multiplexed techniques.

I. INTRODUCTION

The resonance absorption project [1] incorporates a transmission-type radiographical system for detecting explosives. Gamma rays are passed through an object and are detected on the opposite side by an array of gamma detectors. The gamma rays of interest are between 6 and 10 MeV. The detector array consists of 64 bismuth germinate (BGO) detectors, each with a maximum average signal rate of ~25 kHz. Because we use a radio-frequency-quadrupole (RFQ)-type accelerator with a maximum duty factor of 20%, the maximum single-detector-channel instantaneous rate is 5 times the average rate, or ~125 kHz. The total-detector-array average rate is 64×25 kHz, or 1.6 MHz, giving a total instantaneous rate approaching 10 MHz.

The data output from this system consists of several region-of-interest (ROI) integrals for each viewing position and a full-energy histogram for each detector. The data is also tagged with both rotational and vertical position information. The histogram data is used for on-line diagnostic purposes, and the ROI data is used for tomographic reconstruction and subsequent analysis. Minimizing dead-time effects resulting from processing electronics was a major design goal of this data acquisition system.

II. DATA-ACQUISITION-SYSTEM DESIGN CRITERIA

The data acquisition system was designed to meet the following criteria:

- provide near real-time results; that is, the total data set must be acquired and processed at a rate of ~1.6 million events/s;
- contribute very little additional dead time;
- allow changing requirements, such as greater computational power, greater amounts of memory, etc.;
- use commercially available hardware and software that ensures reliable operation and ease of reproduction; and
- use custom-designed hardware and software only where necessary to meet system requirements.

Given these criteria, a VMEbus-based system [2] was selected as the platform. The VMEbus provides a vast source of high-performance, commercially available products and allows the use of multiple processors and large shared-memory arrays. The VMEbus has 32-bit addressing and up to 64-bit data transfer capabilities [3]. VxWorks, from Wind River Systems [4], was selected as the real-time operating system. All software development is done on a Sun SparcII workstation, and each CPU on the bus runs the VxWorks real-time kernel. The Vxworks development software allows programs to be developed on the workstation, then down loaded to each target CPU on the bus as executable code. This down loading is performed over an Ethernet link. The control of each processor on the VMEbus can be orchestrated from the workstation via a UNIX-type remote log-in.

III. DATA ACQUISITION HARDWARE

A. General Description

Figure 1 is a hardware block diagram of the data acquisition system. The detector signals, derived from individual photomultiplier tubes viewing BGO scintillators, lead directly into the individual channels of the charge-integrating, multichannel analyzer (VMEMCA) boards [5]. This board comprises two sections: a Mizar MZ8135,3U VME board and an analog processing section. The Mizar board consists of a Motorola MC 68030 CPU, with one megabyte of dual-port memory, and a daughter-board interface that allows custom boards to be attached. Designed specifically for this project, the analog processing section has 12 independent channels. Each channel consists of a programmable low-level discriminator (LLD); a programmable gain amplifier (PGA); a charge integrator; an analog-to-digital converter (ADC); and a first-in first-out memory (FIFO).

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Fig. 1. Hardware block diagram.

Under normal operation, the program executed by the VMEMCA's CPU sequentially reads each FIFO of the analog section. The FIFO's data is combined with the detector number and the rotational and vertical position information to form a specific memory address used to generate an energy histogram and the ROI data. This data is stored in the VMEMCA's dual-ported memory, which can be read by other CPUs on the bus for further processing.

B. System Performance

The time required to process each event is dominated by the time to integrate the charge from each detector. The dead-time contribution of the processing electronics is <100 ns. Depending on the desired resolution required, an integration time can range from 400 to 1400 ns; the principal decay time of BGO is 300 ns [6]. Depending on the integration time, each event requires 500 to 1500 ns to process and store data into the FIFO. A 125-kHz, single-channel instantaneous rate implies a 6% dead time for a 500-ns processing time, and a 16% dead time for 1500 ns. Because the average single-channel rate is one-fifth the instantaneous rate, each FIFO must be read out at a 25-kHz rate to prevent data losses. The amount of time for histogramming and generation of ROIs for all 12 channels is carried out at <3 μ s/event, or ~ 300 kHz.

Energy resolution tests were performed using radiation check sources (^{60}Co and ^{137}Cs) with BGO, NaI(Tl), and BaF₂ detectors. Figure 2 shows the pulse-height spectrum for 9.172-, 7.000-, and 6.130-MeV gamma rays obtained with the system's standard 2- by 4- by 10-cm BGO detector.

C. Analog Power Distribution

The large number of analog channels in the VME crate required a method of distributing analog power. After considering various methods, such as using on-board power converters or the CERN VME430 backplane, we selected a backplane made by the Augat Corp. The Augat PN.8160-VME-0-20E-A1 has five extra power planes that can be connected to pins on P2 either with solder clips or wire-wrap. We used a separate linear power supply for the analog section.

Fig. 2. Spectrum from system's standard BGO detector.

IV. SOFTWARE DESCRIPTION

A. Software Development

All of the software developed for this project was written in the ANSI C-programming language, using a Sun SparcII workstation and the VxWorks development environment. The GNU-C cross compiler was used to generate executable code for the Motorola MC68030 CPUs on the VMEbus. This configuration has proven to be very powerful in developing the system's software. Not only are all the tools of the UNIX operating system available, but the extensions provided by VxWorks allow relatively painless implementation of the real-time programs. For example, the workstation can provide a window for each CPU on the VMEbus (see Fig. 3). The lower left-hand window is remotely logged into one CPU on the VMEbus, and the lower right-hand window is remotely logged into another CPU, in this example, a VMEMCA board. This feature permits the loading of control programs for each CPU at the workstation, which is also used as the operator input and display. The largest window in Fig. 3 shows the pulse-height spectrum of ^{60}Co measured with a BGO scintillator input into one channel of the VMEMCA card. The "cmdtool" window, located at right center, displays the program running on the workstation that receives data packets sent over Ethernet from the main CPU on the VMEbus. The "text editor" window, located just above the "cmdtool" window, displays the set-up parameters for setting the VMEMCA's gains, LLD, ROIs, etc. This data can be modified and updated at any time.

B. Software Operation

The software programs that control the system are distributed among the Sun workstation; a MVME147 CPU, which serves as the VMEbus master CPU; and the six VMEMCA CPUs on the VMEbus backplane. The following sequence of operations describes the functions of the separate tasks and their interactions.

1. After powering up the system, the SUN workstation loads and runs the SUN operating system, then the MVME147 CPU and the six VMEMCA CPUs load and begin running the VxWorks operating system.

Fig. 3. Workstation screen dump.

2. The VMEMCA CPUs then download their tasks from the SUN workstation disk via Ethernet. The tasks that run on all VMEMCA CPUs are the same, although each processor sets its dual-ported memory at a different absolute location that is known by the MVME147 CPU.
3. Next, all of the VMEMCA CPUs execute the initialization task "init_mz8135," which performs the following functions:
 - sets base address for dual-ported memory;
 - connects and enables mailbox interrupts for communicating with the MVME147 CPU;
 - writes the DAC values to set up the gain, LLD, etc. for each detector channel;
 - writes an array of pointers to an absolute memory address to allow the MVME147 CPU access to all data;
 - zeros all data arrays; and
 - spawns the "read_fifos" task.
4. The "read_fifos" task sequentially reads each of the VMEMCA's 12 FIFO channels and generates energy histograms and ROI arrays.
5. The other tasks running on each VMEMCA CPU are connected to mailbox interrupts; they are "enable_acq," "disable_acq," "zero_memory," and "disable_read_fifos."
6. The tasks on the MVME147 CPU control overall system operation. After the MVME147 downloads files from SUN disk via Ethernet, it executes the "init_mv147" task. This task reads both the data pointers from the six VMEMCA boards and the ROI limits from disk file on SUN, then calculates and stores the ROI lookup tables on each VMEMCA board.
7. The task "go_tomo" is used to scan an object and performs the following functions:
 - reads the setup disk file from the SUN (this file contains all pertinent run parameters, such as the number of views in a 360-deg rotation and the number of slices needed to fully measure the object);
 - initializes the MVME147's serial ports;
 - sends commands to motor controllers to position the rotary table and vertical translator for obtaining the unattenuated data set; and
 - spawns the "master_acq" task.
8. The "master_acq" task takes the unattenuated data, then positions the rotary table and vertical translator to take slice-1, view-1 data. After acquiring enough data to meet a specific statistical precision, the rotary table is positioned to view 2. This sequence is repeated for up to 64 slices, with 64 views each. This task also controls the six

VMECA boards by issuing mailbox interrupts to zero data and enable/disable acquisition. After the completion of each slice, the data is written to a file on the SUN workstation.

9. After an object is scanned, the data reduction task is executed, which performs the following:
 - normalizes detector array data with the monitor detector data;
 - calculates transmissions (the ratio of the attenuated to unattenuated data) for all detector, view, and slice data;
 - writes a data file to be used by reconstruction software; and
 - generates single-slice sinogram plots.

V. CONCLUSION

The data acquisition system described above (see Fig. 4) was used successfully to obtain a series of tomographic measurements. The RFQ accelerator operated at a 2 % duty factor, with peak currents and pulse widths approaching those of the design criteria. The energy resolution, dead time, and throughput performance of the system were as designed.

The versatility of the VMEbus and the modular design of the system allow for easy expansion to service larger detector arrays or to include additional CPUs or DSP modules, allowing all data reduction and analysis to be performed in near real time.

Fig. 4. Photo of data acquisition system and 64 detectors.

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