NYU ULTRACOMPUTER PROJECT

Final Project Summary
for Period 1979 - 1993

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October 1994

Prepared for

THE U. S. DEPARTMENT OF ENERGY
AGREEMENT NO. DE-FG02-ER25052

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Results from our DOE (and other) Support

From its inception in 1979 through 1993, the NYU Ultracomputer project has been continually and primarily supported by the DOE. At various times during the period, significant additional support was received from the NSF. From 1985 through 1988, substantial support was received from IBM (who were themselves funded by DARPA) for our work with the RP3 project, which initially emphasized software (primarily OS) development and subsequently was expanded to also provide support for RP3-specific combining switch VLSI design.

Rather than attempt to specify which items were accomplished under each grant, we instead describe the research accomplishments of the project as a whole. In addition to the work described below, RP3-specific development was performed for IBM.

1. Early work

Our very first work was the study of a message-passing private-memory machine with a shuffle-exchange interconnection topology. High-level simulators were constructed (Gottlieb [10] and Gottlieb and Kruskal [15]), but the principal contributions were theoretical: A series of parallel algorithms with complexity analyses were presented in an important paper by Schwartz [UC]. This paper also introduced the name Ultracomputer for the shuffle-exchange machine and coined the term *para-computer* for an idealized shared-memory machine, which we now more properly call a CRCW PRAM (Snir [44]). Another early result was a proof that the permutation problem can not be completely parallelized (later published in Gottlieb and Kruskal [11]). After meeting with a Burroughs team (led by Steve Lundstrum and George Barnes) working on a proposal for NASA's "Digital Wind Tunnel", our group turned its attention to shared-memory.

A new coordination algorithm, replace-add (later somewhat improved and renamed to fetch-and-add), was discovered and applied to find highly-parallel algorithms for queues and the readers/writers problem. These algorithms, as well as the idea of combining and a very preliminary hardware design for VLSI combining switches, appeared in Gottlieb *et al.* [16].¹

A significant consequence of our research is that, fetch-and-add and combining are now recognized as being an important part of highly parallel shared memory designs. Fetch-and-add, in particular is included in the Intel 486 microprocessor and the CRAY C90 Vector Supercomputer

2. Simulation Studies

As indicated, we first simulated Schwartz's shuffle-exchange machine. However our major simulation activity studied shared-memory designs. The Washcloth instruction-level CRCW PRAM simulator was built (Gottlieb [12]) and numerous

¹Better hardware and VLSI descriptions appear in Gottlieb *et al.* [40], Edler *et al.* [78], and Gottlieb [100].

application programs were run and timed.² Netsim (Snir [28]) extended Washcloth to incorporate a stochastic model of omega network delays to shared memory. More recently we have constructed a series of functional simulators of an omega network composed of $N \times N$ buffered crossbar switches. With the first simulator, we performed numerous experiments to test the effectiveness of combining, and the sensitivity of performance to various network parameters (Liu and Dickey [141]). The second simulator is actually a multilevel system in which switch-level transistor simulation may be driven by simulations at the register transfer and behavioral levels. It was used first during the development of our VLSI switches and then to verify the correct behavior of the fabricated parts (Dickey's Ph.D. Dissertation). The latest simulator is the most efficient to date and the most highly parameterized and therefore has been used to simulate large networks than previously possible (4096×4096) (Edler [189]).

3. Network Analysis

Analytical work on the behavior of switches and networks has concentrated on buffered networks without combining. A clock-regulated queue fed by two Bernoulli streams of messages was studied. This corresponds to one of the two output buffers used in a 2-input 2-output switch. Results were obtained for the exact analytical distributions of queue length, waiting time, and output runs (i.e. number of consecutive cycles in which an output is produced). Both infinite and finite capacity queues were analyzed. The analytical solution also has been obtained for the joint distribution of the number of waiting messages in the two output ports (Percus and Percus [138]). More recently we have obtained analytic results applicable to the second and subsequent stages of the network where one cannot assume Bernoulli streams (Percus and Percus [153]). We have applied these analyses, together with simulations, to various possible switch designs (Dickey's Ph.D. Dissertation).

A traffic model for a delta network with a single hot-spot has been developed (Liu [132]) that shows that any switch in such a network, whether buffered or unbuffered, can be analyzed as either within or isolated from a hot traffic tree. This allows methods similar to those used for uniform traffic to be used to obtain latency estimates for traffic containing single hot-spots.

4. Other Theoretical Results

We have developed a variety of theoretical results included in the list of papers below. Particularly noteworthy are those of Cole, Landau, and Vishkin whose early work includes significant advances and insights in parallel algorithms for MIMD shared memory architectures.

5. Prototype Hardware

We have constructed several bus-based Ultracomputer prototypes and currently maintain a single Ultra II prototype (now in its tenth year of operation) containing eight PEs and 8-MBs of shared memory. (Ultra I, a 2-processor system based on Motorola education boards, is no longer in use.) The memory supports fetch-and-add

²See Kalos [30]; Rushfield [55]; Korn [23], [24], and [31]; Kalos *et al.* [27]; Lubachevsky [42], Kalos and Zhong [46], Korn and Rushfield [55], and Bishop [63].

as well as other fetch-and-ops. Each PE contains a 10 MHz Motorola MC68010 augmented with Weitek 1164/65 floating-point units, a 32KB two-way set associative cache, hardware support for fetch-and-add, two serial ports, and a small amount of RAM and ROM. The PEs and MMs are placed on a single "Ultrabus" that arbitrates among the PEs. Originally, a second port on each MM was connected to a PDP-11 that, in addition to serving as an all-purpose I/O controller, connected the prototype to the NYU network, and hence to the Internet as well. More recently, we have replaced the PDP-11s with PC-clones and the NYU network structure has changed.

These prototypes were in routine use during a five year period for software development, algorithms and application studies, and scientific production, both within and outside NYU. We delivered an additional 8-PE, 8MB prototype to the NYU robotics laboratory for real-time robot control. The computer science department has offered several courses on programming MIMD shared-memory computers for which students were required to develop, run, and analyze programs on the prototypes. These courses have been valuable in disseminating the methodologies of programming the Ultracomputer in C, FORTRAN, and Lisp for a wide variety of applications. Thus, the reliability of this hardware and software has been confirmed. Over the last few years, the Ultra II prototypes have not seen much use. However, we do keep one prototype running. We expect the Ultra III prototype hardware and software to be as reliable as our Ultra II prototypes have been.

Our current hardware efforts are directed at Ultra III a 16 PE machine with 16 MMs containing 256-MBs of shared memory. Each processor is an AMD 29050 microprocessor with a 32-KB data cache and a 128-KB instruction cache. In addition, two Xilinx 4010 FPGAs are included with each processor to facilitate experiments. The PEs and MMs are connected via an omega network featuring NYU-designed, MOSIS-fabricated, full-custom, VLSI combining switches. The switch boards also contain Xilinx 4010 FPGAs to gather data for our experiments. We first constructed a 4-PE system using all the component types required for the Ultra III prototype. We now await rewiring of some miswired circuit boards (the vendor has apologized for the error and is doing the rework without charge) in order to complete the full 16-PE system.

6. VLSI Design

The PE to MM interconnection network for Ultra III is composed of custom VLSI chips which were designed by our group and have been fabricated by MOSIS in 2 μ CMOS. We currently use two part types: a forward path component, which routes and combines messages from the PEs to the MMs, and a return path component, which routes responses from the MMs to the PEs and decombines messages that have been combined on the forward path. The return path component contains an associative wait buffer that stores the combined requests until the response arrives from memory. Using MOSIS 132-pin packages, four of each component are required for a 2 $\times$ 2 switch; using 208-pin packages to be provided by NCR, two of each component are required.

In preparation for producing complete combining switches, we had designed several simpler chips, which have been fabricated by the MOSIS foundry (sponsored by DARPA and NSF); testing at NYU confirmed that the parts worked as expected. Initially, we used the MOSIS 3 μ nMOS process and obtained both combining and

non-combining 2x2 buffered switches (with narrow data paths) that operated in the 15-20 MHz range. MOSIS has fabricated a CMOS version of our non-combining switch (37-bits wide internally, 11 bits/port brought to pads) that contains approximately 36000 FETs, uses NORA clocking, and runs at 15 MHz. Using these chips, we built and tested a 4x4 network but with only a narrow data path.

The key subcomponent of the MM-to-PE direction of the combining switch is the wait buffer, an associative memory needed for the decombining of memory responses. We first built and tested MOSIS-fabricated CMOS chips containing this subcomponent. They are 32 bits wide internally, contain about 21000 transistors, and run at 16 MHz.

The combining switch that we have designed and fabricated for use in the 16 PE NYU Ultracomputer prototype is a 2x2 switch node composed of four FPCs and four RPCs. The FPC contains a single one-input, one-output combining queue, which includes an embedded ALU. The RPC contains a wait buffer, two non-combining queues, one for messages from the previous stage and one for decombined messages, and an ALU for decombining. Control for the switch is distributed as tri-state selection logic in each chip. The routing information is included in the message. Flow control avoids the necessity of acknowledgement for messages and allows pre-computation of signals that control data movement from stage to stage. The components accept two and four packet messages and allow the first packet of a message arriving when the queue is empty to exit at the next cycle.

Both the FPC and the RPC have been fabricated in 2 μ CMOS with 132 pin packages using the MOSIS service. The FPC has about 30,000 transistors, the RPC about 50,000. Both parts run solidly at 10 MHz, the upper limit of performance that can be measured in the test rig. A 4x4 combining switch board has been in use in a 4 PE prototype since November of 1992, and functions correctly at all speeds at which the memory and processors work reliably (up to 15MHz). Currently, in spring 1994, a 12 PE, 4 MM configuration using two switch boards in a 4-stage network is operational.

The combining switch components have also been prepared for fabrication by NCR in a 1.4 μ process with 208 pin packages. While the MOSIS parts can be used only in systems with no more than 16 PEs, because only 4 pins are allowed for PE/MM address, the NCR parts can be used in systems of up to 256 PEs. The higher pin count packages also allow the logic from two MOSIS chips that share an output port to be packaged on a single chip.

The modifications to the NORA (no race) clocking methodology used to implement the semi-systolic queue design is described in Dickey and Kenner [175]. Details of the VLSI design of the combining switch implementation can be found in Dickey and Kenner [192] and Dickey's Ph.D. Dissertation.

7. Coordination Algorithms

From its inception the Ultracomputer group has developed bottleneck-free process coordination algorithms. In addition to basic algorithms such as queue manipulation, readers/writers coordination, hash table access, and implementing path expressions (Dinning and Mishra [154]), we have produced variations, such as queues with multiplicity (Gottlieb *et al.* [16] and Wilson's Ph.D. Dissertation) and

readers/readers (Edler [189]), inspired by specific needs of our system software. For example, the ready queue in our operating system is composed of queues with multiplicity. Other algorithms have been developed to satisfy application programming requirements. For example our standard libraries include various barrier and semaphore algorithms in addition to the bottleneck-free algorithms that form our primary goal. We continue to evaluate our algorithms (Wood [150]) and seek improvements (Freudenthal and Peze [148]).

Several manufacturers have told us that, for their existing hardware environment (but not for new designs), it would be significantly easier to implement fetch-and-add(X, e) if e were restricted to ± 1 . These restricted operations are often called fetch-and-increment and fetch-and-decrement. In response, we have reviewed many of our algorithms to see which ones can be implemented with equal (asymptotic) efficiency using only fetch-and-increment/decrement; the most surprising positive result was for readers/writers (Freudenthal and Gottlieb [159]). Yew *et al.* and Goodman *et al.* have shown that one can always simulate fetch-and-add at a cost logarithmic in the number of processors.

In order to support a "loosely synchronous" programming style where algorithms employ barriers fairly frequently and the set of cooperating processes is determined only at runtime, we have developed a series of *group lock* coordination algorithms. Processes may enter and leave groups dynamically and current members can execute barriers (Dimitrovski [112] and his Ph.D. Dissertation).

8. Systems Software

We first implemented a serialized "master-slave" version of UNIX to obtain a functioning operating system as soon as possible and thus allow early experimentation with parallel application programs. Our major effort was a highly-parallel extension of UNIX (Version 7), which has been implemented and been in routine production use on our hardware prototypes. This system, dubbed "Symunix", is fully symmetric in that all PEs can execute the operating system concurrently. The master-slave system should be thought of as a serial program (running on multiple processors) that supports concurrent user programs; whereas Symunix is itself a highly parallel program using F&A-based algorithms that are largely free of critical sections. A spawn system call, capable of creating concurrently multiple new processes, has been implemented and is usable from both C and FORTRAN.

A new operating system, "Symunix II", is currently being developed which is based on Berkeley UNIX (4.3 BSD) but with major conceptual changes to memory management and process control along with support of asynchronous system calls. These changes, were initially described in Edler *et al.* [135] and [136], and definitively in Edler's Ph.D. Dissertation. are intended to aid in the support of highly parallel applications.

Our environment supports parallel programming in C, FORTRAN (Berke [137]), Lisp (Dimitrovsky's Ph.D. Dissertation), and Ada (Flynn *et al.* [107] and Flynn's Ph.D. Dissertation). We had participated actively in the Parallel Computing Forum (PCF) national effort to define a standard for parallel FORTRAN.

We have studied theoretical and pragmatic issues involved in the debugging of parallel programming. Our parallel debugger, pdb (Berke, Ultracomputer

Documentation Note #3), has been used to track down subtle errors both in users' programs and systems software. Study of on-the-fly detection of access anomalies has resulted in new algorithms with lower costs (Schonberg [149]).

9. Application Software

Application studies run under simulation began well in advance of hardware design. During 1985, when our hardware became available for production use, application programmers shifted their emphasis from simulations to experiments performed on the prototypes (Greenbaum [99], Greenbaum *et al.* [126], and Chiabaut *et al.* [144]). The primary subject area has remained scientific programming, the longtime strength of the Courant Institute.

10. Compiler Development

One of our staff members has become the lead maintainer of GCC, the widely used GNU C compiler. This work, which began when we needed a compiler for the AMD 29000 series processor chosen for Ultra III, has attracted the attention of a number of computer manufacturers. One result has been the arrival of workstations donated/loaned by these manufacturers for our use. These workstations include, DEC Alpha, IBM RS6000, DG Aviiion, and HP Snake.

11. PhD Theses A number of PhD theses have been supported by our project. Seven have been completed:

- Clyde Kruskal, on analysis of parallel algorithms
- Lawrence Rudolph, on software structures for parallel computing
- Kevin McAuliffe, on caches for parallel systems
- Isaac Dimitrovsky, on a parallel LISP system
- Jim Wilson, on parallel queue algorithms
- Yue-Sheng Liu, on network simulation
- Patricia Teller, on TLB consistency mechanisms
- Susan Dickey, on the design of combining switches.

One thesis is being completed this year:

- Jan Edler, on parallel operating systems

Other graduate students who have worked on our project are Brian Anderson, Wayne Berke, Guoying Chen, Susan Flynn, Eric Freudenthal, Benchiao Jai, Larry Kaplan, Richard Kenner, Susan Lambe, Mikha Liberman, Markantonatos Mitsoulides, Nagabhu Prabhu, Debera Rennels, Milan Tuba, John Turek, Jiarui Wang, Cheuk-Bun Wong, David Wood, Chin Woo You, and Yongtao You.

One NYU undergraduate student, Miriam Ayala, has also worked on the project, as have three undergraduates visiting from France.

Some of the students listed above have later joined our project as full-time staff members.

Since the inception of our project, we have produced almost 300 reports, most of which are available in both electronic and paper form. As of now, we have written 195 Ultracomputer Notes, 2 Ultracomputer Application Notes, 7 Ultracomputer Documentation Notes, 28 Ultracomputer Hardware Notes, 2 Ultracomputer Scientific Programming Notes, and 66 Ultracomputer System Software Notes.

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