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1993 Annual Final Progress Report: July 1992 through June 1993

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ABSTRACT

This is the first annual report since the Inauguration of the University Center of Excellence for Photovoltaics Research and Development (UCEP) at Georgia Tech. The essential objective of the Center is to improve the fundamental understanding of the science and technology of advanced PV devices and materials, to provide training and enrich the educational experience of students in the field, and to increase U.S. competitiveness by providing guidelines to industry and DOE for achieving cost-effective and high efficiency PV devices. These objectives are to be accomplished through a combination of research and education. This report summarizes the technical accomplishments, including modeling, processing, and characterization of cast multicrystalline silicon solar cells; use of modeling and PCD measurements to develop a road map for progressing toward 20% multicrystalline and 25% single crystalline cells; the development of a novel PECVD SiN/SiO₂ AR coating that also provides good surface passivation; PECVD deposited SiO₂ films with record low S and D_{it} at the SiO₂/Si interface; and educational activities and accomplishments.

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SUMMARY

As research and development continues towards the goal of determining viable materials to convert sunlight into electricity, it becomes increasingly obvious that single crystal and multicrystalline silicon materials continue to be the most reliable and cost effective PV materials available today. It is expected that this will remain the case well into the next century. In 1992, of the 18.1 megawatts of PV energy sold by companies in the U.S., 16.4 megawatts came from single and multicrystalline silicon. The remaining 1.7 megawatts were thin film panels, primarily amorphous silicon.

The last ten years have seen significant increases in single crystalline and multicrystalline solar cell efficiencies. However, there exists a large gap between current and theoretical efficiencies for solar cells made from these materials. This is why basic research into crystalline silicon PV materials continues to be so important toward achieving high efficiency and low cost PV power as a clean, safe alternative to conventional power production.

Single and multicrystalline silicon materials research at Georgia Tech follows two tracks. One track pursues a basic understanding of the limiting mechanisms in material quality which affect device performance. The second track seeks to develop methodologies, compatible with solar cell processing, that will enhance material quality and lead to higher efficiencies.

Following these tracks has lead toward significant advancement of understanding the limiting mechanisms in cast and sheet multicrystalline

materials. This understanding has enabled the optimization of our processing technology to yield higher quality surface passivation and longer bulk carrier lifetimes. This optimization has resulted in significant increases in solar cell efficiencies on cast and sheet multicrystalline materials.

A combination of optimized aluminum and phosphorous gettering, oxide passivation and double layer AR coating resulted in a record high 17.7% efficient one-sun solar cell on cast multicrystalline silicon. It has been identified that the aluminum treatment used to form back surface fields can contribute up to 1% (absolute) increase in cell efficiency and can improve bulk lifetime from 10 μ sec to 24 μ sec. There is, however, a combined decrease in back surface reflection and an increase in J_0 because of the rough surface which results from alloying of the silicon with the aluminum. Effective phosphorous gettering, without severe heavy doping effects, is attained through a deep phosphorous diffusion followed by an etch back to target resistivity. Front oxide passivation reduced J_0 by a factor of two and increased J_{sc} by 1mA/cm², which finally lead to an additional ~1% (absolute) increase in efficiency for these cells.

Significant increases in solar cells processed from EFG multicrystalline silicon have been achieved by applying the optimized processes outlined above and used on cast multicrystalline materials. Gains in EFG cell efficiency from 7.8% to 14.1% have been achieved using a combination of front surface oxide passivation, and aluminum diffusion followed by a 400°C forming gas anneal. Detailed studies show that oxide passivation of these cells leads to an additional

0.8% increase in efficiency. Al BSF formation can lower J_0 by a factor of two which results in an additional 1.4% increase in efficiency. An additional 4.1% increase resulted following a 400°C forming gas anneal following the aluminum diffusion. These complementary effects yield a total increase in efficiency of 46%.

Significant gains have been made during the past year on the development of plasma enhanced chemical vapor deposition (PECVD) of SiO_2 and SiN films for both surface passivation and AR coatings. As an AR coating, it has been demonstrated that the (PECVD) SiO_2 /SiN gives much greater improvement in cell parameters, 57% in J_{sc} , 8% in V_{oc} , and 66% in efficiency when compared with thermally evaporated MgF_2 /ZnS coatings which improves J_{sc} by 50%, V_{oc} by 2%, and cell efficiency by 54%, for cells without thermal oxide passivation. For cells that have a thermal oxide, the improvements in J_{sc} , V_{oc} , and efficiency are fairly comparable for the two films. We have also demonstrated that thin SiO_2 ($\sim 100\text{\AA}$) deposited by direct PECVD at 250°C on to high resistivity wafers, and annealed using an optimized rapid thermal anneal (RTA) in forming gas at 350°C, results in very low surface recombination lifetimes ($< 2\text{ cm/s}$). This low temperature process also results in very high effective carrier lifetimes ($> 5\text{ms}$). Concurrently a similar process has been developed for metal-oxide-silicon (MOS) structures. Approximately 500-A-thick SiO_2 layers, deposited on Si by PECVD at 250°C with 0.02 W/cm^2 rf power, then covered with an evaporated thin aluminum layer, and finally subjected to

a photo-assisted anneal in forming gas ambient at 350°C, resulted in interface state density(D_{it}), in the range of $1-4 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ near midgap of silicon. The best D_{it} value achieved in this study was $1.1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$. This is the lowest D_{it} value report to date for PECVD deposited oxides.

1.0 INTRODUCTION

1. Objective

This marks the first annual report since the Inauguration of the University Center of Excellence for Photovoltaics Research and Development (UCEP) at Georgia Tech. The essential objective of the center is to improve the fundamental understanding of the science and technology of advanced PV devices and materials, to provide training and enrich the educational experience of students in the field, and to increase U.S. competitiveness by providing guidelines to industry and DOE for achieving cost-effective and high efficiency PV devices.

These objectives are to be accomplished through a combination of research and education. In addition to teaching solar cell courses and providing practical training to students at Georgia Tech, a new Educational Support Program (ESP) laboratory has been built from scratch. This lab will support university-level educational programs in the nation through the establishment and operation of the ESP silicon solar cell fabrication laboratory. The fabrication laboratory will provide a baseline capability to manufacture 18% - 20% efficient silicon solar cells from 3" Fz wafers. The fabrication laboratory shall fabricate silicon solar cells according to run sheets and materials submitted by students in university-level courses or programs on solar cells. The second major objective of this program is to conduct basic and applied research to advance the science and technology of silicon solar cells and materials. This work is

expected to assist the PV industry in cost-effective development of silicon solar cells and give US a competitive edge in the field by setting the pace and trajectory of research and development and will produce well trained students to continue the much needed development of cost-effective and high efficiency photovoltaic devices. The quality of research will be sufficient for graduate thesis requirements.

Research thrusts involve developing and optimizing cost-effective processes for use in the fabrication of solar cells, gettering and passivation of impurities and defects, modeling and design of high efficiency cells and fabrication and testing of high efficiency one-sun cells on monocrystalline and multicrystalline silicon substrates.

This program provides the opportunity for scientists from other institutions to work in the ESP laboratory which may also provide a means of technology transfer from Georgia Tech and other institutions.

1.2 Accomplishments

Significant progress was made last year in the area of research and education of photovoltaic. This report summarizes the technical accomplishments. Sections 2 and 3 describe modeling, processing and characterization of cast multicrystalline silicon solar cells. Attempts were made to quantify and improve fundamental understanding of the beneficial effects of oxide passivation, Al diffusion, and forming gas anneal, which resulted in the

fabrication of a record high 17.7% efficient cell on OTC multicrystalline silicon and a 14.1% efficient EFG cell without H^+ implantation. Accomplishments on single crystal include fabrication ~19% efficient flat cells and ~21% efficient textured monocrystalline cells. Through modeling and PCD measurements, a road map has been developed for progressing toward 20% multicrystalline and 25% single crystalline cells. These results are discussed in section 4. The development of a novel PECVD SiN/SiO_2 AR coating that also provides good surface passivation is discussed in section 5. PECVD deposited SiO_2 films with record low S and D_{it} at the SiO_2/Si interface is also discussed. Finally, section 6 describes the educational activities and accomplishments. These include construction and completion of the educational support program lab, design and printing of a brochure, course offerings on solar cells and the visiting scientist program.

2.0 FABRICATION AND MODELING OF MULTICRYSTALLINE SILICON SOLAR CELLS

2.1 Introduction

In the last 10 years, one sun single crystal cell efficiencies have increased from 18% to 23% while the multicrystalline silicon cell efficiencies have risen from 16% to 17.7%. In spite of this progress, considerable research opportunities and gap exist between the current and theoretically achievable cell efficiencies which are estimated to be in the range of 25-27% for single crystal and 20-22% for multicrystalline silicon.

Large-grain multicrystalline silicon is widely used for production of silicon solar cells. The major advantage of multicrystalline silicon is its relatively low cost. The disadvantages are the significantly lower lifetime compared to single crystal Si and inhomogeneous nature of material. These two drawbacks, which are due to the presence of grain boundaries as well as large concentrations of dislocations, defects, and impurities result in smaller multicrystalline silicon cell efficiency compared to single crystal silicon. Since we have to live with this defective material, we need to find some smart and inexpensive ways to improve the quality of the multicrystalline silicon. Various ways to improve multicrystalline silicon solar cell efficiency have been pursued in the past. One strategy is to reduce the cell thickness and to employ light-trapping concepts which make the cell performance less dependent on lifetime. A second alternative is to use hydrogen passivation to reduce the electrical activity of defects whereby hydrogen atoms tie up the dangling bonds in the

defected regions and reduce the density of midgap recombination centers. The third method involves gettering of lifetime-limiting impurities which removes recombination centers from the active part of the cell. This section of the report focuses on optimization of gettering conditions while the next section deals with hydrogen passivation of EFG sheet silicon.

In spite of recent accomplishments in boosting multicrystalline cell efficiency, the exact identification and degradation mechanisms of efficiency limiting defects in multicrystalline cells are not fully understood. Extensive research has been conducted on this topic using single crystal silicon, but little has been done on multicrystalline silicon. Multicrystalline silicon quality suffers from the presence of grain boundaries and point defects, such as vacancies, interstitial, transition metal impurities, oxygen, carbon, and their complexes. Therefore what has been learned on single crystal silicon is not always applicable to multicrystalline silicon. Gettering and passivation techniques need to be developed, understood, and optimized for multicrystalline materials. For example, we showed elsewhere [1] that optimum resistivity ($\geq 1 \Omega\text{-cm}$) for multicrystalline cells differs from the optimum resistivity of single crystal silicon ($0.2 \Omega\text{-cm}$), possibly because of dopant-defect interactions in multicrystalline silicon. Also, unlike single crystal silicon, a small amount of oxygen may be beneficial to some multicrystalline silicon materials by virtue of defect passivation [1-3].

The objective of this section is to fabricate and analyze high efficiency

multicrystalline cells by a combination of gettering, passivation, detailed cell characterization, and modeling. Phosphorus and aluminum treatments were investigated and optimized for gettering and passivation of defects in multicrystalline silicon. An optimized process sequence was developed to achieve high efficiency cells on cast multicrystalline silicon wafers obtained from Osaka Titanium Corporation (OTC). The same optimized process sequence was also used to fabricate cells on single crystal Float Zone (FZ) wafers. OTC multicrystalline silicon wafers were 0.8 Ω -cm, boron-doped p-type with $1-10 \times 10^{17} \text{ cm}^{-3}$ oxygen and $3-5 \times 10^{17} \text{ cm}^{-3}$ carbon (measured by the OTC supplier). Single crystal FZ wafers were also p-type but had lower (0.2 Ω -cm) resistivity. Due to the lack of availability of the appropriate grain boundary defect data, and a model to account for the grain boundary effects in the cells, model calculations were attempted by ignoring grain boundary effects. Instead, a measured effective carrier lifetime in the cell was used. A good correlation was found between the measured and calculated cell data. Model calculations are performed to provide guidelines for achieving greater than 20% efficient multicrystalline silicon solar cells.

2.2 Experimental Work

2.2.1 Gettering and Oxide Passivation

In this study phosphorus diffusion on the front and aluminum treatment on the back were used as the main gettering steps, which also form the n^+ -

emitter and p^+ -back surface field, respectively. Thus, gettering is an integral rather than additional part of the cell process sequence. Prior to fabricating the high efficiency cells, baseline experiments were conducted to optimize the gettering conditions.

In our optimized process sequence, phosphorus gettering was performed at 930°C for 25 minutes, using P_2O_5 solid source. In order to take advantage of the intense phosphorus gettering, without paying the penalty of heavy doping effects in the emitter, a controlled etch-back technique was used to partially etch the n^+ -region. This approach is similar to Narayanan et al. [4], who implemented this idea successfully. A $\text{HNO}_3\text{:HF:H}_2\text{O}$ [1000:1:100] etch was used in our process sequence to increase the emitter sheet resistance from $16\ \Omega/\square$ to 30 and $80\ \Omega/\square$ by varying the etch time.

Aluminum gettering was performed by evaporating $1.2\ \mu\text{m}$ thick Al on the back of the cells followed by a high temperature drive-in for 35 minutes. Oxide passivation was done during the Al drive-in to simplify and maintain the cost-effectiveness of the process sequence. After a $1.2\ \mu\text{m}$ thick Al evaporation on the back, wafers were inserted at 850°C in the oxygen ambient to first grow $\sim 100\ \text{\AA}$ thick passivating oxide on top of the n^+ emitter region on the front. After 5 minutes of oxide growth, gas ambient was switched to nitrogen for an additional 30 minute Al drive-in. The temperature was ramped down to 400°C and then forming gas was switched on for two hours. Some cells were also fabricated without the oxide passivation or

without the Al layer during the drive-in process to quantify the merit of oxide passivation and Al treatment on multicrystalline cells.

2.2.2 Fabrication of High Efficiency Multicrystalline Solar Cells

Attempts were made to fabricate 1cm x 1cm high efficiency multicrystalline solar cells using the optimized gettering conditions, oxide passivation, and an evaporated double layer ZnS/MgF₂ antireflection coating. This cell structure was first introduced by Green et al [4-6]. First 30-40 μm Si was removed from each side by a chemical etch in order to remove the saw damage from the as-received multicrystalline wafers. After the chemical polishing, the substrate thickness was about 300 μm . The emitter region was formed by 930°C/25 min phosphorus diffusion followed by an etch-back to 80 $\Omega/\square$. Then, as explained in section 2.2.1, the 850°C oxide passivation and Al drive-in were performed. The front grid contact was formed by evaporation of Titanium/Silver (600 Å/600 Å) and the lift-off technique. Back contact was formed by evaporating 500 Å Ti/ 500 Å Ag on the top of the Al Back Surface Field (BSF) contact region. Contacts were annealed in the forming gas ambient for 30 minutes at 400°C. About 5 μm thick silver was plated on the front grid pattern to reduce the series resistance. Finally, a 550 Å ZnS/1100 Å MgF₂ double layer AR coating was deposited by thermal evaporation on the cells. All the cells were characterized by light and dark I-V measurements, open circuit voltage decay lifetime measurements, spectral response, hemispherical

reflectance, and internal quantum efficiency measurements. Dark I-V data was also taken and analyzed by a double exponential model [7] to determine the reverse saturation current (J_{01}), junction recombination current (J_{02}), and series and shunt resistances.

2.3 Solar Cell Modeling

Solar cell modeling was performed to match the performance of the highest efficiency cell obtained in this study and to provide guidelines for achieving greater than 20% efficient cells. Solar cell efficiency calculations were performed using the PC-1D model [8] in a mode which allows external input file for the doping profile. PC-1D is a software package for personal computers that uses finite-element, drift-diffusion analysis to solve the fully-coupled, two-carrier, semiconductor transport equations in one dimension [9]. Grain boundary defects and effects were ignored. Instead, the measured effective bulk lifetime was used as the input to assess whether grain boundary or intragrain defects dominate the cell performance. A good match between the measured and calculated cell parameters and IQE would suggest that intragrain defects dominate the cell performance. A significant mismatch would indicate the importance/dominance of grain boundary defects on the cells. The following n^+pp^+ cell configuration and reasonable material input parameters were used for the numerical simulations.

1. Cell area of 1 cm².
2. Cell thickness of 300 μm .
3. p-type base with resistivity of 0.8 $\Omega\text{-cm}$.
4. External doping file, 16 $\Omega/\square$ Ercf doping etched to 80 $\Omega/\square$ sheet resistance, junction depth of 0.5 μm .
5. Ercf doping profile with surface concentration of $5 \times 10^{18} \text{ cm}^{-2}$ for the 1 μm thick Al BSF.
6. Measured bulk lifetime.
7. FSRV of 1000 cm/sec for passivated phosphorus emitter between the contact grid lines and 1.0×10^6 cm/sec beneath the fingers.
8. BSRV of 1.0×10^6 cm/sec at metal-silicon contact.
9. Measured J_{02} and ideality factor.
10. Measured series resistance.
11. Measured 3% shadow loss and external input file for the measured front surface reflectance.
12. 69% efficient back surface reflector (measured at Sandia).
13. Flat front and back surface.
14. Spectrum AM1.5 Global.

Front and back surface recombination velocities (SRV), and BSF doping profile were the only unmeasured parameters used in the modeling of the highest efficiency cell. Both the SRV numbers used are reasonable for a

passivated emitter and metal backed BSF. BSF doping profile was taken from experimental data in reference 15.

In order to provide guidelines for achieving higher efficiency cells, various cell design parameters, such as lifetime, thickness, surface texturing, and surface recombination velocities were varied after matching the performance of the 17.7% efficient cell obtained in the investigation.

2.4 Results and Discussion

2.4.1 Effects of Phosphorus Gettering and Emitter Etch-back

Phosphorus diffusion, which is known to be an effective impurity gettering process in silicon [10], also has the potential of passivating grain boundaries [11]. However, preferential grain boundary diffusion of phosphorus much deeper than 10 μm is not practical because it must be done at a temperature ($\geq 1000^\circ\text{C}$) considerably higher than the desirable solar cell junction-formation temperature [11]. The phosphorus diffusion temperature in this study was varied in the range of 880-1030 $^\circ\text{C}$ to find the optimum texture. Since it was not easy to measure PCD lifetime in multicrystalline silicon materials, the measured Open Circuit voltage Decay (OCD) lifetime on just the phosphorus diffused samples was used as an indicator for gettering efficiency or process optimization. Table 2-1 clearly shows that the optimum phosphorus diffusion temperature is around 930 $^\circ\text{C}$ for these multicrystalline silicon cells. This is consistent with Martinuzzi et al. [12].

Table 2-1. The Effect of Phosphorus Diffusion Temperature on Measured OCD Lifetime.

Phos. Diffusion Temperature (°C)	OCD Lifetime (μ sec)	Sheet Resistance($\Omega/\square$)
880	6.0 (± 1.0)	25
930	9.0 (± 1.0)	16
980	2.0 (± 0.5)	12
1030	1.0 (± 0.5)	8

Diffusion time was also varied from 15-45 min. but no change was observed in the measured lifetime. So the phosphorus diffusion temperature was intentionally kept below 1000°C to prevent any process induced lifetime degradation in multicrystalline silicon [12], but was kept above the conventional 850°C temperature to achieve fairly intense gettering (Table 2-1). It has been suggested [10] that phosphorus diffusion causes substitutional impurities to become interstitial, which then diffuse into the n^+ -region. Narayanan and Green [4] have suggested that phosphorus diffuses more rapidly in the grain boundaries to form deeper p-n junctions in the grain boundaries which can also improve carrier collection. However, spreading resistance data showed that the 930°C/25 min diffusion used in our study gave 16 $\Omega/\square$ sheet resistance, with $\sim 1\mu\text{m}$ thick, very heavily doped emitter. This reduced the cell performance

because of the thicker dead layer and heavy doping effects, such as Auger recombination and bandgap narrowing. Therefore, an emitter etch-back technique was used to partially remove the heavily doped n^+ -region, thus raising sheet resistance and thinning the emitter. Table 2-2a shows a comparison of the oxide passivated cells fabricated with different emitter sheet resistance. The cells with high emitter sheet resistance of $80 \Omega/\square$ gave the highest V_{oc} , J_{sc} and cell efficiency while the $16 \Omega/\square$ cells gave the lowest cell efficiency. No attempts were made to increase the sheet resistance beyond the $80 \Omega/\square$ because the grid design used in this study was not suitable for greater than $100 \Omega/\square$ sheet resistance. These cells were also analyzed by the reverse saturation current (J_{01}) and internal quantum efficiency (IQE) measurements. J_{01} consists of emitter and base components ($J_{01} = J_{01e} + J_{01b}$). J_{01b} should be independent of emitter etch-back, therefore any measured difference in the J_{01} with emitter etch-back will reflect the change in the J_{01e} provided the J_{01e} is an appreciable part of the J_{01} . A comparison of the reverse saturation current (J_{01}) of the oxide passivated cells with different emitter sheet resistances, Table 2-2b, shows that an increase in the sheet resistance from 30 to $80 \Omega/\square$ decreased the J_{01} by a factor of 7.3 in the single crystal cells. This indicates that the J_{0e} contributes extensively to the total J_{01} in the FZ cells. However, there was virtually no change in the J_{01} due to emitter etch-back of the multicrystalline cells, indicating that the J_{0e} plays a negligible role in dictating the J_{01} or V_{oc} of these gettered and oxide passivated multicrystalline cells with

lifetimes of 25 μsec . Figure 2-1 shows that the emitter etch-back from 30 to 80 $\Omega/\square$ enhanced the quantum efficiency of the multicrystalline cells in the short wavelength range by reducing the heavy doping effects and absorption in the dead layer. This resulted in about 2.3 mA/cm^2 increase in J_{sc} .

Table 2-2a. Light and Dark I-V Analysis of the Oxide Passivated Cells Fabricated on OTC Multicrystalline Silicon with Different Emitter Sheet Resistances

Emitter Sheet Resistance ($\Omega/\square$)	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Efficiency (%)	R_{series} (Ω)	R_{shunt} (K Ω)	J_{01} (A/cm ²)	J_{02} (A/cm ²)	Lifetime (OCD) μ S
80	35.6	626	0.792	17.7	0.34	299	1.33×10^{-12}	9.37×10^{-7}	25
30	33.3	616	0.776	15.9	0.30	2485	1.29×10^{-12}	8.73×10^{-7}	25
16	32.5	608	0.757	15.0	0.28	456	1.12×10^{-12}	8.23×10^{-7}	24

2-12

Table 2-2b. Light and Dark I-V Analysis of the Oxide Passivated Cells Fabricated on FZ Single Crystal with Different Emitter Sheet Resistances.

Emitter Sheet Resistance ($\Omega/\square$)	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Efficiency (%)	R_{series} (Ω)	R_{shunt} (K Ω)	J_{01} (A/cm ²)	J_{02} (A/cm ²)	Lifetime (OCD) μ S
80	36.7	663	0.806	19.6	0.33	285	1.87×10^{-13}	1.83×10^{-6}	18
30	33.3	635	0.815	17.2	0.27	280	1.36×10^{-12}	6.13×10^{-6}	18

Figure 2-1. The effect of different emitter sheet resistance on Internal Quantum Efficiency.

2.4.2 Beneficial Effects of Al Treatment

Several investigators [11-14] have studied the beneficial effects of rear aluminum treatment on multicrystalline silicon solar cells. It has been suggested in the literature that the preferential aluminum diffusion might passivate grain boundaries by (1) reducing the grain boundary states via removal of dangling bonds and interaction with segregated oxygen in the grain boundary [11] and/or (2) the formation of a high-low junction at the grain boundary which can reduce the effective recombination velocity at the grain boundaries [11]. Other considerations for using aluminum for the backside gettering include process compatibility with solar cell fabrication sequence because Al diffusion not only makes the rear contact and BSF, but Al and phosphorus gettering effects were shown by Martinuzzi to be complimentary in nature [15]. It is well known [16] that phosphorus getters metallic impurities such as Fe, Cr, and Ti, while there is a lack of similar data for Al. Thus Al treatment has the potential of improving J_{sc} by gettering-induced bulk lifetime enhancement and grain boundary passivation, and V_{oc} by the formation of back surface field and increased bulk lifetime. It has also been shown by other investigators [17] that optimizing the alloying temperature and the amount of Al can reduce the back surface recombination velocity (BSRV) to less than 1000 cm/sec at the p-p⁺ interface.

The aluminum drive-in temperature in this study was varied in the range of 750-950°C to find the optimum temperature. The temperature should not be very high to avoid process-induced degradation of lifetime in multicrystalline

silicon, because Si materials which contain impurities and defects generally cannot stand very high temperature. On the other hand, Al gettering can be more effective at higher temperatures. Proper cleaning of Al and silicon wafers was found to be critical for minimizing the Al process-induced contamination. Improvement in V_{oc} contains the information about the enhanced lifetime as well as the BSF effect. Since it was not easy to decouple the two effects precisely in these cells, the V_{oc} was used as the indicator for process optimization. Figure 2-2 clearly shows that for this OTC multicrystalline silicon material, 850°C is the optimum drive-in temperature because it gave the highest V_{oc} . The exact gettering mechanism and the reasons underlying the optimum Al gettering temperature are not clear at this time. Below the 850°C drive-in, the V_{oc} increased with increasing drive-in temperature for two reasons: first, the Al gettering efficiency increases with the temperature, and second, the thickness and effectiveness of the BSF increases with the temperature. The decrease in V_{oc} beyond 850°C is probably because defective materials like multicrystalline silicon cannot stand very high temperature processing without lifetime degradation.

Figure 2-2. The effect of Al drive-in temperature on V_{oc} of the OTC multicrystalline silicon solar cells.

In order to understand the effect of Al treatment and decouple the impact of BSF, BSR, and gettering, 1cm x1cm cells were fabricated with only half the multicrystalline silicon wafer covered with Al. Thus half the cells on the wafer have 850°C Al BSF, but the cells on the other half only experience the high temperature cycle without Al. This was followed by Al deposition and 400°C/45 min forming gas sintering for the back contact formation.

Figure 2-3a shows that the cells with Al drive-in have 1% (absolute) higher cell efficiency coupled with 0.8 mA/cm² higher J_{sc} and ~9 mV higher V_{oc} . These cells have lower efficiency compared to the best cells reported in section 2.4.3 because of ~5% higher surface reflectance and higher series resistance (1 Ω -cm²).

In an attempt to determine whether Al process induced improvement is entirely due to BSF or partly due to lifetime improvement, PC-1D model calculations were performed for cells with and without BSF. Analysis of the Al effect is complicated by the reduced BSR because Al diffusion roughens the back surface. Therefore first BSR was determined by an analysis of the near band edge IQE and reflectance data [18,19]. The back surface reflectance was found to be 69% for the Al-diffused cells compared to 85% for the sintered cells without Al diffusion. Figure 2-3a shows a comparison of the measured and modeled data for the Al diffused and Al sintered cells. We were able to obtain a near perfect match between the cell data and modeled IQE for the Al diffused and Al sintered cells. This shows that grain boundary effects are not

very significant in these cells, since the grain boundary effects were ignored in the modeling. Modeling in Figure 2-3b shows that the bulk lifetime in the Al diffused cells is 24 μsec as opposed to 10 μsec in the Al sintered cells. Curve 3 in Figure 2-3b represents an Al diffused cell with 10 μsec lifetime. This will be the case if Al treatment did not do any gettering. The significant mismatch between curves 2 and 3 in Figure 2-3b clearly shows the combined BSF and BSR effects of the Al process cannot fully account for the observed increase in the IQE of the Al diffused cells. The bulk lifetime in the Al diffused cells had to be raised from 10 μsec to 24 μsec in order to get a near-perfect match in the cell data and IQE of the Al diffused cell. Thus within the limits of modeling assumptions, it appears that the Al treatment improves bulk lifetime in the multicrystalline cells. Model calculations revealed that Al treatment increased J_{sc} by 0.2 mA/cm^2 due to BSF, decreased J_{sc} by 0.1 mA/cm^2 due to reduced BSR, and increased J_{sc} by 0.7 mA/cm^2 due to lifetime enhancement, accounting for the observed increase of 0.8 mA/cm^2 in the J_{sc} of these cells. The Exact mechanism of Al gettering is still not understood.

It is important to note that the effect of texturing due to the roughened Al-Si back surface was ignored in the above analysis. Such texturing can result in an increased number of passes for the long wavelength photons which may give artificially higher bulk lifetime when texturing is ignored in the model calculations. Preliminary model calculations performed by introducing a perfect Lambertian textured surface at the back (coupled with 86% internal reflection

at the top surface [18,19]) showed only about 0.45 mA/cm² increase in J_{sc} , little change in V_{oc} , and ~0.2% increase in cell efficiency. Additionally, IQE analysis showed that the perfect random back texturing effects the IQE of these cells only beyond 0.9 μ m wavelength and, therefore, cannot account for the IQE difference between curves 1 and 3 in the wavelength range of 0.6-0.9 μ m in Figure 2-3a. Thus even perfect back texturing, in conjunction with BSF and BSR effects at the back surface, cannot account for the observed increase in the cell response unless the bulk lifetime is increased.

PC-1D model calculations gave a $J_{ob} = 1.22 \times 10^{-12}$ A/cm² and $J_{oe} = 2.89 \times 10^{-13}$ A/cm² for the Al treated cells. This translates into a $J_0 = 1.51 \times 10^{-12}$ A/cm² which is in very good agreement with the measured J_0 value of 1.79×10^{-12} A/cm². It is important to recognize that J_0 is dominated by J_{ob} in these oxide passivated cells due to fairly high saturation current density ($\sim 5 \times 10^{-11}$ A/cm²) of the Al diffused BSF with Al contact. Attempts to etch-off the top Al-layer after the drive-in and grow an oxide to passivate the Al-Si layer did not improve J_0 appreciably. This indicates that even though Al treatment improves the bulk lifetime and gives 1% improvement in the cell efficiency, it reduces the Back Surface Reflectance (BSR) and gives fairly high J_0 which could limit the V_{oc} of the cells. Reduced BSR could hurt the performance of the front surface textured cells even more. Point contact Al BSF through an oxide should be able to mitigate the above undesirable effects of Al process; however, it could be at the expense of improvement in bulk lifetime.

Figure 2-3a. A comparison of measured and modeled IQE and cell data for Al-diffused and Al-sintered cells.

Comparison of IQE Modelled by PC-1D

Figure 2-3b. Model calculations to determine the effect of lifetime and BSF on IQE and cell parameters of Al treated cells.

2.4.3 Effect of Oxide Passivation on Multicrystalline Silicon Cells

Like gettering and emitter etch-back, oxide passivation was found to be quite beneficial for the multicrystalline silicon cells. Table 2-3a shows about 1.0 mA/cm^2 improvement in the J_{sc} of the multicrystalline cells as a result of oxide passivation. This increase in J_{sc} is supported by the appreciable increase in the short wavelength response of the polycrystalline cells due to the oxide passivation (Figure 2-4). Dark I-V analysis in Table 2-3a shows that the oxide passivation of these polycrystalline cells also reduced the J_{01} by a factor of ~ 2 . This combination of increased J_{sc} and reduced J_{01} should result in an increase of 18 mV in V_{oc} [$V_{oc} = kT/q \cdot \ln(J_{sc}/J_0 + 1)$]. This agrees fairly well with the observed increase of 16 mV in V_{oc} .

Figure 2-5 shows that the optimized process sequence resulted in a record high 17.7% efficient cell (verified by NREL) on $0.8 \Omega\text{-cm}$ Osaka Titanium multicrystalline silicon with V_{oc} of 626 mV and J_{sc} of 35.60 mA/cm^2 . Even though a 17.8% efficient multicrystalline silicon solar cell was reported [2], using the Sandia National Labs calibration [20], this is the first 17.7% efficient multicrystalline silicon cell tested and verified at NREL. Dark I-V analysis gave a reverse saturation current density of $1.33 \times 10^{-12} \text{ A/cm}^2$ and a series resistance of $0.34 \Omega\text{-cm}^2$. Open Circuit voltage Decay (OCD) lifetime measurements gave effective carrier lifetime of 25 μsec measured at V_{oc} , which is quite respectable for such low resistivity multicrystalline silicon. Figure 2-6 shows the reflectance and internal quantum efficiency of the 17.7% efficient cell. It should be

recognized that optimum process sequence for multicrystalline silicon may be material specific because of the large variation in the material quality, grain size, and impurity and defect content of various multicrystalline materials. The efficiency distribution was in the range of 16.6%-17.7% (all tested and verified at NREL) on the wafer, which gave the 17.7% efficient, 1 cm², solar cell (Table 2-4). This difference in cell efficiency is partly due to nonuniform AR coating.

Table 2-3a. Light and Dark I-V Analysis of the Cells Fabricated on OTC Multicrystalline Silicon with and without Passivation Oxide.

Cell Specification	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Efficiency (%)	R_{series} (Ω)	R_{shunt} (K Ω)	J_{01} (A/cm ²)	J_{02} (A/cm ²)	Lifetime (OCD) μ S
80 $\Omega/\square$ with passivating oxide	35.6	626	0.792	17.7	0.34	299	1.33×10^{-12}	9.37×10^{-7}	25
80 $\Omega/\square$ without passivating oxide	34.6	610	0.787	16.6	0.33	150	2.70×10^{-12}	9.60×10^{-7}	23

Table 2-3b. Light and Dark I-V Analysis of the Cells Fabricated on FZ Single Crystal with and without Passivating Oxide.

Cell Specification	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Efficiency (%)	R_{series} (Ω)	R_{shunt} (K Ω)	J_{01} (A/cm ²)	J_{02} (A/cm ²)	Lifetime (OCD) μ S
80 $\Omega/\square$ with passivating oxide	36.7	663	0.806	19.6	0.33	285	1.87×10^{-13}	1.83×10^{-6}	18
80 $\Omega/\square$ without passivating oxide	35.9	650	0.792	18.5	0.32	251	3.10×10^{-13}	2.27×10^{-6}	15

Figure 2-4. The effect of emitter oxide passivation on Internal Quantum Efficiency.

Georgia Inst Tech Multi-Si Global

Sample: GTT125#23

Temperature = 25.0°C

Jan. 29, 1992 3:12 pm

Area = 1.000 cm²

$V_{oc} = 0.6259$ volts

$I_{sc} = 35.60$ mA

$J_{sc} = 35.60$ mA/cm²

$P_{max} = 17.65$ mW

Fill factor = 79.21 %

$I_{max} = 33.40$ mA

Efficiency = 17.7 %

$V_{max} = 0.5284$ V

Figure 2-5. Light I-V data of the 17.7% efficient OTC Multicrystalline cell tested at NREL.

Fig. 2-6. Reflectance and Internal Quantum Efficiency of the 17.7% efficient OTC Multicrystalline cell.

Table 2-4. Cell efficiency distribution on the wafer producing the 17.7% efficient cell.

Cell ID	J_{sc} (mA/cm²)	V_{oc} (mV)	FF	Efficiency(%)
23	35.6	626	0.792	17.7
43	35.2	623	0.785	17.2
33	34.1	618	0.794	16.7
42	34.7	613	0.779	16.6

2.4.4 Modeling and Directions for High Efficiency Multicrystalline Cells

Model calculations were performed to match the performance of the 17.7% efficient cell using the PC-1D program with the input parameters mentioned in the previous section. Table 2-5 shows that the model calculations are in a reasonably good agreement with the experimentally measured cell parameters, in spite of ignoring the grain boundary defects and effects. The slight mismatch could be due to grain boundary effects, because if we alter the ideality factor from 3.6 to 3.1, or change J_{02} from 9.37×10^{-7} to 2.50×10^{-6} A/cm², or change R_{series} from 0.34 to 0.70 Ω -cm², we can obtain even a better match in V_{oc} , J_{sc} , and FF simultaneously. Some differences in the measured and modeled lighted I-V parameters may also be due to the assumption of flat surfaces and assumed SRV values. A measured effective bulk lifetime of 25 μ sec was used in the model calculation. This indicates that in properly-gettered, large-grain multicrystalline cells, intragrain defects are probably more important than the grain boundary defects in dictating the cell performance.

Table 2-5. Comparison of the Calculated and Measured Parameters for the High Efficiency Multicrystalline Silicon Cell.

Comparison of Model & Exp.	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Efficiency (%)
Measured parameters	35.6	626	0.792	17.7
PC-1D Model	35.8	621	0.807	17.9

After matching the measured cell parameters of the 17.7% efficient multicrystalline cell, attempts were made to change the cell design and material properties, such as R_s , cell thickness, front and back SRV, BSF thickness, lifetime, and surface texturing, to provide guidelines for achieving even higher efficiencies. Table 2-6 shows quantitatively the effect of changing some of the design parameters on the performance of the cell.

Table 2-6. Modeling the Effect of Selected Design Parameters on Performance of the 17.7% Efficient Cell.

Changed Parameters	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Efficiency (%)
a: Cell thickness = 250 μ m	35.6	619	0.808	17.8
b: FSRV = 50 cm/sec	35.8	621	0.807	17.9
c: R_{series} = 0.1 Ω -cm ²	35.8	621	0.818	18.2
d: Lifetime (τ) = 100 μ sec	36.2	628	0.808	18.4
e: BSF thickness = 10 μ m	36.5	627	0.807	18.5
f: Front surface texturing	37.2	619	0.806	18.6
g: BSRV = 500 cm/sec	36.9	631	0.807	18.8
h: Front surface texturing and Reduced BSRV (f + g)	38.4	629	0.807	19.5
i: Lifetime of 100 μ sec, Front surface texturing, and Reduced BSRV (d + f + g)	39.4	658	0.809	21.0

Table 2-6 shows that change in FSRV, R_{series} , and bulk lifetime have very little effect on the cell efficiency for this cell structure. Increase in the carrier lifetime from 25 to 100 μ sec increases the absolute efficiency 0.5% (case d) for this cell with 1 μ m deep unpassivated BSF. Therefore additional gettering will not do much for this cell unless the BSF or BSRV are improved. Figure 2-7 shows that some gettering is very important, because efficiency increases rapidly with lifetime (τ) up to a lifetime value of about 40 μ sec. Beyond $\tau = 40$ μ sec, relative improvement in cell efficiency becomes very small. Model calculations show that even with the increase in the bulk lifetime value up to

1 msec, an efficiency of only 18.6% can be realized with this cell structure. Since J_{01} is dominated by J_{0b} in this cell, reduced FSRV from 1000 to 50 cm/sec also has very little effect on the performance of this cell (case b). However, significant gain in the performance, from 17.7% to 18.8%, can be realized by reducing the BSRV alone from 10^6 to 500 cm/sec by growing a passivating oxide on the back surface (case g). Similarly, surface texturing alone (case f), using slats or grooves with a pitch of 100 μ m and slat angle of 60°, can also raise the efficiency of this cell to 18.6% (Figure 2-7). Such surface texturing can be achieved with a dicing machine [21,22] or laser grooving [23]. A combination of reduced BSRV and front surface texturing can produce 19.5% efficient cells (case h). It should be noted that the Al treatment on the back leaves a roughened surface which may be difficult to passivate to the degree that can give a BSRV of 500 cm/sec, unless point contact Al diffusion is used. Finally, a combination of texturing, reduced BSRV, and increase in lifetime up to 100 μ sec can raise the efficiency of the cell to 21% (case i). Because of the reduced BSRV, an increase in lifetime from 25 to 100 μ sec has a higher effect on efficiency. Attempts are now being made to attain these design features on multicrystalline cells. There could be some inaccuracies in the absolute values of the calculated cell parameters due to certain assumptions; nevertheless, such model calculations provide useful guidelines for achieving greater than 20% efficient multicrystalline silicon cells.

Figure 2-7. The effects of lifetime and surface texturing on multicrystalline cell performance.

2.5 Mechanical Texturing of Multicrystalline Materials

It was shown in the previous sections that multicrystalline silicon solar cells with efficiencies of more than 17% have been fabricated on cast material. These results are attained by the improvement in casting technology and in the cell fabrication process. Crystallographic texturing of the cell surface, using anisotropic alkaline etching, has been used successfully to improve single crystalline cell performance. However, the overall spectral reflectance for multicrystalline substrate after anisotropic alkaline etching is not as good because the substrate has grains with different crystal orientations. For the purpose of reducing the surface reflectance and introducing light trapping in multicrystalline silicon solar cells, several investigators are using dicing machines for mechanical grooving of multicrystalline silicon substrate.

In order to study the effects of mechanical grooving on solar cell performance, we sent five Osaka Titanium Co. (OTC) wafers ($10 \times 10 \text{ cm}^2$) to Konstanz University in Germany for mechanical grooving with $100 \mu\text{m}$ pitch and $80 \mu\text{m}$ height (slat angle of 60°). In January 1993, we received seven $5 \times 5 \text{ cm}^2$ wafers. Figure 2-8 shows a cross-section scanning electron micrograph of the V-grooved surface. Measured hemispherical reflectance of these grooved wafers is shown in Figure 2-9.

We evaporated a double layer ZnS/MgF_2 AR coating on the grooved wafers and measured the reflectance. Figure 2-10 shows a comparison of the measured total hemispherical reflectance of the uncoated flat multicrystalline

silicon (back surface of the grooved wafers), uncoated grooved-multicrystalline silicon, and double layer AR coated grooved-multicrystalline silicon. The data clearly shows a significant reduction in the reflectance due to such mechanical grooving. In order to model these measured results we used the **TEXTURE** program, developed at Georgia Tech, to simulate the performance of the AR coated grooved-multicrystalline silicon wafers. Figure 2-11 shows that the measured and calculated reflectance are in the good agreement. Initial attempts to fabricate cells on these wafers did not succeed because it is practically impossible to form contacts by photolithography on wafers with such tall grooves.

Figure 2-8. SEM micrograph showing a cross section of the mechanically V-grooved surface on multicrystalline silicon.

Figure 2-9. Hemispherical reflectance for an uncoated V-grooved surface measured at the University of Konstanz, Germany.

Figure 2-10. Hemispherical reflectance measurements for a) flat, b) mechanically grooved, and c) grooved with ZnS/MgF₂ AR coating. All on multicrystalline silicon.

Figure 2-11. Comparison of measured reflectance vs. calculated reflectance using TEXTURE a model used for the design and analysis of light trapping structures.

2.6 Comparison of Different Multicrystalline Materials

For this study, 1cm X 1cm solar cells were processed on multicrystalline substrates from different vendors. The materials processed were Osaka Titanium conventional poly, Osaka Titanium electromagnetic grown poly, EFG ribbon material, Crystal Systems HEM grown poly, and poly material from Solarex.

These cells were processed using the optimized process discussed earlier. This process consists of a phosphorus diffusion using solid sources at 930°C for 25 minutes. This yields an emitter sheet resistance of 16-18 $\Omega/\square$. Because heavy doping in the emitter region can be an area of high recombination, the emitter was etched back using a $\text{HNO}_3:\text{HF}:\text{H}_2\text{O}$ [1000:1:100] etch. The target sheet resistivity for this run was approximately 60-70 $\Omega/\square$. An aluminum back surface field was formed by thermal evaporation a 1-1.5 μm aluminum layer on the back. The wafers were inserted into a diffusion furnace at 850°C. Initially, the wafers were inserted into an oxygen ambient to facilitate the growth of $\sim 100 \text{ \AA}$ passivating oxide on the surface of the n^+ emitter. After approximately 5 min of oxide growth the gas ambient was switched to nitrogen for an additional 30 minute aluminum drive-in. The furnace temperature was then ramped down to 400°C, and forming gas switched on. The front grid contact was formed by defining the grid configuration in photoresist, removing the oxide from the grid areas with a BOE, etchant and evaporating a Titanium/Silver layer over the wafer surface. The back contact was formed by evaporating Ti then

Silver on top of the Al/Si alloy at the surface of the Back Surface Field. Approximately 5 μm of additional silver was plated on both the front pattern and the back contacts. The contacts were then annealed in forming gas at 400°C for 20 minutes. A mesa was etched around each cell on the wafer to isolate each of the devices. Finally, a 550Å ZnS/1100Å MgF₂ double layer AR coating was deposited by thermal evaporation on the cells. All cells were characterized by light and dark I-V as well as internal quantum efficiency measurements.

Light and dark I-V data for three cells from each of the material types are shown in Table 2-7. In general, the data indicates that the Osaka conventional poly typically yields higher efficiencies followed by HEM, Solarex, Osaka electromagnetic and then EFG. The reason for the differences in efficiencies is clearly illustrated in Figure 2-12, which contains graphs of the internal quantum efficiency (IQE) along with the I-V data for the best cell from each wafer. As the cells decrease in efficiency there is also a decrease in the red response for the cells IQE. This red response reflects a decrease in bulk lifetime and diffusion length. EFG, Osaka electromagnetic and Solarex materials also demonstrate suppressed blue response. It is possible that this suppressed blue response may be due to uneven etch-back and a lower sheet resistivity.

IQE of the Crystal systems HEM material tracks well with the Osaka material except at the longer wavelengths, and the current density of the best HEM cell nearly matches the best Osaka cell. Based on the I-V and IQE data, it

appears that the only thing holding back the efficiency of the HEM cell relative to the Osaka cell is its lower V_{oc} . This lower V_{oc} may be due to lighter base doping. Lowering the base resistivity of this material without degrading the bulk lifetime may result in devices with efficiencies approaching those achieved with Osaka Titanium material.

Table 2-7. Light and dark I-V characteristics for cells processed on different multicrystalline materials. All with ZnS/MgF₂ AR coating.

HEM (JHEM-1)

Cell ID	R _s (Ω)	R _{sh} (KΩ)	V _{oc} (mV)	J _{sc} (mA/cm ²)	CFF	Eff.(%)	J ₀₁ (mA/cm ²)	J ₀₂ (mA/cm ²)
3	0.183	734	588.1	34.6	0.784	15.9	3.84x10 ⁻¹²	2.3x10 ⁻⁷
5	0.208	900	584.9	34.1	0.789	15.7	4.09x10 ⁻¹²	1.72x10 ⁻⁷
10	0.340	3183	587	33.9	0.782	15.6	3.42x10 ⁻¹²	1.68x10 ⁻⁷

Osaka EM (JOEM-1)

Cell ID	R _s (Ω)	R _{sh} (KΩ)	V _{oc} (mV)	J _{sc} (mA/cm ²)	CFF	Eff.(%)	J ₀₁ (mA/cm ²)	J ₀₂ (mA/cm ²)
2	0.357		588.5	32.6	0.766	14.7	3.26x10 ⁻¹²	2.0x10 ⁻⁷
4	0.194	596	590.5	32.9	0.772	15.0	3.18x10 ⁻¹²	1.9x10 ⁻⁷
5	0.288	29.4	582.2	32.3	0.764	14.4	3.84x10 ⁻¹²	1.46x10 ⁻⁷

Solarex (JSX-1)

Cell ID	R _s (Ω)	R _{sh} (KΩ)	V _{oc} (mV)	J _{sc} (mA/cm ²)	CFF	Eff.(%)	J ₀₁ (mA/cm ²)	J ₀₂ (mA/cm ²)
8	0.228	9505	607.1	32.7	0.795	15.8	1.59x10 ⁻¹²	2.17x10 ⁻⁷
9	0.244		604.3	31.9	0.784	15.1	1.81x10 ⁻¹²	2.47x10 ⁻⁷
10	0.307	594	591.1	30.3	0.777	13.9	2.75x10 ⁻¹²	1.52x10 ⁻⁷

EFG (2-5-1B)

Cell ID	R _s (Ω)	R _{sh} (KΩ)	V _{oc} (mV)	J _{sc} (mA/cm ²)	CFF	Eff.(%)	J ₀₁ (mA/cm ²)	J ₀₂ (mA/cm ²)
2	0.290	730	541.3	29.7	0.755	12.1	1.15x10 ⁻¹¹	9.23x10 ⁻⁸
3	0.295	683	549.0	30.0	0.762	12.6	1.04x10 ⁻¹¹	1.00x10 ⁻⁷
6	0.244	949	504.9	24.7	0.743	9.25	3.07x10 ⁻¹¹	1.35x10 ⁻⁷

Osaka Conv. (JOCT-2)

Cell ID	R _s (Ω)	R _{sh} (KΩ)	V _{oc} (mV)	J _{sc} (mA/cm ²)	CFF	Eff.(%)	J ₀₁ (mA/cm ²)	J ₀₂ (mA/cm ²)
3	0.300	990	615.1	34.6	0.775	16.5	1.38x10 ⁻¹²	3.84x10 ⁻⁷
8	0.303	1354	615.2	34.2	0.772	16.4	1.20x10 ⁻¹²	5.60x10 ⁻⁷
9	0.202	636	613.0	34.7	0.790	16.8	1.51x10 ⁻¹²	4.45x10 ⁻⁷

Cell	Voc	Jsc	CFF	Eff	J01	J02	Rs	Rsh
EFG1-3	549	30.0	.762	12.6	1.04E-11	1.00E-7	.295	683
JHEM1-3	588.1	34.6	.784	15.9	3.84E-12	2.30E-7	.183	744
JOCT2-9	613.0	34.7	.790	16.8	1.51E-12	4.45E-7	.202	636
JOEM1-4	590.5	32.9	.772	15.0	3.18E-12	1.9E-7	.194	596
JSX1-8	607.1	32.7	.795	15.8	1.59E-12	2.17E-7	.228	557

Figure 2-12. Plot of Internal Quantum Efficiency along with I-V data for the best cell from each of the materials tested.

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3.0 THE EFFECTS OF ALUMINUM TREATMENT AND FORMING GAS ANNEAL ON EFG SILICON SOLAR CELLS

3.1 Introduction

EFG is a very promising large grain multicrystalline sheet material which contains intragrain defects like dislocations, carbon, and impurities [1]. The average grain size of EFG is $\sim 0.5 \mu\text{m}$. EFG material is also known to respond quite favorably to hydrogen passivation by hydrogen implantation [2]. Since aluminum treatment is effective in gettering impurities, and it has been suggested that forming gas anneal in the presence of aluminum can generate atomic hydrogen that will act as a passivating agent [3], an attempt was made in this study to understand and quantify the role of aluminum gettering and forming gas anneal in upgrading the quality of EFG silicon. These steps were combined to achieve over 14% efficient EFG cells without any hydrogen implantation.

3.2 Experimental Work

3.2.1 Gettering, Oxide Passivation, and Forming Gas Anneal

In this study, phosphorus diffusion on the front and aluminum treatment on the back were used for gettering, which also form the n^+ -emitter and p^+ -back surface field, respectively. Thus, gettering is an integral, rather than additional, part of the cell process sequence. Phosphorus gettering was performed at 930°C for 25 minutes, using P_2O_5 solid source. In order to take

advantage of the intense phosphorus gettering without paying the penalty of heavy doping effects in the emitter, a controlled etch-back technique was used to partially etch the n^+ -region. This approach is similar to Narayanan et al. [4]. A $\text{HNO}_3\text{:HF:H}_2\text{O}$ [1000:1:100] etch for 20 min. was used to increase the emitter sheet resistance from $16 \Omega/\square$ to $80 \Omega/\square$.

Aluminum gettering was performed by evaporating $1 \mu\text{m}$ thick Al on the back of the cells followed by a high temperature drive-in for 35 minutes. Oxide passivation was done during the Al drive-in to simplify and maintain the cost effectiveness of the process sequence. In order to understand the effects of Al treatment and the importance of forming gas anneal, $1\text{cm} \times 1\text{cm}$ cells were fabricated with only half the back of the EFG material covered with Al. Thus, only half the EFG cells have Al BSF, and the other half experience the same high temperature cycle without the Al diffusion on the back. The former are referred to as Al-diffused cells while the latter, which do not have Al BSF, but only Al back contact sintered at 400°C , will be called sintered cells in this paper. For Al-sintered cells, the 850°C anneal was still carried out even when there was no Al on the back in order to give cells an equivalent high temperature thermal treatment. After the Al evaporation on half of the back of the EFG material, samples were inserted at 850°C in the oxygen ambient to first grow $\sim 100 \text{ \AA}$ thick oxide on top of the n^+ emitter region. After 5 minutes of oxide growth, gas ambient was switched to nitrogen for an additional 30 minute Al drive-in. In some instances, cells were fabricated without the 5 min.

oxidation to quantify the merit of oxide passivation on EFG cells. In order to understand and study the effect of forming gas anneal (FGA) on EFG cells, after the 850°C aluminum diffusion the temperature was ramped down to 400°C in nitrogen and then the cells were annealed for an additional two hours in nitrogen or forming gas ambient at 400°C. This was followed by a second Al deposition and 400°C/45 minutes sintering in nitrogen or forming gas for the ohmic back contact formation. Notice that one set of samples went through the forming gas anneal and the other set went through the nitrogen anneal in order to assess the importance and impact of forming gas ambient, which contained 10% hydrogen. This experimental strategy resulted in a matrix of cells with and without aluminum diffusion, oxide passivation, and forming gas anneal. Nine different EFG cells were fabricated, and the process sequence is summarized in Figure 3-1.

3.2.2 Fabrication of High Efficiency EFG Solar Cells

High efficiency n^+p-p^+ EFG solar cells were fabricated using the aluminum and phosphorus gettering, oxide passivation, forming gas anneal, and an evaporated double layer ZnS/MgF₂ antireflection coating. First, 30-40 μm Si was removed from each side by a chemical etch. After the chemical polishing, the substrate thickness was about $\sim 300 \mu\text{m}$. The emitter region was formed by 930°C/25 min phosphorus diffusion followed by an etch-back to 80 $\Omega/\square$. Then, as explained in section 3.2.1, the 850°C oxide passivation and

Al diffusion were performed. The front grid contact was formed by evaporation of Titanium/Silver (600 Å/600 Å), a lift-off technique, followed by 5 µm silver plating. The back contact was formed by evaporating titanium and silver on the top of the Al Back Surface Field (BSF) contact region. Contacts were annealed in either nitrogen or forming gas ambient for 30 minutes at 400°C. Finally, a 550 Å ZnS/1100 Å MgF₂ double layer AR coating was deposited by thermal evaporation on the cells. All the cells were characterized by light and dark I-V measurements, Open Circuit voltage Decay (OCD) lifetime measurements, spectral response, hemispherical reflectance and Internal Quantum Efficiency (IQE) measurements. Dark I-V data was also taken and analyzed by a double exponential model [5] to determine the reverse saturation current (J_{01}), junction recombination current (J_{02}), and series and shunt resistances.

Figure 3-1. Process sequence of nine cells to decouple the effects of oxide passivation, Al treatment, and FGA.

3.3 Results and Discussion

Figure 3-2 shows that a combination of oxide passivation, Al gettering, and forming gas anneal raised the EFG cell efficiency from 7.8% to 14.1% (verified by NREL) with V_{oc} of 569 mV and J_{sc} of 31.9 mA/cm². The IQE measurements in Figure 3-3 show that there was a very significant increase in the short and long wavelength response of the 14.1% efficient EFG cell compared to the 7.8% cell. Following sections contain detailed analysis of these cells to explain, decouple, and quantify the improvements due to gettering and passivation associated with oxide passivation, Al treatment, and forming gas anneal.

3.3.1 Effect of Oxide Passivation on EFG Cells

Figure 3-2 shows that oxide passivation alone raised the EFG cell efficiency from 7.8% to 8.6% (cells 5 and 6). Table 3-1 shows a comparison of Al-sintered as well as Al-diffused cells fabricated with and without oxide passivation. Oxide passivation was found to be quite beneficial for the EFG silicon cells. Similar trends were observed for the sintered and Al-diffused cells. In each case, the oxide passivation effect leads to essentially the same change in cell performance regardless of the change in bulk material properties produced by the Al process: an efficiency increase of 0.8% (absolute); a decrease in J_{01} by a factor of 1.2; and an increase in the blue response. For example, the IQE response of cells 5 and 6 in Figure 3-3 shows that the front

oxide passivation of EFG cells increases the short wavelength response and J_{sc} by 1.7 mA/cm^2 , while the dark I-V analysis in Table 3-1 reveals a reduction in J_{01} by a factor of 1.2. This combination of increased J_{sc} and reduced J_{01} should result in an increase of $\sim 7 \text{ mV}$ in V_{oc} because $V_{oc} = kT/q \cdot \ln(J_{sc}/J_0 + 1)$. This agrees fairly well with the observed increase of 5 mV in V_{oc} . As expected, oxide passivation does not change the bulk diffusion length (Table 3-1 and Figure 3-2), but it only improves front surface recombination velocity. Figure 3-3 shows that the oxide passivation can improve the short wavelength response further (cell 2), if 400°C forming gas anneal is used after the oxide passivation. This is because forming gas anneal passivates the dangling Si bonds at the Si/SiO₂ interface.

Oxide passivation showed slightly larger improvements for cast multicrystalline silicon cells (16 mV in V_{oc} and 1.1% in absolute cell efficiency) [7]. This is probably because EFG cells have somewhat lower bulk lifetime and, therefore, $J_0 (J_{0b} + J_{0e})$ is dominated by J_{0b} and the front oxide passivation, which lowers J_{0e} , and does not influence J_0 as much.

Figure 3-2. The effects of different treatments on the performance of the EFG cells.

Figure 3-3. The effects of various treatments on IQE of the EFG cells.

Table 3-1. Effects of Emitter Oxide Passivation on Nitrogen Annealed* EFG Cells

Cell ID	Forming Gas	Oxide Pass.	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Eff. (%)	Lifetime (μ sec)	R_{series} (Ω -cm ²)	R_{shunt} (K Ω -cm ²)	J_{01} (A/cm ²)	J_{02} (A/cm ²)	L (μ m)
Alsintered	No	No	20.8	520	0.718	7.8	3	0.55	700	3.51×10^{-11}	3.16×10^{-7}	57
Al-sintered	No	Yes	22.5	525	0.732	8.6	5	0.59	54	2.91×10^{-11}	3.83×10^{-7}	67
Al-diffused	No	No	22.6	531	0.756	9.1	5	0.42	72	2.84×10^{-11}	2.85×10^{-7}	110
Al-diffused	No	Yes	24.5	536	0.762	10.0	12	0.49	370	2.36×10^{-11}	1.48×10^{-7}	134

3.3.2 Beneficial Effects of Al Treatment

Figure 3-2 shows that the oxide passivation raised the EFG cell efficiency from 7.8% to 8.6%, which went up to 10% as a result of the Al treatment (cells 5, 6, and 2). A comparison of all four kinds of Al-diffused and sintered cells in Tables 3-2a and 3-2b clearly shows that the Al diffusion process produces about 1.4% increase in absolute cell efficiency, regardless of oxide passivation and forming gas anneal. This indicates that the effect of Al treatment is complimentary to oxide passivation and forming gas anneal. Detailed analysis of the cells in Tables 3-2a and 3-2b reveals that Al process-induced improvement in EFG cell efficiency is associated with 10-20 mV increase in V_{oc} and 1.8-2.0 mA/cm² increase in J_{sc} . The IQE response of cells 2 and 6 in Figure 3-3 supports the significant increase in diffusion length from 67 μ m to 134 μ m due to the Al treatment. Al alloying process introduces pitting/damage on the surface which can provide a sink for gettering impurities and defects, and accounts for the increase in IQE and bulk diffusion length.

A similar study on Osaka Titanium cast multicrystalline silicon showed about 1 mA/cm² improvement in J_{sc} and 10 mV increase in V_{oc} , indicating that Al gettering is very effective for multicrystalline silicon cells in general, and is relatively more beneficial for the EFG cells than the cast multicrystalline silicon cells. This is probably because there are more defects and impurities to be getterred in EFG material.

Table 3-2a. Al-Diffused EFG Multicrystalline Silicon Cells

Cell ID	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Eff. (%)	Lifetime (μsec)	R_{series} (Ω-cm ²)	R_{shunt} (KΩ-cm ²)	J_{01} (A/cm ²)	J_{02} (A/cm ²)	L (μm)
1 No Oxide Passivation + Nitrogen Anneal	22.6	531	0.75 6	9.1	5	0.42	72	2.84×10^{-11}	2.85×10^{-7}	110
2. Oxide Passivation + Nitrogen Anneal	24.5	536	0.76 2	10.0	12	0.49	370	2.36×10^{-11}	1.48×10^{-7}	134
3 No Oxide Passivation + Forming Gas	30.4	566	0.77 3	13.3	17	0.44	211	1.63×10^{-11}	1.17×10^{-7}	174
4. Oxide Passivation + Forming Gas	31.9	569	0.78 0	14.1	16	0.44	244	1.23×10^{-11}	1.10×10^{-7}	187

Table 3-2b Al-Sintered EFG Multicrystalline Silicon Cells

Cell ID	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Eff. (%)	Lifetime (μ sec)	R_{series} (Ω -cm ²)	R_{shunt} (K Ω - cm ²)	J_{01} (A/cm ²)	J_{02} (A/cm ²)	L (μ m)
5 No Oxide Passivation + Nitrogen Anneal	20.8	520	0.71 8	7.8	3	0.55	700	3.51×10^{-11}	3.16×10^{-7}	57
6. Oxide Passivation + Nitrogen Anneal	22.5	525	0.73 2	8.6	5	0.59	54	2.91×10^{-11}	3.83×10^{-7}	67
7 No Oxide Passivation + Forming Gas	28.4	548	0.75 5	11.7	14	0.48	456	2.20×10^{-11}	2.81×10^{-7}	149
8. Oxide Passivation + Forming Gas	30.0	550	0.75 2	12.4	14	0.42	1420	1.98×10^{-11}	2.73×10^{-7}	168

3.3.3 Effects of Forming Gas Anneal on EFG Cells

Defect passivation by hydrogenation has been well established [8]. Several production-compatible approaches for hydrogenation have been investigated in the past [8-12], but the exact mechanism for defect passivation and hydrogen diffusion in silicon is still not fully understood. For example, it is accepted that hydrogen passivates dangling bonds associated with the defects, but there appear to be other mechanisms related to hydrogen-induced defect passivation, particularly when defects are accompanied by impurity segregation at the defect sites [9,13]. It has been observed that the degree of hydrogen-induced improvement in cell performance depends on the defect structure and, perhaps, on other impurities present in the substrate. Hydrogen atoms can interact with impurities (oxygen, carbon, metals), segregated or precipitated at extended defects [9,13]. Hydrogenation produces damage when it is done by ion implantation or by RF plasma; others have shown that deposition of Si_3N_4 layer by PECVD in an ambient containing hydrogen can be very efficient for defect passivation [10]. It has been suggested that forming gas anneal at 400°C in the presence of aluminum can generate atomic hydrogen [11,12]. This process is highly compatible and inexpensive for solar cell fabrication and is routinely used successfully in MOS devices to reduce the Si-SiO_2 interface density [11]. The real question is whether enough atomic hydrogen can be generated and transported deep into the bulk of multicrystalline silicon materials to be effective for bulk defect passivation.

Therefore, we decided to investigate this process, and selected the EFG material because it responds quite favorably to hydrogenation [4].

Figure 3-2 showed that oxide passivation raised the EFG cell efficiency from 7.8% to 8.6%, Al gettering increased that value to 10%, and the forming gas anneal raised it from 10% to 14.1% (cells 2 and 4). IQE response of cells 2 and 4 in Figure 3-3 shows a very significant increase in the short and the long wavelength response due to forming gas treatment. This indicates that the use of forming gas not only provides better oxide passivation to improve the short wavelength response, but also passivates bulk defects to improve the long wavelength response. The cell analysis in Table 3-2a and 3-2b shows an increase in diffusion length from 134 μm to 187 μm along with 7.4 mA/cm^2 increase in J_{sc} , and a factor of 1.9 decrease in J_{01} .

The observed forming gas-induced effect on cell performance and IQE are similar to what is generally observed in EFG cells after intentional hydrogen implantation. In our process sequence, forming gas anneal was performed at 400°C for 2 hrs after the Al drive-in. It is possible that the interaction between remaining Al or Al/Si layer with the 10% H_2 in the forming gas resulted in generation of atomic hydrogen, which can passivate bulk defects. In order to test this hypothesis, two kinds of Al-sintered cells were fabricated. One went through 400°C/2 hrs FGA while the other one was subjected to 400°C/2hrs N_2 anneal (Table 3-3 and Figure 3-1). Notice that there is no forming gas/Al interaction in this experiment. The IQE response (Figure 3-4) and cell data

(Table 3-3) show that FGA alone, without any help from Al, is capable of giving 2.6% improvement in IQE response via defect passivation. Exact mechanism for dissociation of H_2 molecule in the absence of Al is not understood at this time. One possibility is that the free electrons in the n^+ emitter region may contribute to the splitting of H_2 molecules [3]. It is also noteworthy that the forming gas anneal of the Al-diffused cells gave 4.1% improvement compared to 2.6% increase in efficiency of the Al-sintered cells. This suggests that the interaction of forming gas with Al or Al/Si layer on the back also generates additional atomic hydrogen to promote defect passivation and enhance bulk diffusion length. Thus, forming gas anneal may be able to inject atomic hydrogen into the bulk from both n^+ and p^+ /Al surface via interaction with free electrons.

In contrast to EFG cells, the forming gas treatment had virtually no effect on the OTC cast multicrystalline silicon cells (Table 3-4). This is probably because this cast multicrystalline silicon material does not have those defects that can be passivated by hydrogenation and contribute to significant increase in bulk lifetime and cell performance.

Figure 3-4. The effect of FGA on the performance of the EFG cells.

Table 3-3. Effects of Anneal Stage on EFG Cells

Cell ID	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Eff. (%)	Lifetime (μsec)	R_{series} (Ω-cm ²)	R_{shunt} (KΩ-cm ²)	J_{01} (A/cm ²)	J_{02} (A/cm ²)	L (μm)
9. Al-sint. + With FGA	27.5	540	0.756	11. 2	11	0.41	342	2.45x10 ⁻¹¹	3.20x10 ⁻⁷	120
6. Al-sint. + No FGA	22.5	525	0.732	8.6	5	0.59	54	2.91x10 ⁻¹¹	3.83x10 ⁻⁷	67

Table 3-4. Effects of Forming Gas Anneal on Al-Diffused OTC Cast Multicrystalline Silicon Cells

Cell ID	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF	Eff. (%)	Lifetime (μsec)	R_{series} (Ω-cm ²)	R_{shunt} (KΩ-cm ²)	J_{01} (A/cm ²)	J_{02} (A/cm ²)
No Oxide Passivation + Nitrogen Anneal	34.4	606	0.715	14.9	23	0.37	342	1.69x10 ⁻¹¹	9.37x10 ⁻⁷
No Oxide Passivation + Forming Gas	34.1	600	0.727	14.9	19	0.39	1420	2.53x10 ⁻¹¹	9.56x10 ⁻⁷

3.4 Conclusions

This study shows for the first time that Al treatment on the back, oxide passivation on the front, and 400°C forming gas anneal can raise the EFG cell efficiency from 7.8% to 14.1% which is comparable to some of the highest efficiency EFG cells fabricated by intentional hydrogen implantation. These techniques are frequently used and are highly compatible with cell fabrication. Growth of a 100 Å passivating oxide on top of the emitter resulted in ~0.8% increase in EFG cell efficiency which is associated with increase in blue response, 1.7 mA/cm² increase in J_{sc} and a reduction in J_{01} by a factor of 1.2. Aluminum diffusion at 850°C alone on the back side increased the EFG cell efficiency by 1.4% (absolute) which is associated with 67 μm increase in diffusion length due to Al process-induced gettering. Finally, forming gas anneal at 400°C, after the aluminum diffusion, improved the absolute efficiency by 4.1% which is associated with an additional 53 μm increase in diffusion length, 7.4 mA/cm² increase in J_{sc} , and reduction in J_{01} by a factor of 1.9. A combination of the above three steps improved the EFG cell efficiency by 6.3% (absolute), suggesting that these effects are complimentary.

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4.0 FABRICATION AND MODELING OF HIGH EFFICIENCY MONOCRYSTALLINE SILICON

4.1 Crystalline Silicon for Photovoltaic; Opportunities and Challenges

4.1.1 Introduction

Low-cost, high-efficiency solar cells are the key to large scale applicability of photovoltaic (PV) systems. The cost of PV modules need to decrease by about a factor of 5 to \$1/watt in order to realize the goal of producing electricity at 6-8¢/KWhr from PV. This goal can be achieved by various combinations of module cost and efficiency. That is why research is being conducted on various PV materials that can produce efficiencies in the range of 10-35% at various costs. Crystalline silicon is the most promising and mature candidate today for terrestrial PV applications. Silicon offers several advantages relative to other PV materials, including abundance, established technology base, high quality, and good surface passivation characteristics. The obvious disadvantages compared to other PV materials are the indirect bandgap and current high processing costs for silicon material and devices.

In the last six years, one-sun single crystal cell efficiencies have increased from 19% to 23%, while the multicrystalline silicon cell efficiencies have risen from 14% to 17.7%. In spite of this progress, considerable research opportunities and gap exist between the current and practically achievable cell efficiencies which are estimated to be in the range of 25-27% for single crystal and 20-22% for multicrystalline silicon. The objective of this section is two

fold: (a) to address near term research and development opportunities by identifying important silicon material problems that lack fundamental understanding; and (b) to point out some innovative research opportunities involving new materials and techniques.

4.1.2 Material Specification for High Efficiency Silicon Cells

Device considerations and performance are the ultimate judge of material quality. Therefore, before discussing the research opportunities in silicon, selected model calculations were performed to specify various combinations of resistivity, minority carrier lifetime, surface texturing, and surface recombination velocity to bridge the gap between current and practically achievable silicon cell efficiencies. All other silicon material parameters, such as mobility, diffusivity, absorption, bandgap narrowing, intrinsic recombination coefficients etc, are well known and were kept constant in these calculations. Figure 4-1 shows that if silicon was perfect, 100% light trapping was possible, and zero surface recombination velocity (S) was achievable, then 200 μm thick $n^+ - p - p^+$ silicon cell efficiencies in excess of 27% could be achieved on any resistivity silicon with resistivity greater than 0.2 $\Omega\text{-cm}$. In Figure 4-2, lifetime at each resistivity is dictated by intrinsic recombination mechanisms. If we take a step back and replace the perfect light trapping by the best achieved light trapping today using inverted pyramids [1], then efficiencies approaching 26% can be achieved (Figure 4-1). If we take another step back and allow the lifetime to be dictated

by Shockley-Read-Hall (SRH) mechanisms along with finite S values, then efficiencies can range anywhere from 5%-25% depending on the lifetime and resistivity (Figure 4-2). Finally, if we take one more step and allow S to be greater than zero, in conjunction with 2 Ω -cm/10 msec lifetime base and inverted pyramid light trapping, then $> 25\%$ cells can be achieved only when $S < 100$ cm/sec (Figure 4-3). Using the best reported lifetime value of ~ 2 msec on 2 Ω -cm base, and $S = 500$ cm/sec, inverted pyramid cell efficiency of $\sim 24\%$ can be achieved, which is close to the best reported one sun silicon cell efficiency of 23.3% [1] today. Thus in order to go beyond 25% efficiencies we need to increase the bulk lifetime, lower the surface recombination velocity, and improve the light trapping. The following sections provide guidelines for achieving these goals.

4.1.3 Light Trapping in Silicon

Figure 4-1 shows that without any light trapping, n^+ -p- p^+ flat cells cannot reach 25% efficiency even if the material and surfaces are perfect. We have developed a light trapping model and analyzed various combinations of the front and back textures on a 100 μ m thick cell to point out research opportunities in this area. Model calculations show that in order to go beyond the inverted pyramid/flat texturing, we need to explore Lambertian random texturing, three perpendicular planar (3PP) geometry, perpendicular slats, and tilted pyramid [1].

4.1.4 Surface Recombination Velocity

In order to achieve silicon cell efficiencies beyond 25%, it is necessary to reduce carrier recombination as much as possible in conjunction with light trapping. In the early cell designs, recombination in the bulk silicon and contacts dominated the performance. These effects have been reduced to a large extent by much improved bulk silicon quality, optimized doping profiles and reduced contact coverage. Recombination in the record high silicon cells (23.3%) today is largely dominated by the surfaces. Even though silicon has been blessed with SiO_2 for surface passivation, further efficiency gains will rely on better or improved surface passivation techniques. Several investigators have shown that S can be reduced below 10 cm/sec by growing a thermal oxide on a nondiffused silicon surface. However, there is some evidence that various environmental stresses, including uv exposure, can degrade the effectiveness of surface passivation and raise the S value above 100 cm/sec [2]. Figure 4-3 shows that this phenomenon would significantly reduce the cell performance. Some investigators now used passivated diffused regions to avoid this instability problem by paying a price in the cell efficiency up front. This area needs to be investigated further otherwise when we get to greater than 25% efficient one sun silicon cells, they will not be stable.

4.1.5 Bulk Lifetime in Silicon

This area needs the most attention and better fundamental understanding. Figure 4-4 shows that in spite of orders of magnitude improvement in lifetime in silicon in the last decade, lifetime in silicon still falls well short of the theoretical intrinsic limit at doping concentrations below $5 \times 10^{17} \text{ cm}^{-3}$. The exact reason for this discrepancy is not fully understood. The effect of oxygen, carbon, transition metals, dopants and point defects is suspected, but not established in the best silicon materials available today. This is partially because most of the existing techniques fail to detect recombination centers in silicon when the lifetime exceeds $100 \mu\text{sec}$. There is a need to identify the exact source of lifetime problems in silicon and develop better gettering and passivation techniques to remove or deactivate them. Some specific research opportunities in this area are discussed below.

Figure 4-1. Importance of light trapping in high efficiency silicon solar cells.

Figure 4-2. Effect of resistivity and lifetime on efficiency of inverted pyramid cells.

Figure 4-3. Importance of surface recombination velocity on high efficiency inverted pyramid cells.

Figure 4.4. Lack of understanding and scatter in minority carrier lifetime in silicon.

4.1.5.1 Effect of Oxygen on Lifetime in Silicon

All the record high efficiency single crystal cells to date have been fabricated on FZ silicon while the crucible grown CZ silicon cell efficiencies are still 2-3% (absolute) the FZ cells. This is because CZ silicon, for reasons not fully understood, suffers from low lifetime, especially during the high temperature processing. Since FZ has very low oxygen (< 0.2 ppm) and CZ contains ~ 15 ppm O_2 , it is generally concluded that O_2 is the culprit, but exactly how it degrades the lifetime is not fully understood. The Literature is full of qualitative and speculative models, such as oxygen precipitates, oxygen-impurity complexes, and oxygen-defect interactions to explain the harmful effect of oxygen. In an attempt to understand the role of oxygen, we recently conducted a study [3-5] involving MCZ silicon with a controlled amount of oxygen, and showed that (a) crucible grown MCZ silicon has a much higher lifetime than CZ before and after processing even with comparable O_2 ; (b) O_2 in the as-grown MCZ does not degrade lifetime, but it does make lifetime somewhat sensitive to process induced degradations (c) MCZ silicon can have a lifetime comparable to FZ, even after processing and; (d) lifetime in the range of 1-6 msec can be achieved in the processed MCZ. This study strongly recommends the use of MCZ silicon for PV, but the question still remains why the cheaper CZ silicon today is not good enough for $< 20\%$ efficient cells.

Contrary to the general belief in the single crystal silicon, some investigators [3-5] have shown that moderate amount of oxygen (< 10 ppm)

in some multicrystalline silicon materials like EFG can actually improve the bulk lifetime either by passivating some defects or by enhancing the effectiveness of defect passivation by hydrogen in these materials. These topics urgently need fundamental research.

4.1.5.2 Effect of Dopants on Lifetime in Silicon

Similar to oxygen, the undesirable effect of dopants on the lifetime in silicon is suspected but not fully understood. SRH lifetime is generally found to decrease at higher doping concentrations. There are two possible reasons for this: either the shallow traps control the lifetime [7], or dopants are directly involved in the formation of lifetime killers [6]. It is not clear which is the case. We showed that if a shallow trap, such as Ti, Cr or divacancy, dominates the lifetime in a given silicon material, then the lifetime will drop more rapidly with increased doping, resulting in lower efficiency cells [7]. If the dopants are involved in defect formation, such as B-Fe pair and B-O-V complexes, not only the cell efficiency will decrease with doping, but the optimum resistivity will shift to a higher level [6]. We point out that this may be the reason why for conventional cell designs, single crystal silicon cell efficiency peaks at $\sim 0.2 \Omega\text{-cm}$ while multicrystalline silicon efficiency peaks anywhere in the range of $0.8\text{-}5 \Omega\text{-cm}$, depending on the degree of dopant-defect interaction [6]. It is possible that there is some dopant-defect interaction even in the widely used $0.2 \Omega\text{-cm}$ FZ silicon because the measured lifetimes are generally of the order of 20-50

μsec as opposed to $\sim 1 \text{ msec}$, expected from the intrinsic recombination mechanisms. Identification and elimination of such defects will allow us to achieve very high efficiency cells on low-resistivity and relatively low-lifetime silicon instead of going for high-resistivity silicon with very high-lifetime (Figure 4.3). This will relax the processing constraints because it is hard to maintain such high lifetimes during the cell processing. Fundamental understanding of the role of dopants on lifetime may also help in reducing the gap between single and multicrystalline silicon cell efficiencies. This area offers a real opportunity for much needed fundamental research which will greatly help the yield and performance of low resistivity single and multicrystalline silicon cells.

4.1.5.3 Effect of Transition Metals on Lifetime in Silicon

Transition metal impurities are generally present in most starting silicon PV materials, and can also be introduced during device processing. These impurities form deep levels and cause lifetime degradation. Thus, there is a real need to understand the behavior of transition metals in silicon and develop efficient gettering methods to move them to a level where they are no longer a factor in limiting lifetime. A detailed study [8] conducted at Westinghouse showed that 14% efficient cells can be achieved on 4 ohm-cm silicon with 10 μs lifetime provided transition metal content did not exceed 10^{10} - 10^{16} cm^{-3} range. However, the most harmful impurities, such as Ti, Mo, V and Cr, need to be below a concentration level of 10^{12} cm^{-3} even for the 14% cells. The

threshold impurity content can be calculated from this study if much higher lifetimes or cell efficiencies are desired [8]. For greater than 2 ms lifetime, which may be required to achieve > 25% efficient cells (Figure 4-1), the extrapolation scheme suggested in ref. 8 reduces the allowable impurity content in the range of 10^{17} - 10^{13} cm⁻³ with most of the detrimental impurities well below a level 10^9 cm⁻³. This puts a lot of constraints on the crystal growth and cell fabrication technology and emphasizes the need for gettering/passivation studies and fundamental understanding of impurity diffusions, precipitation, lattice site occupancy, and interaction with other point-defects in silicon.

4.1.6 Silicon Crystal Growth

Most high efficiency cells to date have been made on FZ silicon because it not only gives higher lifetime but, is also more forgiving during the thermal processing. Crucible grown CZ material, which can be grown in large diameters and is readily available, has more impurities and defects and gives more than 3% (absolute) lower cell efficiency than the FZ silicon. The General perception is that FZ is more expensive than CZ, and may not be cost-effective for PV. However, another school of thought is that FZ crystals are not necessarily more expensive than CZ. Given the large number of processing steps involved in going from semiconductor grade Si to solar array, a small difference in cost between FZ and CZ is likely to be even less important, because FZ gives higher efficiency cells. Some investigators [9] argue that, in principle, it should be

possible to make the cost of FZ much lower because of faster growth speeds, fewer consumables, and no crucible cost. However, this will require research to improve better one-pass yield, a simplified and improved growth apparatus and tighter control. Recent investigations [5] have shown that crucible grown low oxygen (< 10 ppm) Magnetic Czochralski (MCZ) silicon can be an effective substitute for FZ, because lifetimes in excess of 5 ms can be maintained even after processing. More research on MCZ growth and cell fabrication needs to be done to evaluate if MCZ can be a cost-effective substitute for FZ without sacrificing the cell efficiency.

4.1.7 Porous Silicon for PV

Porous Silicon (PS) is an emerging material whose potential for PV has not yet been explored. PS was originally discovered in 1956 by Uhlir [10] and was recently rediscovered by Canham [11]. PS layers can be produced on crystalline silicon by electrochemical etching in HF solutions. The PS material is "sponge-like", containing randomly positioned holes. As the material is processed to increase the porosity to about 80%, a sparse network of columns is formed with nanometers to tens of nanometers diameter exhibiting both photoluminescence (PL) and electroluminescence (EL) with typical bandgap in the range of 1.5-2.0 eV. This has prompted some researchers to discard previously held biases against Si for use in optoelectronic applications. The mechanism for PL from PS has been subject of considerable debate. One school

of thought is that the presence of a-Si surface layer is the source of PL while others think that quantum confinement within the nanometers column is responsible. A partially direct and adjustable bandgap between 1.5-2.0 eV with random structure offers several potential promising applications in PV, including (a) formation of heterojunction silicon solar cell with relatively defect free homogeneous interface, (b) development of Si tandem solar cells with 1.7 eV bandgap PS cell on top of 1.1 eV bandgap Si cell, (c) surface texturing, and (d) surface passivation. The most promising near-term use of PS for PV may be the efficient light trapping, because very small nm scale size columns in PS approach the optimal light trapping geometry of Lambertian surface. PV texturing could be a real blessing for multicrystalline silicon cells because it is not easy and cost-effective to texture multicrystalline silicon surface by conventional methods. Gee et al. at Sandia National Labs have recently shown some preliminary data to confirm that PS layer can indeed reduce silicon surface reflectance. There are some major problems with PS because PL properties are not stable in oxygen or moisture containing environment; it is not easy to form heavily doped PS layers; and finally it is not clear whether PS can be treated as a true bulk material.

4.1.8 Subgap Absorption in Silicon by Defect Layer

Recently, Li et al. [12] reported 35% one sun silicon solar cell efficiency by creating a p-n junction near a localized defect layer (JNLD). This caught most

PV investigators by surprise, and there are still some concerns about the validity of measurements and physics behind the operating of this cell. A local defect layer (LDL) was formed at a depth of $0.6\text{ }\mu\text{m}$ below the silicon surface by 180 KeV proton bombardment with a dose of $3 \times 10^{16}\text{ H}^+/\text{cm}^2$, followed by $930^\circ\text{C}/10\text{ sec}$ rapid thermal anneal with $1180^\circ\text{C}/20\text{ min}$ furnace anneal. A $0.75\text{ }\mu\text{m}$ deep $\text{p}^+ \text{-n}$ junction was formed by boron diffusion at 900°C . The regions underneath the gridlines were not damaged to provide a lower resistivity path for carrier flow, instead of penetrating across the LDL.

The reported J_{sc} for the above cell was $69.1\text{ mA}/\text{cm}^2$ which is about $25\text{ mA}/\text{cm}^2$ larger than if all the photons in the AM 1.5 solar spectrum above the Si bandgap energy were absorbed and contributed to J_{sc} . Li et al. attributed such high currents to the subgap excitation processes, which involved electron-hole pair generation by IR photons via defect levels in the LDL layer. They have also shown a significant IR response of this cell beyond $1.5\text{ }\mu\text{m}$. We have made some preliminary model calculations assuming all the photons up to $3\text{ }\mu\text{m}$ absorbed in the LDL with 100 ns lifetime. If each photon contributed to one e-h pair, the J_{sc} can be about $72\text{ mA}/\text{cm}^2$ with V_{oc} of 687 mV and cell efficiency of 38%. However, if two or three photons in the wavelength beyond $1.2\text{ }\mu\text{m}$ create one e-h pair, which would be the case for subgap excitation, it is not possible to get $69\text{ mA}/\text{cm}^2$ current. Thus, the physics of this cell is not understood and should be looked at more carefully. Nevertheless, if the report experimental data is correct, then this approach offers tremendous opportunity

because efficiency of this cell should not depend on the base material quality and thickness. This could lead to super high efficiency cells on low-cost substrates.

4.1.9 Conclusions

In order to achieve one-sun silicon solar cell efficiencies beyond 25%, lifetime limiting defects and mechanisms need to be understood. The role of dopants, hydrogen, oxygen, and transition metals needs to be examined in both high quality single crystal silicon as well as multicrystalline silicon. The Development and understanding of defect passivation and gettering procedures is also important for yield and performance of high efficiency Si cells. An investigation of better light trapping geometries and stable surface passivation with $S < 100$ cm/sec will also be required to go beyond 25% efficiency. There are also some fundamental research opportunities in the area of exploiting subgap absorption in Si by defect layers. The use of wide gap porous silicon and microcrystalline silicon should also be explored for PV.

4.2 Practical Training Of Silicon Solar Cell Fabrication

An attempt was made to develop a process sequence which allows the fabrication of four kinds of cells in one run. Figure 4-5 shows the schematic diagram of the four types of cells and Tables 4-1 through 4-4 show the corresponding process flow chart. The four cell structures include: (a) simple base line cell (SBLC) with n^+ emitter, p^+ BSF and no surface texturing, (b) advanced base line cell (ABLC) with an additional deep n^+ diffusion underneath the grid lines and Al point contacts on the back, (c) textured base line cell (TBLC) with random pyramid texture on the front surface for light trapping, and (d) inverted pyramid base line cell (IBLC) with inverted pyramid texture on the front surface. Notice that the SBLC process requires only two masks, ABLC requires 4 masks, and TBLC and IBLC structures require 5 masks. Detailed process sequences for each cell are given in Appendix A. Such a training run is indeed quite ambitious, but we feel it will bring students up the speed quickly and provide them with solid foundation for high efficiency cell fabrication. A typical training run starts with 12 wafers involving three wafers for each four cell designs. Initial experience suggests that IBLC cells with five masks takes two to three weeks and has a low yield. More work is in progress to standardize the process and introduce more control. At present, SBLC cells efficiencies are about 18-19% while inverted pyramid cell efficiencies range from 19.5-21%.

Figure 4-5. Schematic diagram of the four types of cells that are fabricated in a training run.

Table 4-1. Process Sequence for Simple Base Line Cell (SBLC).

Step 1.	Sample Identification
Step 2.	Initial Sample Cleaning
Step 3.	Phosphorus Diffusion
Step 4.	Emitter Etch Back
Step 5.	Wafer Cleaning for Aluminum Treatment
Step 6.	Aluminum Evaporation on the Back Side
Step 7.	Aluminum Treatment
Step 8.	Lift-off for Front Metallization
Step 9.	Back Metallization
Step 10.	Silver Plating
Step 11.	Anneal
Step 12.	Mesa Etch
Step 13.	Test
Step 14.	AR Coating
Step 15.	Test

Table 4-2. Process Sequence for Advanced Base Line Cell (ABLC)

Step 1.	Sample Identification
Step 2.	Initial Sample Cleaning
Step 3.	Oxidation and Oxide Pattern
Step 4.	Grid Phosphorus Diffusion and Deglaze
Step 5.	Field Oxide Pattern
Step 6.	Field Phosphorus Diffusion and Deglaze
Step 7.	Passivation Oxide Growth
Step 8.	Oxide Pattern and Back Al Evaporation
Step 9.	Al Treatment
Step 10.	Lift-off for Front Metallization
Step 11.	Back Metallization
Step 12.	Silver Plating
Step 13.	Sinter
Step 14.	Test
Step 15.	AR Coating
Step 16.	Test

Table 4-3. Process Sequence for Texture Base Line Cell (TBLC).

Step 1.	Sample Identification
Step 2.	Initial Sample Cleaning
Step 3.	Oxidation and Oxide Pattern
Step 4.	Texture
Step 5.	Oxidation and Oxide Pattern
Step 6.	Grid Phosphorus Diffusion and Deglaze
Step 7.	Field Oxide Pattern
Step 8.	Field Phosphorus Diffusion and Deglaze
Step 9.	Passivation Oxide Growth
Step 10.	Oxide Pattern and Back Al Treatment
Step 11.	Lift-off for Front Metallization
Step 12.	Back Metallization
Step 13.	Silver Plating
Step 14.	Sinter
Step 15.	Test

Table 4-4. Process Sequence for Inverted Pyramid Base Line Cell (IBLC).

Step 1.	Sample Identification
Step 2.	Initial Sample Cleaning
Step 3.	Oxidation and Oxide Pattern
Step 4.	Inverted Pyramids
Step 5.	Oxidation and Oxide Pattern
Step 6.	Grid Phosphorus Diffusion and Deglaze
Step 7.	Field Oxide Pattern
Step 8.	Field Phosphorus Diffusion and Deglaze
Step 9.	Passivation Oxide Growth
Step 10.	Oxide Pattern and Back Al Treatment
Step 11.	Lift-off for Front Metallization
Step 12.	Back Metallization
Step 13.	Silver Plating
Step 14.	Sinter
Step 15.	Test

4.3 Fabrication and Analysis of High Efficiency One-Sun Single Crystal Silicon Solar Cells

This section summarizes inverted pyramid cell runs made on low resistivity (.2-.3 Ω -cm) FZ Wacker silicon. Table 4-5 shows the process sequence used to fabricate these cells while Figure 4-6 shows a schematic diagram of the cell structure. The light IV data of these cells are summarized Table 4-6. The cell efficiency of 19.8 % was obtained with V_{oc} of 658 mV and J_{sc} of 37.2 mA/cm². Figure 4-7 shows the surface reflectance and internal quantum efficiency (IQE) of these inverted pyramid cells with ZnS/MgF₂ or SiN/MgF₂ double layer anti reflective coatings (DLAR).

PC-1D model was used to match the IQE and cell parameters of these cells in an attempt to obtain guidelines for further improvements. Figure 4-8 shows a good match between the measured and calculated IQE with front and back surface recombination velocity of 1E4 cm/sec (FSRV = BSRV = 1E4 cm/sec), lifetime of 25 us and back surface reflectance (BSR) of 80%. High BSRV and low BSR were due to full Al alloyed back contact in these cells. The FSRV and J_o of the emitter were also too high because the diffusions were not optimized. Therefore, the next step was to optimize the n⁺ diffusion in order to reduce J_{oe} , and incorporate point contact Al on the back to reduce BSRV and increase BSR.

Table 4-5. Processing Sequence for Inverted Pyramid Solar Cells.

Step 1.	.2-.3 ohm-cm, FZ, p-type, 300 um thick
Step 2.	Oxide growth at 1050°C for 2 hr
Step 3.	Oxide patterning
Step 4.	Inverted pyramids KOH:H2O = 8:100 (w/v) at 70°C
Step 5.	Rounding the edges with HF:HN03 = 1:40
Step 6.	Oxide growth 1050°C 3 hr
Step 7.	Oxide patterning for N ⁺ phosphorous diffusion
Step 8.	Phosphorous diffusion 930°C 20min 15-20 Ω / $\square$
Step 9.	Deglaze HF:H2O = 1:20 for 2 min
Step 10.	Oxide growth 1050°C 2 hr
Step 11.	Oxide patterning for emitter diffusion
Step 12.	Phosphorous diffusion at 880°C for 20 min 80-100 Ω / $\square$
Step 13.	Deglaze HF:H2O = 1:20 for 2 min
Step 14.	Passivation oxide growth at 1000°C
Step 15.	Remove back side oxide
Step 16.	Al evaporation for rear contact and 900°C treatment
Step 17.	Oxide patterning for front metallization
Step 18.	Top contact metal Ti/Ag 600/600 Å lift-off
Step 19.	Rear contact metal Al 1 μ m
Step 20.	Ag plating top to 6 μ m and anneal at 400°C in FG for 30 min

Table 4-6. Light IV Data for IP Solar Cells with DLAR Using Process Sequence In Table 4-5.

Cell ID	Jsc	Voc	FF	EFF(%)
JIPZM1	37.2	658	.808	19.8
JIPSM2	37.01	657	.810	19.7

Figure 4-6. Schematic of inverted pyramid solar cell structure with full Al back contact.

Figure 4-7. Measured reflectance and the IQE of 19.7% inverted pyramid cell fabricated with ZnS/MgF₂ and SiN/MgF₂ DLAR coating.

Figure 4-8. A comparison of the measured and modeled IQE of the 19.7% efficient inverted pyramid cells with full Al back.

4.3.1 Optimization of Phosphorus Diffusion

Diffused test structures were fabricated on high resistivity wafers for three different diffusion conditions, shown in Table 4-7. These test structures have phosphorus diffusion on both sides followed by 1050°C oxidation and 30 min forming gas anneal (FGA at 400°C) to give 1100 Å thick SiO₂ for passivation and antireflective coating. J₀ measurement were performed by PCD lifetime measurements as a function of injection level. Table 4-VII shows that J₀ decreases with decreasing phosphorous diffusion temperature or surface doping concentration. This shows that for high resistivity samples, higher sheet resistivity, which means lower doping concentration, gives lower values of J₀. One might think that higher surface doping concentration should give lower J₀ because it can shield the carriers from surface recombination centers. However, in this case, we have transparent emitters and J₀ is dominated by surface recombination velocity at the doped Si/SiO₂ interface. Surface recombination velocity increases with surface dopant concentration and band-gap narrowing in the heavily doped region raises the J₀ value. This experiment shows that 850 °C diffusion can give about 120-160 Ω / □ and a relatively low J₀ of 4E-14 A/cm².

Table 4-7. J₀ Values Measured by PCD on High Resistivity Samples After 20 Min Phosphorous Diffusion Followed by 70 Min 1050°C Oxidation and 30 Min 400°C FGA.

<u>Sample ID</u>	<u>PH.Diff. Temp.°C</u>	<u>Sheet Resis. $\mu/\square$</u>	<u>J₀ [A / cm²]</u>
JPO1	850	120-160	4E-14
JPO2	880	40- 60	3.5E-13
JPO3	930	17- 20	6.3E-13

4.3.2 Optimization of Al Diffusion

High efficiency solar cells also require low back surface recombination velocity. Ohmic contacts, such as metal back, have very high recombination velocity ($\geq 10^6$ cm/sec) at the semiconductor/metal interface which increases J_0 and lowers V_{oc} . To obtain high efficiency cells, the metal contact areas must be restricted to small fraction of the rear surface, usually below 1%. Spacing between these point contacts is important because it can affect the J_0 of the solar cells which in turn affect the V_{oc} and J_{sc} .

Point contact Al diffused test structures were fabricated on high resistivity material to minimize J_0 . High resistivity samples were first oxidized at 1050 °C to grow 1100 Å SiO_2 and then 150 μm square contact holes with 2 mm separations were opened photolithographically through the oxide on both sides of the wafers. Using the lift-off technique, the Al metal was evaporated only in the contact holes and Al/Si alloy was formed by drive-in at different temperatures. Table 4-8 shows that the measured J_0 values for the samples that went through different Al diffusions followed by 400 °C 30 min FGA. Excess Al was etched after the Al drive in. Table 4-8 shows that 800 °C Al drive gave lower J_{0b} compared to 900 and 1000 °C.

Table 4-8. J_0 Values Measured by PCD on High Resistivity Samples After 1100°C Oxidation for 70 Min Followed by Al Point Contact Diffusion and 30 Min FGA at 400°C.

<u>Sample ID</u>	<u>Al Diff. Temp.°C</u>	<u>J_0 [A / cm²]</u>
JOAF1	800	3E-13
JOAF2	900	7-8E-13
JOAF3	1000	7-8E-13

4.3.3 20.7% Solar Cell on .2-.3 Ω -cm FZ Si

The optimized phosphorous and point-contact Al diffusions were used to minimize surface recombination velocities and J_o . The process sequence used for this run is shown in Table 4-9, which resulted in 20.7% efficient cell with V_{oc} of 678 mV and J_{sc} of 38.98 mA/cm² on .2-.3 Ω -cm FZ silicon. The cell area was 4 cm². Table 4-10 shows light I-V data for the cells tested at Sandia National Labs. Figure 4-9 shows the schematic diagram of the cell structure. Figure 4-10 shows the IQE and surface reflectance of the best cell.

Figure 4-11 shows inverse IQE versus optical absorption length for the best cell. There are two linear regions in this plot. The slopes give L_{IQE} , which represent effective diffusion length enhanced by texturing and W_{IQE} , which represents effective photogeneration thickness and includes path length enhancement due to texturing. Table 4-11 summarizes the result of this analysis. The value of L_{IQE} , which is affected by back-surface recombination, was 467 μ m which is in good agreement with the measured open circuit voltage decay (OCVD) lifetime value of 94 μ s. The light trapping parameters derived from this plot gives an internal back-surface reflectance of 93.6% and internal front-surface reflectance of 93.8% with an effective number of passes of 30.4. These numbers support very good light trapping efficiency of these cells.

V_{oc} and J_{sc} analysis gives total J_o value of 130 fA/cm² and J_{ob} of 9×10^{-14} and J_{os} of 4×10^{-14} A/cm². These values in good agreement with measured values of J_o , J_{ob} and J_{os} even though high resistivity material was used for

characterization of J_0 . Ideally, similar resistivity materials should be used for J_0 characterization, but it is difficult to make such measurements on low resistivity, low lifetime materials.

Table 4-9. Process Sequence Developed for Inverted Pyramid Solar Cells After J₀ Measurement for Al and Phosphorous Diffusions.

STEPS	
1.	.2-.3 ohm-cm, FZ, p-type, 300 um thick
2.	Oxide growth at 1050 °C for 2 hr
3.	Oxide patterning
4.	Inverted pyramids KOH:H ₂ O = 8:100 (w/v) at 70 °C
5.	Rounding the edges with HF:HNO ₃ = 1:40
6.	Oxide growth 1050 °C 3 hr
7.	Oxide patterning for N ⁺ phosphorous diffusion
8.	Phosphorous diffusion 930 °C 20 min 15-20 Ω / □
9.	Deglaze HF:H ₂ O = 1:20 for 2 min
10.	Oxide growth 1050 °C 2 hr
11.	Oxide Patterning for emitter diffusion
12.	Phosphorous diffusion at 850 °C for 20 min 120-160 Ω / □
13.	Deglaze HF:H ₂ O = 1:20 for 2 min
14.	Passivation oxide growth at 1050 °C
15.	Define point contact areas on the back side
16.	Al evaporation and lift-off for rear contact and 800 °C treatment
17.	Oxide patterning for front metallization
18.	Top contact metal Ti/Ag 600/600 °A lift off
19.	Rear contact metal Al 1 um
20.	Ag plating top to 4-6 um and anneal at 400 °C in FG for 30 min

Table 4-10. Light IV Solar Cell Parameter for 4 cm² Inverted Pyramid Cells
Fabricated on .2-.3 Ω -cm and Measured at Sandia National Labs.

CELL ID	V _{oc}	J _{oc}	FF	EFF (%)	τ_{ocvd} [μ s]
JSIVP3-A	.678	38.98	.783	20.70	94
JSIVP3-B	.675	38.50	.789	19.99	86
JSIVP3-C	.675	38.07	.777	19.97	97
JSIVP3-D	.672	37.91	.778	19.82	84

Table 4-11. Light Trapping Parameters Derived from Reflectance and IQE
Measurement at Sandia for Sample JSIVP3-A.

Analysis of the near bandgap IQE and reflectance data has revealed the following :

W_{iqe}	= 12075 μ m	Slope of IQE ⁻¹ vs. α ⁻¹ plot
η_c	= 76.9 %	Collection efficiency
L_{iqe}	= 467 μ m	Effective photogeneration thickness
R_{sub}	= 50.8 %	Sub-bandgap reflectance
R_{fe}	= 6.8 %	External front-surface reflectance

The light trapping parameter derived from these parameters are;

Internal Back-Surface Reflectance	= 93.6 %
Internal Front-Surface Reflectance	= 93.8 %
Effective Number of passes	= 30.4

Figure 4-9. Schematic of inverted pyramid solar cell structure with Al point contact in the back.

Figure 4-10.

IQE and reflectance of cell id JSIVP3-A measured at Sandia.

Figure 4-11. Inverse internal quantum efficiency versus optical absorption length for cell id JSIVP3-A.

Dark IV analysis of the best cell showed the 20.7% efficient cell suffers from high series resistance of about .82-.85 $\Omega\text{-cm}^2$, which we think is caused by high contact resistance of the point contact structure on the back. These cells have low J_{sc} due to high series resistance and low-resistivity, low lifetime material. Use of higher resistivity material (2 $\Omega\text{-cm}$) and incorporation of BBr_3 for BSF can increase the J_{sc} and the cell performance.

PC-1D model calculations in Figure 4-12 for different resistivities as a function of lifetime shows that If 1 ms lifetime can be maintained in 2 $\Omega\text{-cm}$ material, one can get greater than 23% efficient solar cells. This is entirely consistent with the work of Green et al.

Figure 4-12. PC-1D model calculations of efficiency versus lifetime for different resistivity materials.

4.4 RAY TRACING ANALYSIS OF THE INVERTED PYRAMID TEXTURING GEOMETRY FOR HIGH EFFICIENCY SILICON SOLAR CELLS

4.4.1 Introduction

Texturing solar cell surfaces to improve the cell performance has been attempted since 1960 [13]. There are three major objectives to light trapping by texturing the cell: a) *reduce the front surface reflectance*, b) *increase the path length of the light through the cell*, and c) *increase the amount of trapped light, reflected from the back surface, by total internal reflection at the front surface/air interface by making the incident angle greater than the critical angle*. Current ray tracing analyzes concentrate on the path length enhancement and internal characteristics [14,15]. However, examination of the these two effects does not totally characterize the light trapping capabilities of a particular geometry. The light trapping geometry which has been utilized on the highest efficiency cells [16,17], inverted pyramids, has not yet been analyzed in terms of the three criteria listed above.

The purpose of this section is to examine all three aspects of light trapping in the inverted pyramid geometry shown in Figure 4-13. The properties of the inverted pyramids will be compared to the slats, pyramids, and Lambertian geometries to highlight the advantages and disadvantages of the geometry. First, the maximum current as a function of texturing angle and front surface reflectance is calculated. A spectral response argument for the increase in current as a function of texture angle is then formulated. The short

wavelength spectral response, assuming 100% collection efficiency, is indicative of the number of bounces a ray undergoes on the front surface before being reflected away from the cell. Reflection is the dominant loss mechanism. Comparison of the short wavelength spectral response at the natural texturing angles (53.75°) for the geometries shows the superior overall reflectance properties of the inverted pyramids. The internal characteristics and path length enhancement of all the geometries are calculated to support the improvement in current for the inverted pyramids. The maximum current as a function of cell thickness is then illustrated for Lambertian and inverted pyramid geometries with a double layer AR coating on the front surface. Finally, estimates of cell efficiencies are presented to show the potential of the inverted pyramids geometry.

Figure 4-13. The inverted pyramids geometry used for light trapping on the highest efficiency silicon solar cells.

4.4.2 Ray Tracing Program and Material Parameters

TEXTURE [18,19], a Monte Carlo ray tracing program, was used extensively in this paper for the characterization and calculation of the light trapping efficiency for the surface structures. Two of the four output modes (quantitative and qualitative) are used in the analysis presented here.

In the quantitative mode, the program calculates the percentage of photons absorbed at each wavelength simulated. This is equivalent to the idealized spectral response with 100% internal quantum efficiency. From the knowledge of the front surface reflection coefficient and the percentage of photons absorbed at short wavelengths, the number of bounces on the front surface may be estimated. For instance, if the front surface reflectance ($R < 1$) is 30% and 97.3% of the photons are absorbed (A) then the rays of light must undergo a triple bounce before being reflected away from the cell ($A = 1 - R^3$). The quantitative mode also provides the total number of photons absorbed. Multiplying this number by the electronic charge (q) gives an estimate of the maximum short circuit current assuming 100% collection of the photogenerated carriers. The increase in average surface area relative to a planar cell is also calculated in this mode to aid in estimating the change in open circuit voltage and efficiency of the textured cells following the analysis of Roedel and Holm [20]. In addition, the program calculates the number of photons not absorbed in the semiconductor due to losses out the sides of the cell and those lost at the back surface due to imperfect reflection.

In the qualitative mode, the program simulates the percentage of rays remaining as a function of the number of passes through the cell, the quantitative information about photon absorption is absent. As a texturing geometry becomes more efficient in trapping light by total internal reflection, a higher percentage of rays remain for the same number of passes through the cell. The qualitative mode also provides the average path length, relative to the thickness of a planar cell, to indicate the path length enhancement of the texturing scheme. Therefore, by a judicious use of the two output modes of the program, all three important aspects (front surface reflectance, path length enhancement, internal reflection characteristics) of a texturing geometry can be examined.

Since texturing is more common for silicon solar cells as compared to the cells fabricated on III-V and II-VI materials, all the analysis and calculations in this paper are performed assuming Si cells. In the qualitative mode the back surface reflectance is automatically set to unity and the front surface reflectance is set to zero, to determine the internal trapping characteristics. Since no information on photon absorption is provided, the absorption coefficient of the material is not necessary. However, for the quantitative mode, the input values for the index of refraction and absorption coefficients as a function of wavelength were obtained by importing the appropriate files from PC-1D version 3, a device modeling program [21]. In the quantitative mode, the back surface reflectance was set to 98% for all wavelengths, unless

specified differently. For the simulation of the absorbed flux, three different front surface reflection coefficients were used. In the first case, the reflectance was static at 30% to simulate bare Si. For the other two cases, files of front surface reflection as a function of wavelength were created to match a single layer anti-reflection (AR) coating of 70 nm of Si_3N_4 and a double layer AR coating consisting of 85 nm MgF and 50 nm of ZnS with a 5 nm SiO_2 passivation layer underneath (Figure 4-14). The light intensity simulated was 0.1 watts/cm^2 with a spectral distribution corresponding to air mass 1.5. The AM1.5 direct spectrum file was imported from PC-1D version 3. The substrate thickness was assumed to be $100 \mu\text{m}$ (unless specified otherwise), all of the texture heights were summed with the substrate thickness to produce the total cell thickness. The cell area was assumed to be 1 cm^2 . The texture period was assumed to be $20 \mu\text{m}$ with face angles of 53.75° , except when the texturing angle was varied. For the estimation of efficiency, the cells considered had a conventional N^+PP^+ design using a $100 \Omega\text{-cm}$ substrate with an emitter depth of $0.2 \mu\text{m}$ and a surface concentration of $2.0 \times 10^{19} \text{ cm}^{-3}$. The back surface diffusion was $2.0 \mu\text{m}$ with a surface concentration of $2.0 \times 10^{18} \text{ cm}^{-3}$. Both diffusions were assumed to have the shape of the complementary error function. The minority carrier lifetime in the base was fixed at 2 msec, to provide collection of nearly all the photogenerated carriers and to model good quality material. The series resistance of the cell was set at 0.2Ω and the surface recombination velocities were fixed at 5 cm/sec for planar surfaces and

50 cm/sec for Lambertian surfaces. This order of magnitude increase in surface recombination velocity may be extreme, but without the proper information these values seem reasonable. Planar and Lambertian cells of this design were simulated using PC-1D version 3. The solar cell parameters calculated from PC-1D for the planar cells were then used in the methodology of Roedel and Holm to estimate the efficiency of the textured cells. A two dimensional analysis is avoided by assuming that all the photogenerated carrier are collected.

Figure 4-14.

Front surface reflectance as a function of wavelength for a single and double layer anti-reflection coatings, a static value of 30% is taken to represent bare silicon.

4.4.3 Results

Figure 4-15 shows the calculated maximum current as a function of texturing angle for the three geometric texturing geometries (slats, pyramids, and inverted pyramids) with bare silicon front surface ($R = 30\%$) condition and no back surface reflector (0% reflection). At 45° and 60° all three geometries produce approximately the same maximum current. Examination of the short wavelength spectral response, Figure 4-16, indicates that at 45° the percentage of photons absorbed is indicative of a double bounce ($S.R. = 1 - R^2$) for all of the texturing geometries. At texturing angles of 60° the spectral response indicates that all of the rays undergo a triple bounce ($S.R. = 1 - R^3$) on the front surface before being reflected away. The small variations in current at texturing angles of 45° and 60° for the three different geometries are due to slight differences in the optical path length. For texturing angles between 45° and 60° the spectral response of the inverted pyramid geometry increases more than the spectral responses of the slats or upright pyramid (Figure 4-16). A higher percentage of rays ($\sim 37\%$ at an angle of 54°) undergo a triple bounce due to interaction with the adjoining planes of the inverted pyramid. Figure 4-17 shows the reflection of light in a slat of 53.75° . No rays striking the surface are capable of experiencing a triple bounce. In the case of the inverted pyramids however, rays which strike one face, reflect light onto an orthogonal plane, which then reflects the light onto the face complementary to the original point of impact, Figure 4-18. Due to the higher percentage of rays undergoing

a triple bounce, the spectral response of the inverted pyramids is higher than that of the slats or upright pyramids at texturing angles between 46° and 59° . The increase in spectral response has been shown to be valid for angles of incidence up to 10° off normal [19], although the spectral response is a complicated function of the angle of incidence. Figure 4-19 shows the maximum current for the three geometric texturing geometries as a function of texturing angle and three front surface reflectance conditions. A 98% effective back surface reflector has been incorporated into the design. Notice the difference in the maximum current assuming bare silicon reflection condition for the three geometries as compared to Figure 4-15. This difference is due to the path length and internal light trapping characteristics which become important because of the application of the back surface reflector. Also from Figure 4-19, notice that as the front surface reflectance is decreased due to the application of AR coatings, the importance of the triple bounce is diminished for the natural texturing angle of 53.75° . The difference in maximum current between the three geometries with AR coatings has become less.

The internal light trapping characteristics and path length enhancement, of the three geometries which have been included implicitly in Figure 4-19, can now be compared to the characteristics of the Lambertian design. It has been well documented that the path length of the Lambertian design is approximately twice the substrate thickness (TEXTURE predicts 1.93). Also, the internal light trapping efficiency has been shown to be proportional to $1/\eta^2$ [14]. This

proportionality dependence is depicted in Figure 4-20, assuming the index of refraction was fixed at 3.6. However, the simulations of the three geometries use index of refraction values which are a function of wavelength. Therefore, the comparison of these isometric geometries to the Lambertian case should be for a variable index of refraction, which is also shown in Figure 4-20. The final three curves in Figure 4-20 show the percentage of rays trapped for the three isometric geometries. Recall that there is no front surface reflectance and the back surface reflectance has been set to one. After two passes the inverted pyramids retains a higher percentage than either the pyramids or slats geometries. However, the percentage trapped by the inverted pyramids is much less than the Lambertian design. As previously stated, the path length of the Lambertian design is approximately 2, while the inverted pyramid is 1.4073, this is superior to the slats and pyramids which have path length enhancements of 1.127 and 1.303, respectively.

The maximum current as a function of cell thickness is shown in Figure 4-21 and given in Table 4-12 for the Lambertian and inverted pyramid designs assuming a double layer AR coating. As the thickness of the cell increases the difference in the predicted current between the two geometries decreases. Table 4-13 also contains the number of photons (in terms of current) lost due to the imperfect rear reflector (recall that it is only 98% effective) and finite cell dimensions. The magnitude of these losses is fairly small, but no longer insignificant.

Figure 4-15.

Maximum current as a function of texturing angle for the slats, pyramids, and inverted pyramids designs on $100\ \mu\text{m}$ cells. The front surface reflectance is set at 30% and no back surface reflector.

Figure 4-16.

Spectral response for the three cells depicted in Figure 4-15 at several texturing angles. The magnitude of the short wavelength response is indicative of the number of bounces on the front surface.

Figure 4-17.

Reflection of ray in slats with an angle to the horizontal of 53.75° . No rays are able to hit the surface three times. The same is true for the pyramids design.

Three Sides of Inverted Pyramids

Figure 4-18. Reflection of rays in the inverted pyramids design. Due to the impact of hitting an orthogonal plane, a percentage of rays undergo a triple bounce on the front surface.

Figure 4-19.

Maximum current as a function of texturing angle for the slats, pyramids, and inverted pyramids designs on $100\ \mu\text{m}$ cells. Three front surface reflectance conditions are shown. The back surface reflector was assumed to be 98% effective.

Figure 4-20.

Percentage of rays remaining as a function of the number of passes through the cell structure for: a) Lambertian design with $\eta = 3.6$, b) Lambertian design with variable η , c) slats, d) pyramids, and e) inverted pyramids.

Figure 4-21.

Maximum current as a function of cell thickness for the Lambertian and inverted pyramids designs for three front surface reflectance conditions. The back surface reflector is 98% effective.

Table 4-12. Calculated Current Values for Inverted Pyramids and Lambertian Geometries with a Double Layer AR Coating and 98% Back Surface Reflector, All Values in mA/cm².

Cell Thickness s (μm)	Inverted Pyramids			Lambertian		
	J _{sc}	Back Loss	Side Loss	J _{sc}	Back Loss	Side Loss
50	38.8059	.64706	.03225	40.0823	1.2647	.08216
75	39.5079	.56089	.04454	40.6128	1.1382	.11107
100	40.2837	.6586	.06324	40.9639	1.0577	.13709
125	40.8077	.60283	.08624	41.2250	.99645	.16308
150	41.0805	.5906	.06285	41.4072	.9554	.1990
175	41.297	.66344	.1237	41.5572	.9161	.2328
200	41.6577	.6773	.14501	41.7116	.8758	.2612
225	41.4862	.5597	.08460	41.8289	.8458	.2771
250	41.7255	.5372	.11483	41.9283	.82098	.28182
275	41.9170	.5388	.09983	42.0170	.80066	.30516
300	42.0933	.4700	.11711	42.0969	.7863	.3128
325	42.1862	.48868	.1205	42.1660	.7699	.33156
350	42.226	.4825	.2480	42.2280	.7474	.34716
375	42.2285	.4959	.18798	42.2897	.7336	.3422
400	42.3242	.5494	.1374	42.3426	.7225	.3475

Table 4-13. The Values of Maximum Short Circuit Current for Various Surface Texturing Designs at Air Mass 1.5 Direct with Three Different Front Surface Reflection Coefficients. The Cell Number Corresponds to That Geometry in All of the Figures.

<u>Cell Number</u>	<u>Front</u>	<u>Back</u>	<u>30% Reflectance</u>	<u>Single Layer AR Coating</u>	<u>Double Layer AR Coating</u>
1	3PP	Flat	40.99	42.16	42.29
2	3PP	Lambertian	40.82	42.01	42.19
3	Inverted Pyramids	Lambertian	39.27	41.75	42.14
4	Pyramids	Lambertian	38.27	41.59	42.11
5	Slats in X	Lambertian	38.25	41.57	42.11
6	Slats in X	Slats in Y	38.06	41.46	42.09
7	Lambertian	Lambertian	29.51	38.49	41.05
8	Lambertian	Flat	29.44	38.41	40.96
9	Flat	Lambertian	29.44	38.41	40.96
10	Inverted Pyramids	Flat	37.76	40.03	40.23
11	Pyramids	Flat	36.41	39.47	39.79
12	Slats in X	Flat	35.92	38.90	39.15
13	Flat	Flat	26.71	35.16	37.34

4.4.4 Estimation of Cell Efficiency

The methodology of Roedel and Holm [20] was used to estimate the texture-induced improvement in cell efficiency and the degradation in open circuit voltage compared to the corresponding planar cell. In this methodology, the open circuit voltage of the textured cell (V_{oc}^T) is expressed as

$$V_{oc}^T = V_{oc}^f + \frac{KT}{q} \ln \left(\frac{1 + \frac{J_{sc}^T - J_{sc}^f}{J_{sc}^f}}{\frac{Area^T}{Area^f}} \right) \quad (1)$$

Where V_{oc}^f , $Area^f$, J_{sc}^f are the open circuit voltage, surface area, and short circuit current of the planar cell, $Area^T$ and J_{sc}^T are the area and calculated short circuit current of the corresponding textured cell. The change in efficiency due to the textured surface (η^T) is then estimated from

$$\eta^T = \eta^f + \eta^f \times \left(\frac{\Delta J_{sc}}{J_{sc}^f} + \frac{\Delta V_{oc}}{V_{oc}^f} \right) \quad (2)$$

where η^f denotes the value of the efficiency for the planar cell, $\Delta V_{oc} = (V_{oc}^T - V_{oc}^f)$, and $\Delta J_{sc} = (J_{sc}^T - J_{sc}^f)$. The surface area ($Area^T$) and short circuit current (J_{sc}^T) for the textured cells were obtained from the output of the TEXTURE program.

Using values of efficiency, open circuit voltage, and short circuit current for planar cells, calculated from PC-1D version 3, with equations (1) and (2) provide estimates of textured cell efficiencies assuming that the dominate

recombination mechanism is area dependent. The results of the PC-1D calculations and estimates for inverted pyramids and Lambertian textured cells of various thicknesses are summarized in Table 12 and Figure 4-22. Experimental values of current (42.9 mA/cm^2) from cells with the inverted pyramids geometry have been reported in reference [17], correcting these values by 4 to 5% due to calibration error [22] puts the actual current in the range from 40.75 to 41.18 mA/cm^2 . Model calculations for a substrate of comparable thickness predicted a current of 41.7 to 42.0 mA/cm^2 , which is in good agreement with the experimental numbers considering grid coverage and global spectrum were not included in the simulation.

Figure 4-22. Efficiency estimates for as a function of cell thickness for the planar, inverted pyramids, and Lambertian texturing geometries. The double layer AR coating reflectance was assumed for the front surface reflectance condition.

4.4.5 Conclusions

The light trapping properties of the inverted pyramid geometry have been analyzed for the first time. The increase in current for this type of textured cell is due to the incorporation of all three effects necessary for an efficient light trapping design. The front surface reflectance is reduced by providing the opportunity for a portion of the incoming light to undergo a triple bounce, thereby reducing the overall front surface reflectance. The increase in path length and light trapping efficiency means that a larger fraction of the light which has entered the cell will be absorbed before exiting the cell. It is shown quantitatively for the first time that the inverted pyramids geometry is superior to either the slats or regular pyramids. The inverted pyramids on a 100 micron cell with a two layer AR coating is estimated to give 40.2 mA/cm^2 and cell efficiencies of ~24% with realistic cell design and material parameters.

4.5 A New Texturing Geometry for Producing High Efficiency Solar Cells with No Antireflection Coatings

4.5.1 Introduction

Texturing solar cell surfaces to improve the cell performance has been attempted since 1960 [1]. There are three objectives in light trapping by texturing the cell: a) reduce the front surface reflectance, b) increase the path length of the light through the cell, and c) trap the light reflected from the back surface by total internal reflection at the front surface\air interface by making

the incident angle greater than the critical angle. In the very first textured cell (1960), the primary goal was to reduce the front surface reflectance without applying anti-reflection coatings [1]. Later (1974-1987), texturing was used to produce double bounces on the front surface and trap weakly absorbed long wavelength photons by total internal reflection [2,3,4]. Until the mid 1980s the random or Lambertian design, which relied solely on trapping weakly absorbed light, theoretically outperformed all other texturing designs. Then in 1987, Landis proposed the perpendicular slats geometry, analyzed by Campbell and Green, which could outperform the Lambertian design (Figure 4-23). This enhancement was accomplished by a combination of reducing the front surface reflection by a double bounce on the front surface and trapping weakly absorbed light by total internal reflection due to the randomization of the light within the cell. Experimental verification of the enhancement in absorption of the perpendicular slats was provided by Keavney [5]. To date, cells fabricated using the perpendicular slats geometry have not outperformed other texturing designs, probably due to experimental difficulties and process-induced device degradation. Also, due to the cost of a double texture process (front and back surface), a fabrication sequence with only a single texture definition is still preferred.

The purpose of this section is twofold. First, to introduce a new texturing geometry which could outperform the perpendicular slats geometry in trapping light. Second, to provide guidelines and quantitative comparison for various

promising texturing schemes with single and double sided textures. The proposed texturing scheme consists of three perpendicular planes (3PP) on the front surface (created by intersecting [100], [010], and [001] planes) and a planar back surface (Figure 4-24). It is shown that even with a Lambertian back surface the 3PP geometries' performance characteristics are very similar to the perpendicular slats geometry. The three perpendicular planes provide multiple bounces on the front surface, thereby reducing the front surface reflectance. Due to the strong coupling between the planes of the texturing geometry, light returning from the back surface is totally internally reflected at the semiconductor/air interface.

The remainder of this paper will introduce the applicability of a raytracing program [6] in quantifying optical confinement and discuss its application in analyzing the light trapping efficiency of promising texturing schemes, including the breakdown of the improvement from reduced reflection and total internal reflection. Finally, some guidelines for developing a fabrication procedure for the proposed new texturing design will be given along with potential cell efficiency improvement from the new design.

Figure 4-23. Schematic drawing of perpendicular slats geometry for textured solar cells.

Figure 4-24. Schematic drawing of the three perpendicular planes geometry for textured surfaces.

4.5.2 Raytracing Program

TEXTURE, a Monte Carlo raytracing program to model textured solar cells, was introduced and described in more detail at the 21st PVSC [6], and is used extensively in this paper for the characterization and calculation of the light trapping efficiency for various surface geometries. Two of the four output modes (quantitative and qualitative) are used in the analysis presented here. In the quantitative mode, the program gives the percentage of photons absorbed at each wavelength simulated. From the knowledge of the front surface reflection coefficient and the percentage of photons absorbed at short wavelengths, the number of bounces on the front surface may be estimated. For instance, if the front surface reflectance (R) is 30% and 97.3% of the photons are absorbed (A) then the rays of light must undergo a triple bounce before being reflected away from the cell ($A = 1 - R^3$). The quantitative mode also provides the total number of photons absorbed, and multiplying this number by the electronic charge (q) gives an estimate of the maximum short circuit current, assuming 100% collection of the photogenerated carriers. The maximum short circuit current ($J_{sc\ max}$) is a good indicator of the light trapping efficiency of the texturing scheme. The increase in average surface area relative to a planar cell is also obtained in this mode to aid in estimating the change in open circuit voltage and efficiency of the cell [7]. In addition, the program determines the number of photons not absorbed in the semiconductor due to losses out the sides of the cell and the back due to imperfect back surface

reflectors. For most texturing designs the loss from the sides of the cell is small ($< 0.075 \text{ mA/cm}^2$); however, as the light trapping improves, an appreciable amount ($\sim 0.16 \text{ mA/cm}^2$) may be lost out the sides of the cell.

In the qualitative mode, the program output is the percentage of rays remaining as a function of the number of passes through the cell, and the quantitative information about photon absorption is absent. As a texturing geometry becomes more efficient in trapping light by total internal reflection, a higher percentage of rays remain for the same number of passes through the cell. The qualitative mode also gives the average path length, relative to the thickness of the planar cell, to indicate how the texturing scheme enhances the path length. Therefore, by a judicious use of the two modes of this program all three important aspects (front surface reflectance, path length enhancement, internal reflection characteristics) of a texturing geometry can be examined.

4.5.3. Material Parameters

Since texturing is more common for silicon solar cells as compared to the cells fabricated on III-V and II-VI materials, all the analysis and calculations in this paper were performed assuming Si cells. The input values for the index of refraction and absorption coefficients as a function of wavelength were obtained by importing the appropriate files from PC-1D version 3, a device modeling program [8]. In the qualitative mode the back surface reflectance is automatically set to unity, and the front surface reflectance is set to zero. In

the quantitative mode the back surface reflectance was set to 98% for all wavelengths. For the simulation of the absorbed flux, three different front surface reflection coefficients were used. In the first case, the reflectance was static at 30% to simulate bare Si. For the other two cases, files of front surface reflection as a function of wavelength were created to match a single layer anti-reflection (AR) coating of 70 nm of Si_3N_4 and a double layer AR coating consisting of 110 nm MgF_2 and 50 nm ZnS with a 5 nm SiO_2 passivation layer underneath (Figure 4-25). The light intensity simulated was 0.1 watts/cm^2 with a spectral distribution corresponding to air mass 1.5. The AM1.5 direct spectrum file was imported from PC-1D version 3. The substrate thickness was assumed to be $100 \mu\text{m}$, all the texture heights were summed with the substrate thickness to produce a total cell thickness of $105 \mu\text{m}$. The cell area was assumed to be 1 cm^2 . For the slats and inverted pyramids geometry the natural angles of 53.75° were simulated. For the estimation of efficiency the cell structure considered had a conventional N^+PP^+ design using a $100 \Omega\text{-cm}$ substrate with an emitter depth of $0.2 \mu\text{m}$ and a surface concentration of $2.0 \times 10^{19} \text{ cm}^{-3}$. The back surface diffusion was $2.0 \mu\text{m}$ deep with a surface concentration of $2.0 \times 10^{18} \text{ cm}^{-3}$. Both doping profiles were assumed to have a complementary error in shape. Minority carrier lifetime in the base was fixed at 2 msec, to provide a collection of nearly all photogenerated carriers and to model good quality material. By assuming that all of the photogenerated carriers are collected, a two dimensional analysis technique is

avoided. The series resistance of the cell was set at $0.2 \, \Omega$ for the flat and Lambertian front surfaces. The surface recombination velocity was set at 5 cm/sec for flat cells and 50 cm/sec for the Lambertian texture. For other textured surfaces, the surface recombination velocity of the flat surface (5 cm/sec) was used. The increase in the area was incorporated into the open circuit voltage expression. This order of magnitude increase in recombination velocity for a Lambertian surface may be extreme, but without the proper information these values seem reasonable.

Figure 4-25. Plot of three different front surface reflectance conditions used in cell modeling: base silicon surface, single layer, and double layer anti-reflection.

4.5.4 Results

Figure 4-26 shows the percentage of rays remaining as a function of the number of passes for several single sided textured geometries. The three perpendicular planes (3PP) geometry maintains the largest percentage of trapped rays for up to 15 passes through the structure. It should be noted that the Lambertian design on either the front or back provided very good internal trapping characteristics for a single sided geometries. On the other hand, the inverted pyramids, pyramids, and slats geometries provide poor internal reflection properties when used alone (Figure 4-26). However, when these geometries are used in conjunction with a Lambertian texture on the back surface, the internal light trapping characteristics improve and become very similar to the perpendicular slats and Lambertian designs (Figures 4-27 and 4-28). This is contrary to the case of the 3PP geometry with a Lambertian back surface, in which the light trapping efficiency decreases; compare Figures 4-27 and 4-28. This decrease in the trapping efficiency may be due the strong coupling between the planes on the front surface; i.e. the history of the ray is destroyed using the Lambertian back surface. Note that if the percentage of rays remaining increases as the number of passes increase, the red response of the cell should improve. It is important to realize that the use of Figures 4-26, 4-27 and 4-28 alone in evaluating a texturing design could be misleading because these figures only reveal the internal characteristics or just one aspect of the texturing geometry.

Figure 4-26. Plot of percentage of incident rays remaining trapped within the cell as a function of the number of passes. Single sided texture with planar rear surface.

Figure 4-27.

Plot of percentage of incident rays remaining as a function of the number of passes through the cell for several double sided texturing geometries.

Figure 4-28.

Plot of percentage of incident rays remaining as a function of the number of passes through the cell for the most efficient double sided texturing geometries.

The external characteristics or the front surface reflectance of a flat or Lambertian, inverted pyramids, and 3PP textures, assuming a bare silicon front surface and a planar back surface with a 98% effective reflector, are shown in Figure 4-29. The figure clearly shows that for the inverted pyramids, small percentage the rays of light undergo a triple bounce ($\sim 37\%$) while the rest of the rays experience a double bounce ($A = 1 - 0.63 \cdot R^2 - 0.37 \cdot R^3$). For the 3PP geometry all the rays (100%) experience a triple bounce ($A = 1 - R^3$) on the front surface. An example of a ray experiencing the triple bounce is shown in Figure 4-30. This triple bounce results in a substantial reduction in the front surface reflectance. Preliminary results indicate that for angles of incidence more than 5° off normal, not all of the rays experience the triple bounce leading to a reduction in the spectral response. The maximum possible short circuit current is shown in Table 4-14 and Figure 4-31, assuming 100% collection of all photogenerated carriers. Notice that cells which have the 3PP geometry on the front and planar or Lambertian back surface are capable of producing very high currents using just bare silicon with no AR coatings. However, as the front surface reflection is reduced with the application of anti-reflection coatings, the relative increase in current is not as dramatic since a double bounce with an AR coating is almost as effective as the triple bounce with no AR coating in reducing the front surface reflectance. Figure 4-32 shows the loss of photons at the back surface of the cell due to the imperfect rear reflector. In all cases, except for the perpendicular slats, this loss is less than 1.1 mA/cm^2 . In the case

of the perpendicular slats the loss is higher due to the double bounce in the slat at the back of the cell since each bounce produces a 2% loss in photons.

Figure 4-29.

Plot of the percentage of photons absorbed as a function of wavelength for three different surface texturing designs. The front surface reflectance was 0.30 and independent of wavelength.

Figure 4-30.

An example of a ray experiencing a triple bounce in the three perpendicular plane geometry. The ray strikes all three of the planes before being reflected away from the cell.

Figure 4-31. Spectral response of the 3PP /flat and 3PP/Lambertian cells. The front surface reflectance was static at 30%.

Figure 4-32.

Modeled $J_{sc\ max}$ for several texturing designs, three different front surface reflection conditions were simulated. See Table 1 for cell configuration key.

Table 4-14. Calculated Values of Short Circuit Current, Open Circuit Voltage, and Efficiency for Various Surface Texturing Designs at Air Mass 1.5 Direct, the Flat and Lambertian Cell Results Are Directly from PC-1D. All Others Are Estimates from the Methodology of Reference [7].

Cell Number	Front Structure	Back Structure	Bare Si			Single Layer AR			Double Layer AR		
			J_{sc}	V_{oc}	η	J_{sc}	V_{oc}	η	J_{sc}	V_{oc}	η
1	3PP	Flat	40.99	0.721	24.38	42.16	0.722	25.18	42.29	0.722	25.26
2	3PP	Lambertian	40.82	0.718	24.21	42.01	0.718	24.94	42.19	0.718	25.05
3	Inverted Pyramids	Lambertian	39.27	0.718	23.28	41.76	0.718	24.80	42.14	0.719	25.04
4	Slats	Lambertian	38.26	0.717	22.65	41.57	0.718	24.69	42.11	0.719	25.03
5	Pyramids	Lambertian	38.27	0.717	22.67	41.59	0.718	24.70	42.11	0.719	25.02
7	Lambertian	Lambertian	29.55	0.723	17.88	38.53	0.729	23.21	41.11	0.731	24.84
8	Lambertian	Flat	29.45	0.726	17.63	38.41	0.733	23.26	40.98	0.735	24.88
9	Flat	Lambertian	29.55	0.724	17.63	38.53	0.730	23.22	41.11	0.732	24.86
10	Inverted Pyramids	Flat	37.76	0.720	22.42	40.03	0.721	23.88	40.23	0.721	24.00
11	Pyramids	Flat	36.41	0.719	21.59	39.47	0.721	23.53	39.79	0.721	23.73
12	Slats	Flat	35.92	0.719	21.29	38.90	0.720	23.18	39.15	0.721	23.33
13	Flat	Flat	26.99	0.725	16.10	35.27	0.732	21.30	37.34	0.733	22.61

The amount of photon loss out the sides of the textured cells is depicted in Figure 4-33. Recall that for the planar cell geometry, the loss out the sides is zero. However, as the light enters the cell or is reflected from the back surface at various angles due to the surface texture, light will be incident upon the sides of the cell. A portion of this light remains in the cell due to total internal reflection; the rest is lost out the sides. In most of the light trapping geometries shown in Figure 4-33, the quantity lost out the sides of the cell is small but no longer negligible. The reason that the loss out the sides for the perpendicular slats is low is the slats tend to confine the rays in a small area, while the Lambertian texture spread the rays throughout the cell.

A comparison of the spectral response of the 3PP geometry with a planar back surface and a Lambertian back surface is provided in Figure 4-34. In the short wavelength range the response of the two cells are identical, as expected, due to both designs having the same reflectance characteristics. In the wavelength range $0.95\ \mu\text{m}$ to $1.1\ \mu\text{m}$ the 3PP/flat geometry possesses a higher response. This is in agreement with Figures 4-26 and 4-28 which showed that this geometry maintained the higher percentage of rays for up to 10 passes. At wavelengths above $1.1\ \mu\text{m}$ the light requires many more passes through the cell structure before being absorbed. Therefore, the response of the 3PP/Lambertian should be higher than the 3PP/flat. This is verified in Figure 4-34.

It is important to note from Table 4-14, and Figures 4-27 through 4-31, that an erroneous conclusion about a surface texture may be drawn by relying

on only one aspect of the light trapping properties of a surface texture. For example, the 3PP with a Lambertian back clearly outperforms (higher $J_{sc\ max}$) the perpendicular slats for all three front surface reflectance conditions simulated (Figure 4-31) even though the internal responses (% rays remaining after a given number of passes) of the two are comparable (Figure 4-28). As shown earlier, this is due to reduced front surface reflectance of the 3PP resulting from the triple bounce.

Figure 4-33. Photon loss (in terms of current) due to imperfect back surface reflector for various surface texturing designs. Three front surface reflection conditions were simulated. See Table 1 for cell configuration key.

	Front	Back
1	3 P. Planes	Flat
2	3 P. Planes	Lambertian
3	I. Pyramids	Lambertian
4	X Slats	Lambertian
5	Pyramids	Lambertian
6	X Slats	Y Slats
7	Lambertian	Lambertian
8	Lambertian	Flat
9	Flat	Lambertian
10	I. Pyramids	Flat
11	Pyramids	Flat
12	X Slats	Flat
13	Flat	Flat

Double Layer Ar Coating
 Single Layer Ar Coating
 Bare Silicon

Figure 4-34. The amount of photon loss (in terms of current) out the sides of the substrate for various surface texturing designs. Three front surface reflection conditions are simulated. See Table 1 for configuration key.

4.5.5 Cell Efficiency

The methodology of Roedel and Holm [7] was used to estimate the texture-induced improvement in cell efficiency and the degradation in open circuit voltage compared to the corresponding planar cell. In this methodology, the open circuit voltage of the textured cell (V_{oc}^T) is expressed as

$$V_{oc}^T = V_{oc}^f + \frac{KT}{q} \ln \left(\frac{1 + \frac{J_{sc}^T - J_{sc}^f}{J_{sc}^f}}{\frac{Area^T}{Area^f}} \right) \quad (3)$$

Where V_{oc}^f , $Area^f$, J_{sc}^f are the open circuit voltage, surface area, and short circuit current, of the flat cell, and $Area^T$ and J_{sc}^T are the area and maximum short circuit current corresponding to the textured cell. The change in efficiency due to the textured surface (η^T) is then estimated from

$$\eta^T = \eta^f + \eta^f \times \left(\frac{\Delta J_{sc}}{J_{sc}^f} + \frac{\Delta V_{oc}}{V_{oc}^f} \right) \quad (4)$$

where η^f denotes the value of efficiency for the planar cell, $\Delta V_{oc} = (V_{oc}^T - V_{oc}^f)$ and $\Delta J_{sc} = (J_{sc}^T - J_{sc}^f)$. The surface area ($Area^T$) and short circuit current (J_{sc}^T) for the textured cells were obtained from the output of the TEXTURE program.

The values of efficiency, open circuit voltage, and short circuit current for planar cells with the three front surface reflection coefficients were calculated using PC-1D version 3. The results of the PC-1D calculations and estimates for textured cells are summarized in Table 4-15 and Figure 4-35. The efficiency calculations for the two geometries with three perpendicular planes show that fairly high efficiency is obtained even with bare silicon surface. More specifically, the three perpendicular planes offer the possibility of producing high efficiency cells (in excess of 24%) without the application of anti-reflection coatings and, therefore, may have the potential of reducing the cost of cell production.

If all the photons with non-zero absorption coefficient ($\alpha > 0$, includes sub-bandgap photons to $\lambda \approx 1250$ nm) in the solar spectrum used in the modeling were absorbed, then the J_L or $J_{sc \text{ max}}$ would have been 47.908 mA/cm². Model calculations not only show that inverted pyramids/Lambertian design without AR coatings can give $J_{sc \text{ max}}$ of 39.275 mA/cm², but they also account for the 8.633 mA/cm² loss in current by revealing a 0.975 mA/cm² loss due to photons escaping through the imperfect back surface, 0.130 mA/cm² loss due to photons being coupled out the sides of the cell, and 7.528 mA/cm² loss from the front surface. The front surface loss consists of front surface reflection as well as photons which are reflected from the back surface but are unable to undergo total internal reflection at the front surface. If only photons with $E \geq E_g$ are considered, then the maximum current attainable would have

been 43.105 mA/cm². Of this 38.931 mA/cm² would be absorbed and the losses would have been 0.268 mA/cm², 0.024 mA/cm², and 3.882 mA/cm² respectively. A consistency check of the program is the photon losses (side, back, reflectance, and zero absorption coefficient) added to the amount of photons absorbed must equal the amount of photons incident. This indicates the applicability and strength of the raytracing model.

Comparison of the efficiency for various texturing schemes in Figure 4-35 indicate that cells with double layer AR coating and inverted pyramids on the front surface along with the Lambertian back surface would produce some of the highest efficiency cells. A more thorough quantitative analysis of the inverted pyramids geometry without the Lambertian back surface is presented in reference [9]. In terms of light trapping ($J_{sc \text{ max}}$), the inverted pyramids without the Lambertian back surface are less effective than the perpendicular slats (see Table 4-14). However, with the incorporation of the Lambertian back surface, the inverted pyramids clearly outperform the perpendicular slats geometry. The perpendicular slats geometry is not included in Figure 4-35 because of the difficulty in modeling the effect of the back surface slat texture. However, the light trapping efficiency ($J_{sc \text{ max}}$) of perpendicular slats falls between the inverted pyramids with and without the Lambertian back (Table 4-14), therefore it is reasonable to expect that important cell parameters (V_{oc} , η) may follow a similar pattern. Figure 4-35 also shows that the 3PP geometry with a planar back surface has the potential to produce a higher efficiency cell

than the inverted pyramids for all cases of front surface reflectance. Some of the highest efficiency cells produced to date utilize the inverted pyramid design on the front [10]. As the texturing technology matures, a logical progression of surface texturing would be from the inverted pyramids with a flat back surface to perpendicular slats. Then as Lambertian back surfaces become available the geometry should switch from perpendicular slats to inverted pyramids with the Lambertian back surface. Finally, provided the 3PP geometry can be produced, the geometry should become 3PP with a planar back surface. A very small sacrifice in efficiency with the 3PP with no AR coatings should become attractive due to the cost reduction.

Figure 4-35.

Estimates of the solar cell efficiency for various surface texturing designs using three different front surface reflection conditions. See Table 1 for cell configuration key.

4.5.6 Proposed Guidelines for Fabrication Procedure

Inverted tetrahedrons, a geometry close to the 3PP, have been produced on the surface of Si by an ultrasonic cutting technique [1]. Neither this technique nor its companion laser cutting are economically feasible at this time, though in the future the cost might become competitive. To economically produce the 3PP geometry modeled in this paper, an anisotropic etch applied to the proper crystalline orientation of Si may be required. The formation of inverted tetrahedrons has been demonstrated when anisotropic etches are applied to multicrystalline Si with grains orientated in the $\{111\}$ direction [11]. A photolithographic step would be required to obtain a regular repeating pattern on the surface before the wafer is immersed in the anisotropic etch. A proposed pattern to be applied to $\{111\}$ Si is shown in Figure 4-36. The peaks of the three perpendicular planes would be directly under the thickest area of the pattern and some under cutting of the oxide would be required.

Fig. 4-36. Proposed mask to produce the three perpendicular planes geometry on (111) silicon. Some undercutting of the oxide would be required.

4.5.7 Conclusions

A new texturing geometry (three perpendicular planes) has been proposed which provides superior light trapping characteristics compared to the perpendicular slats geometry. The superior properties are the result of a reduction in the front surface reflection coefficient and good internal reflection properties of the three perpendicular planes design. In addition, it has been demonstrated that the cost of cell production may be reduced due to the elimination of the anti-reflection coatings. The process technology for the three perpendicular planes geometries needs to be developed. A processing sequence may follow along the methodology used to create inverted pyramids. It is shown that the inverted pyramids geometry with Lambertian back surfaces possess light trapping properties that are superior to the perpendicular slats geometry, which was considered to be the best design until now.

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5.0 DEVELOPMENT OF LOW TEMPERATURE PECVD SiO_2 AND SiN FOR SURFACE PASSIVATION

A technique using low temperature PECVD oxide and SiN for high effective lifetime, low surface recombination velocity and low interface state density at SiO_2/Si interface was developed. In section 5.1, a detailed PECVD processing which results in low surface recombination velocity and high effective lifetime is presented. The effect of photo-assisted anneal of PECVD oxide, and a comparison with furnace anneal are discussed. The oxide charge effect on surface recombination velocity, and the improvement of stability by PECVD SiN deposition, are also analyzed in this section. In section 5.2, a technique which results in record low interface state density for low temperature PECVD oxide is presented. The effect of different PECVD technique and post-anneal process on the interface state density is discussed.

5.1 PECVD Oxide For Low Surface Recombination Velocity And High Effective Lifetime

Low surface recombination velocity and high effective recombination lifetime are both critical for high performance silicon devices. Very thin SiO_2 (~ 100 Å) layers are routinely used in high efficiency silicon solar cells [1], MOSFET, and advanced bipolar devices [2] to reduce surface recombination or to provide high quality insulating layers. Generally, the thin oxide is formed by high temperature (850 - 1050°C) oxidation. The use of low temperature

deposition oxides (SiO_2) is desirable in order to maintain device dimensions within tight tolerance and reduce the process-induced degradation of bulk lifetime. Unfortunately, low temperature processing generally produces low quality oxides with high recombination velocity at the SiO_2/Si interface.³

Recently Bright et al. [3,4] reported on the low-temperature oxide with properties comparable to those of thermal oxides grown at high temperature. In their technique, an initial thin plasma oxide, using low power He plasma containing very low partial pressure of oxygen or water vapor, was found to be critical for obtaining high quality oxide. This initial treatment was followed by the normal PECVD oxide deposition. More recently, Yasuda et al. [5] showed that the SiO_2/Si interface with midgap trap density of $1.7 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ could be achieved by a two step remote plasma-assisted oxidation process, in which the silicon surface is first exposed to oxygen atoms from a remote He/O_2 plasma to produce an oxide of 0.5 nm followed by PECVD SiO_2 deposition and in situ anneal at 400°C at 10^{-8} torr. In the two techniques mentioned above, the interface was formed by high quality plasma oxides which underneath the native oxide, and the conventional PECVD oxides were deposited on top of the native oxide.

In this section, the SiO_2/Si interface was prepared by a direct PECVD deposition followed by RTA. It was found that the PECVD SiO_2 deposited at 250°C followed by RTA at 350°C in forming gas is capable of producing very

low surface recombination velocity and preserving high recombination lifetime in silicon.

5.1.1. Experiments

High resistivity ($> 500 \Omega \text{ cm}$) n-type $\langle 100 \rangle$ FZ silicon material was used in this study. Silicon wafers were cleaned by (a) ultrasonic degreasing in solvents (TCE, Acetone, Methanol), rinsed in running deionized (DI) water, (b) soaked in $\text{HF}(1) : \text{H}_2\text{O}(10)$ for 1 min followed by DI water rinse, (c) boiled in $\text{HCl}(1) : \text{H}_2\text{O}_2(1) : \text{H}_2\text{O}(5)$ for 8 min followed by DI water rinse, (d) soaked in agitated $\text{HF}(1) : \text{HNO}_3(50)$ for 30 sec and then rinsed immediately in DI water. Just before the PECVD deposition, the wafers were dipped in $\text{HF}(1) : \text{H}_2\text{O}(10)$ for 1 min, rinsed in running DI water for 30 sec, and blown dry with filtered nitrogen. This step was found to be critical for obtaining reproducible results. Samples were then loaded into the PECVD system for pump-down. The time lag between the drying to pump-down was typically 1 min. Silicon wafers were etched down to various thicknesses in order to measure the surface recombination velocity and bulk lifetime by photoconductivity decay (PCD) technique [6]. Heated KOH at 80°C used for thinning had an etch rate of about $6 \mu\text{m}/\text{min}$.

A commercial Plasma-Therm. 700 series reactor with 13.56 MHz rf power source was used for the PECVD deposition. The top electrode was maintained at 80°C and substrate temperature was kept at 250°C . A low power

level of 20 W (about 0.02 W/cm²) was used to prevent surface damage by ion bombardment. A mixture of 2% SiH₄ in N₂ and pure N₂O was used. The gas flow rate was 400 sccm for SiH₄, and 900 sccm for N₂O. The total reactor pressure was maintained at 0.9 Torr and the reactive gas ratio R (N₂O/SiH₄) was kept to about 110 in order to grow stoichiometric SiO₂ [7]. Thin PECVD SiO₂ (~ 100 Å) was deposited on both sides of the wafers and the samples were subjected to RTA in the temperature range of 300 - 450°C either in a forming gas or N₂ ambient. The annealing time was 10 - 30 min. The effective recombination lifetime, which includes interface recombination effects, was measured by the PCD technique. The PCD setup and measurement technique are described in detail elsewhere [6,8]. For PCD lifetime measurements, first the voltage decay transient V(t) from the PCD tester is converted to carrier concentration transient [9] and the effective lifetime τ_{eff} at various injection level is determined by

$$\frac{1}{\tau_{eff}} = -\frac{1}{N} \frac{dN}{dt} \quad (1)$$

where N is the injected carrier concentration. For low surface recombination velocity, the effective lifetime τ_{eff} , bulk lifetime τ_b , and surface recombination

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2S}{L} \quad (2)$$

where L is the sample thickness which was varied in the range of 5 to 9 mils in our measurements.

The interface state density (D_{it}) and oxide charge density Q_{ox} were determined by high frequency and quasistatic C-V measurements on MOS capacitors. The measurements were done on identical oxide deposited on 0.2 Ω -cm Si wafers, instead of the 500 Ω -cm or higher samples, because of the difficulty in MOS measurements on the high resistivity substrates.

5.1.2. Rapid Thermal Annealing of the PECVD Oxides

Fig. 5-1 shows photoconductive voltage decay curves for PECVD oxides subjected to different treatments: a) as-grown PECVD oxide with no annealing; b) PECVD oxide deposition followed by RTA in N_2 ambient; and c) PECVD oxide deposition followed by RTA in forming gas ambient. It can be seen in Figure 5-1 that the annealed PECVD oxides gave much stronger signal compared to the unannealed oxide which has very high recombination velocity at the SiO_2/Si interface. Figure 5-1 demonstrates that the RTA process is important for maintaining high effective lifetime, and the forming gas produces much better results compared to the N_2 ambient. The measured effective lifetimes were 5 ms and 100 μs for the forming gas and N_2 ambient, respectively. These results suggest that the presence of 10% hydrogen in the forming gas plays a critical

ms and 100 μ s for the forming gas and N₂ ambient, respectively. These results suggest that the presence of 10% hydrogen in the forming gas plays a critical role in improving the interface.

Figure 5-1. The experimental photoconductive voltage decay transients for the samples with different treatments: PECVD only (thin PECVD SiO₂ on Si); PECVD + N₂ (the sample annealed in nitrogen ambient); PECVD + FGA (the sample annealed in forming gas ambient). The anneals were done in RTA system.

5.1.3 A Comparison of RTA and Furnace Annealing PECVD Oxides

A comparison is also made between the furnace annealed and rapid thermal annealed samples in forming gas ambient. The annealing temperatures and time were kept the same for both cases. The lifetime dependence on RTA temperature was studied in the temperature range of 300 - 450°C. The measured effective lifetimes for furnace and rapid thermal annealed samples are listed in Table 5-1 which shows that the RTA process results in higher effective lifetime than the furnace anneal for the same temperature. The furnace anneal temperature had to be raised to come close to the RTA results. This suggests that the additional optical-heating during the RTA process makes hydrogen passivation of the interface defects more efficient. The effective lifetime is sensitive to the annealing temperature because hydrogenation of the interface defect is closely related to the temperature. Table 5-1 also indicates that the RTA annealing temperature of 350 °C is optimum, probably because annealing at higher temperature results in evolution of hydrogen rather than passivation of the interface.

Table 5-1. Temperature Effect on τ_{eff} in RTA and Furnace Anneal.

Temperature (°C)	τ_{eff} after RTA Anneal (ms)	τ_{eff} after Furnace Anneal (ms)
300	1.1	NA
350	5.5	1.0
400	4.7	4.2
450	4.1	1.6

5.1.4 Effect of Oxide Charge on Interface Recombination Velocity

Interface recombination velocity (S) and true bulk lifetime (τ_b) were determined by measuring τ_{eff} on the annealed oxidized wafers with five different thicknesses (L). Figure 5-2 shows a typical $1/\tau_{\text{eff}}$ vs $1/L$ plot where the intercept of the straight line corresponds to τ_b , and the slope gives S value. The τ_b and S were 23 ms and 2 cm/sec, respectively, at an injection level of $5 \times 10^{14} \text{ cm}^{-3}$. The S value showed an increase from 2 to 30 cm/s when the injection level was increased from 5×10^{14} to $1 \times 10^{16} \text{ cm}^{-3}$.¹⁰ It should be recognized that S is a strong function of SiO_2/Si interface state density, positive charge density in the oxide, carrier injection level, and capture cross section for electrons and holes¹¹⁻¹³. We have developed a theoretical model to calculate the effect of

the effect of these parameters on S . The low S value can be either due to low interface state density or high density of positive charge in the PECVD oxide, or a combination of both. If the positive charge density is larger than the interface state density, it will cause significant down-ward bending of the energy band, increasing the difference in electron and hole concentration in the region near the SiO_2/Si interface and resulting in reduced recombination at the interface. High-low frequency C-V measurements on the PECVD oxides showed a large flat band voltage shift with a positive charge density in the range of $5 \times 10^{11} - 1 \times 10^{12} \text{ cm}^{-2}$, and D_{it} in the range of $5 \times 10^{10} - 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at midgap. Since the C-V measurements were done on low resistivity ($0.2 \Omega\text{-cm}$) samples, D_{it} may be slightly different from the high resistivity samples used for S and τ measurements by PCD measurements. However, the positive charge in oxides may be virtually the same for both the high and low resistivity samples. Model calculations in Figure 5-3 demonstrate quantitatively the relationship between S and positive charge at an injection level of $5 \times 10^{14} \text{ cm}^{-3}$, assuming uniform interface state density with electron and hole cross-section are assumed of 10^{-14} and 10^{-16} cm^2 , [13] respectively. According to Figure 5-3, the positive charge in the range of $1-5 \times 10^{11} \text{ cm}^{-2}$ can significantly reduce the interface recombination velocity if the D_{it} in the range of $5 - 10 \times 10^{10} \text{ cm}^{-2}$. This theoretical prediction is consistent with the work of Aberle in reference [12]. Oxide charge is undesirable for integrated circuit devices because it affects the threshold and breakdown voltage, and the films reported here may

enough for CMOS applications. However, for devices such as high efficiency solar cells in which the surface recombination is of major concern rather than oxide charge, the positive charge of PECVD oxide can indeed be very helpful in reducing the interface recombination to improve device performance. It should be recognized that if the PECVD oxides are used in concentrator cells, where the injection can exceed 10^{16} cm^{-3} , the interface recombination velocity can reach as high as 30 - 60 cm/s based on our experimental measurements.

Figure 5-2. The τ_{eff} were measured on the samples with different thicknesses. The slope of $1/\tau_{\text{eff}}$ vs. $1/L$ gives the S value, and the intercept of the straight line corresponds to the τ_b .

Figure 5-3. Calculated positive charge effect on interface recombination velocity by a simplified model using uniform distribution of interface states.

5.1.5. Stability of Effective Lifetime in PECVD Oxide

The stability of the thin PECVD SiO_2/Si interface was investigated because the increase in interface recombination velocity with UV light exposure has been reported for high quality thermal oxides.[14] Some investigators have also shown that the presence of moisture near the interface increases not only negative charges in oxides but also the recombination center density at the interface.[15,16] Therefore, a protective layer on top of the oxide, such as metal contact in MOS devices or antireflection coating in solar cells, can have

significant impact on the stability. When the unprotected PECVD oxide was exposed to the air for several days the effective lifetime was found to decrease with time, as shown in Figure 5-4. The exact reason for this decay is not fully understood at this time. However, the role of moisture cannot be ruled out, since thinner oxides showed faster degradation. It is also important to note that the reduced effective lifetime can be fully restored by reannealing the oxides.

An attempt was made to prevent this degradation by depositing a PECVD SiN layer on top of the oxide. Figure 5-4 shows the variations in τ_{eff} with time for a duration of two months, for the unprotected thin SiO₂ as well as SiN protected SiO₂. In the case of unprotected SiO₂, τ_{eff} decreased from 7 ms to 3.7 ms in 3 days and to 1.5 ms in a month before stabilizing. In contrast, thin SiO₂ capped with SiN was found to be extremely stable and showed virtually no degradation for the period of two months. The SiN layer which is known to block the moisture from reaching the interface may therefore contribute to the stability improvement. It is interesting to note that the SiN layer not only successfully prevents the degradation but also gives higher effective lifetime (> 10 ms) and very low S (< 1 cm/s). A large amount of hydrogen in the PECVD SiN films, detected by FTIR,[17] along with the additional positive charge in the SiN ($\geq 10^{12}$ cm⁻²) may be responsible for such a low S and high τ_{eff} . In addition, the value of S in the SiN capped PECVD oxide only went up to 15 cm/s at the injection level of 10^{16} cm⁻³.

Figure 5-4. The degradation of effective lifetime in thin PECVD SiO_2/Si for duration of two months. The effects of PECVD SiN layer on the effective lifetime and the degradation.

5.1.6. Conclusions

It is shown for the first time that direct PECVD SiO₂ deposition at 250 °C followed by RTA at 350 °C can result in high effective lifetime (> 5 ms) and very low S (≤ 2 cm/s). Such a low temperature process retains the true bulk lifetime which was found to be 23 ms after the PECVD and RTA processes. MOS measurements coupled with model calculations confirmed that the high effective lifetime and low surface recombination velocity results from the combination of low interface state density ($\sim 5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$) and relatively high positive charge density ($5 - 10 \times 10^{11} \text{ cm}^{-2}$) in the PECVD oxide. Some degradation in the effective lifetime was observed in the thin PECVD oxides but the PECVD SiN layer cap was found to be very effective in preventing this degradation and enhancing τ_{eff} . A detailed investigation of the influence of processing parameters on the interface state and positive charge in PECVD oxides is underway. The annealing studies showed that the forming gas ambient is superior to nitrogen and the RTA is better than the conventional furnace anneal for achieving low interface recombination velocity and high effective lifetime.

5.2 Record Low SiO₂/Si Interface State Density For Low Temperature Oxides Prepared By Direct PECVD Deposition

Low temperature oxides are desirable for greater flexibility in process sequence, tight dimensional control, and preservation of minority carrier lifetime

in high-performance silicon devices. Significant progress has been made in the area of high quality low-temperature PECVD oxides. Remote PECVD and plasma oxidation has recently produced high quality SiO₂/Si interface with D_{it} ~ 1.7x10¹⁰ cm⁻²eV⁻¹ [18-20], but the direct PECVD process gives D_{it} values ~ 5x10¹⁰ cm⁻²eV⁻¹ [21,22]. These D_{it} values are slightly higher but nearly comparable to thermally grown oxides at high temperatures.

Table 5-2 summarizes some of the recent developments on PECVD oxides, along with the oxide interface formation techniques used to obtain low D_{it}. It is important to recognize that there is a fundamental difference between the deposited oxides and thermally grown oxides. In the thermally grown oxides, the SiO₂/Si interface is formed at the end of the process and is located underneath the native oxide. In the case of deposited oxides, the deposition takes place on top of the native oxide, and the native oxide stays at the interface. Consequently, the interface property of the deposited oxides depends strongly on the native oxide. Therefore, the interface formation technique is more critical for obtaining low D_{it} in the PECVD oxides.

In remote plasma-enhanced chemical vapor deposition (RPECVD), excited species from a remote oxygen plasma interact with silane in the deposition zone to avoid ion bombardment damage on the surface. In addition, the use of in situ hydrogen plasma treatment to reconstruct silicon surface just prior to the deposition was also believed to be a key factor in obtaining low D_{it} of 3.7x10¹⁰ cm⁻²eV⁻¹ [18]. Low growth rate plasma oxidation of silicon in dilute oxy-

gen/helium plasma is another promising technique described in reference [19]. In this technique, a plasma grown oxide forms a high quality interface below the original native oxide, and the conventional PECVD oxide is deposited on top of the native oxide. Thus, the interface is dominated by a good quality plasma grown oxide rather than the native oxide or the PECVD oxide. A low D_{it} value of $2.2 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$ was reported by this technique [19]. Yasuda et al [20] showed that the combination of remote PECVD and plasma oxidation technique, along with wet HF etching of native oxide just prior to the deposition, can produce D_{it} as low as $1.7 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$, which is comparable to oxides prepared by thermal oxidation.

Even though the RPECVD and plasma oxidation techniques have successfully produced low D_{it} , it may be difficult to grow such oxides in a commercial PECVD reactor because very low pressure ($< 10^{-8}$ torr) is required [18,20], and the growth rate is very slow ($\sim 3 \text{ \AA/min}$)². On the other hand, direct PECVD is more desirable for commercial scale reactors because it can be works at 0.1 - 1 torr pressures and the deposition rate is few hundred angstrom per minute. Batey and Tierney [21] first reported that low-temperature direct PECVD could result in an interface with D_{it} in the range of mid 10^{10} to $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ by using relatively low growth rate, $60 \text{ \AA/min}$, rather than $500 \text{ \AA/min}$ growth rate in the conventional PECVD. Herman and Terry [22] developed a two temperature PECVD technique, in which the interface was formed at 300°C and the bulk of the film was formed at 350°C . Hydrogen plasma treatment

during the temperature ramp was found to be important for the low D_{it} , and the D_{it} value $\sim 5 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ was reported.

In most previous studies on low temperature PECVD oxides [18-22], attention was focused on the interface formation technique during the oxide growth rather than on the post-deposition treatments. Photo-assisted anneal has been used to improve electrical characteristics of various materials [23,24], including the interface state density in GaAs [25]. However, the exact defect passivation mechanism due to such anneal is not yet fully understood. In this study, photo-assisted anneal was used to reduce D_{it} at the SiO_2/Si interface. Recently, we showed that the deposition of PECVD oxides on high resistivity Si, followed by photo-assisted anneal in a rapid thermal system, can result in a very high effective minority carrier lifetime ($> 5\text{ms}$) and very low interface recombination velocity ($\sim 2\text{cm/sec}$) [26]. In that study, we also showed that the photo-assisted anneal was superior to furnace anneal, and a forming gas ambient was better than nitrogen ambient for achieving low interface recombination velocity.

5.2.1 Experiments

In this investigation, direct PECVD in conjunction with photo-assisted anneal was used to achieve low interface state density in MOS (Al/oxide/Si) structures. P-type $\langle 100 \rangle$ FZ silicon wafers with $\sim 10 \text{ }\Omega\text{-cm}$ resistivity were used. The front side of the wafers was mechanically polished and the back

side was chemically etched. Prior to oxide deposition, the wafers were cleaned as follows: (a) ultrasonic degreasing in solvents (TCE, Acetone, Methanol), followed by running deionized (DI) water rinse; (b) soak in HF(1) : H₂O(10) for 1 min and DI water rinse; (c) boil in HCl(1) : H₂O₂(1) : H₂O(5) for 8 min followed by DI water rinse; and (d) soak in agitated HF(1) : HNO₃(50) for 30 sec followed by DI water rinse. Just before the PECVD deposition, the wafers were dipped in HF(1) : H₂O (10) for 1 min, rinsed in running DI water for 30 sec., and then blown dry with N₂. This step was critical for obtaining reproducible results and mitigating the undesirable effects of the native oxide on the interface. Samples were then loaded into the PECVD system for pump-down. The time lag between the drying to pump-down was typically 1 min. A commercial Plasma-Therm 700 series reactor with 13.56 MHz rf power source was used for the PECVD deposition. The top electrode was maintained at 80°C and the substrate temperature was kept at 250°C. A low power level of 20 W (about 0.02 W/cm²) was used to prevent surface damage by ion bombardment. A mixture of 2% SiH₄ in N₂ and pure N₂O was used in the reaction chamber. The gas flow rate was 100 sccm for SiH₄ and 250 sccm for N₂O. The total reactor pressure was maintained at 0.3 torr. Under these conditions the growth rate was about 100 Å/min. About 500 Å PECVD SiO₂ was deposited on the front side of the wafers followed by thermal evaporation of 2000 Å aluminum for the front gate electrode and back-side contact. The samples were then subjected to photo-assisted anneal in a rapid thermal processing system at a temperature

of 350°C in a forming gas ambient for 20 min. The system is heated by tungsten halogen lamps. All the experiments in this study were conducted in a class 1000 clean room. The interface state density was determined by the conventional high-low frequency capacitance-voltage (C-V) measurements. The high frequency (HF) C-V was measured at 1 MHz, and quasi-static (QS) C-V was measured by voltage ramp method with a ramp rate of 0.1 V/sec.

5.2.2 Results and Discussions

Three sets of samples with identical PECVD deposition but with different post-deposition treatments were tested to evaluate the effect of post-deposition treatments on interface state density. The first set of samples, which saw no treatment at all after the PECVD deposition, gave D_{it} values of above $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. The second set samples were subjected to photo-assisted anneal in forming gas without the aluminum layer on top of the oxide and the aluminum gate electrode with size of 0.785 mm^2 was evaporated after the anneal. Figure 5-5a shows typical high-low frequency C-V curves for group 2 MOS capacitors which gave an average D_{it} value of $4.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. The third set was subjected to photo-assisted anneal in forming gas after the aluminum electrode was evaporated on top of the oxide. Typical high-low frequency curves are shown in Figure 5-5b. The third set gave a typical D_{it} value of $\sim 3.3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ with the best D_{it} value of $1.1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ at midgap which is comparable to the thermal oxides. However, the positive charge in these PECVD oxides was

of the order of 10^{11}cm^{-2} , which is much higher than the thermal oxides. Figure 5-5a and 5b clearly demonstrate the beneficial effect of aluminum during the photo-assisted anneal, because it reduces the D_{it} value by more than one order of magnitude. The merit of having an aluminum layer during annealing process has also been reported for thermal oxides [27]. It has been suggested that the presence of Al helps to generate atomic hydrogen during forming gas anneal [27] which ties up the dangling bonds and reduce D_{it} . Our results in Figures 5-5a and 5b show that the PECVD oxides also respond favorably to the presence of aluminum during the anneal. It should be mentioned that there is some spread in the D_{it} values from MOS capacitors located on the same wafer. The range of midgap D_{it} value for the samples treated by photo-assisted anneal with an aluminum layer was $1 - 4 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$. Figure 2a shows the best C-V characteristics measured in this study on a MOS capacitor with the PECVD oxide. The near-ideal C-V curve endorses the excellent interface quality. The D_{it} spectrum calculated from the high-low frequency curves of Figure 5-6a is shown in Figure 5-6b, which shows a minimum D_{it} value of $1.1 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ at the midgap. This represents the lowest D_{it} value achieved to date for the PECVD oxides. Samples were also subjected to conventional furnace anneal at 400°C in the forming gas for 30 min after the PECVD oxide deposition and aluminum evaporation. The D_{it} value for these samples was found to be in the range of 4×10^{10} to $10^{11} \text{ eV}^{-1}\text{cm}^{-2}$, with the lowest value of $4.2 \times 10^{10} \text{ eV}^{-1}\text{cm}^{-2}$. These values are consistent with the results reported in reference [4]. From the

comparison between the furnace and photo-assisted anneal experiments it is clear that optical-effect during the photo-anneal process also played a key role in reducing D_{it} in this study. This result is consistent with our earlier study on effective minority carrier lifetime [26] which gave higher effective lifetime in the photo-assisted annealed samples compared to the furnace annealed samples. Some investigators have attributed the positive effects of photo-anneal to the electronic excitations which can promote additional reactions [23]. At this time we cannot explain the exact mechanism. In addition to the PECVD growth conditions, photo-assisted anneal, use of Al layer, and forming gas ambient, careful wafer and PECVD chamber cleaning was critical for achieving low interface state density. We found that a dirty PECVD chamber can result in a D_{it} value greater than $10^{11} \text{ eV}^{-1}\text{cm}^{-2}$, with all other conditions being the same.

Figure 5-5 The measured high frequency (HF) and quasi-static (QS) C-V on MOS capacitors, in which the PECVD oxide was annealed in forming gas ambient without an aluminum layer (a); and in which the oxide was annealed in forming gas with an aluminum layer (b).

Figure 5-6. (a) The HF and QS C-V data for the best MOS capacitor measured on PECVD oxide; and (b) the corresponding D_{it} spectrum showing minimum D_{it} around midgap of $1.1 \times 10^{10} \text{eV}^{-1}\text{cm}^{-2}$.

Table 5-2. A Summary of the Interface Formation Techniques and the Corresponding Best Values of Interface State Density, D_{it} , for Low Temperature Oxides.

Ref./year	Interface formation technique	T_{dep} °C	Post-anneal condition	D_{it} $cm^{-2}eV^{-1}$
1/1988	remote PECVD, in situ hydrogen plasma treatment	300	400°C in N_2 30 min	3.7×10^{10}
2 /1991	low-rate plasma oxidation	350		2.2×10^{10}
3/1992	remote PECVD, wet HF etching, plasma oxidation		400°C in 10^{-8} torr, 5min 400°C in N_2 , 30 min	1.7×10^{10}
4/1986	direct PECVD, slow rate (60 Å/min)	350	400°C in forming gas, 30 min	4×10^{10}
5/1991	direct PECVD, two-temperature, in situ H plasma treatment	300- 350	300°C in forming gas, 60 min	$5.3 \times 10^{10}(p)$ $4.0 \times 10^{10}(n)$
this study	direct PECVD, wet HF etching deposition-rate (100 Å/min)	250	photo-assistant ann. 350°C in forming gas, 20 min	1.1×10^{10}

5.2.3 Conclusions

In conclusion, the importance of post-deposition treatment for PECVD oxide is highlighted in this study. It is shown that the combination of photo-assisted anneal, forming gas ambient, and the presence of aluminum layer during the anneal is a very effective post-deposition treatment for Si/SiO₂ interface defect passivation. Without any post-deposition treatment, PECVD oxides gave a D_{it} value $\sim 10^{12} cm^{-2}eV^{-1}$. Photo-assisted anneal at 350 °C in

forming gas reduced the D_{it} value to $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$. Finally, the photo-assisted anneal in forming gas with the Al layer on top of the oxide gave D_{it} in the range of $1 - 4 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ with the best D_{it} value of $1.1 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$. This sets a new record for the lowest D_{it} in direct PECVD oxides fabricated to date.

5.3 A NOVEL AND EFFECTIVE PECVD SiO_2/SiN AR COATING FOR Si SOLAR CELLS

5.3.1. Introduction

Recent studies [28-34] have shown that the application of PECVD-SiN thin film can be very helpful in improving the efficiency of poly-silicon solar cells. It not only acts as an antireflection coating layer with a suitable refractive index, but can also improve the performance of photovoltaic devices by defect/surface passivation. This is because a large amount of atomic hydrogen is produced during PECVD process. In addition, PECVD is a low temperature process (about 300°C) compared to other CVD processes (LPVCD or APCVD), and has high throughput, good uniformity, better thickness control ($< 5\%$), and excellent reproducibility, compared to the physical evaporation techniques. All these advantages make PECVD-SiN film very attractive for solar cells. Double layer MgF_2/ZnS [8] antireflection coating (AR coating) is often used in high efficiency single crystal silicon cells fabricated in the laboratory today because it has much better antireflection properties than that of the single layer SiN

coating. MgF_2 has a refractive index of 1.35 and ZnS has an index of 2.4. Refractive index of stoichiometric silicon nitride (Si_3N_4) is around 2.0, and therefore is not as suitable for a double layer AR coating as ZnS . On the other hand, PECVD SiN is an amorphous form of $\text{Si}_x\text{N}_y\text{H}_z$, in which x, y and z strongly depend on the deposition conditions, especially on gas flow ratio of NH_3/SiH_4 and substrate temperature. The refractive index of SiN depends on the ratio of N/Si in the film, and can be controlled in the range of 1.96 - 3.5 by adjusting the ratio of NH_3/SiH_4 . Thus the PECVD process provides an opportunity for obtaining higher index SiN film by making it silicon rich. However, silicon rich films generally show high absorption; therefore absorption losses must be considered when the higher index of SiN films is used.

The improvements in the minority carrier diffusion length and quantum efficiency due to single layer PECVD SiN on poly-Si solar cells have been reported [29-31], in addition to the beneficial effects on short circuit current, open circuit voltage, and cell efficiency [32-34]. However, the defect or surface passivation effects due to double layer PECVD SiO_2/SiN coating on single crystal silicon cells have never been investigated. In the case of poly-Si, there is significant bulk recombination due to high concentration of unwanted impurities, dislocation, point defects, and grain boundary defects. There are relatively fewer bulk recombination centers in high quality float-zone single crystal Si compared to poly-Si, therefore surface recombination becomes an important loss mechanism. In this section, a novel SiO_2/SiN double layer

coating is prepared by sequential PECVD deposition of SiN and SiO₂ on single crystal Si solar cells. The thickness and refractive index of the SiN film is tailored for the best performance. Improvements in reflectivity and cell performance are compared with the conventional MgF₂/ZnS double layer AR coating, which was deposited by thermal evaporation. The loss due to photon absorption in the SiO₂/SiN is analyzed by internal quantum efficiency (IQE) measurements, and the defect/surface passivation due to PECVD SiO₂/SiN coating is quantified in terms of reverse saturation current J₀ and open circuit voltage V_{oc}. It is shown that in spite of some absorption in the PECVD SiO₂/SiN coating, the net improvement in the cell performance is greater compared to the MgF₂/ZnS coating due to defect/surface passivation feature of the SiO₂/SiN films.

5.3.2. Experiments

PECVD SiN and SiO₂ films were prepared in a Plasma-Therm Inc reactor (series 700) operated at 13.6 MHz. SiH₄, NH₃, N₂ gases were used for SiN deposition, and SiH₄, N₂O, N₂ gases were involved in SiO₂ deposition. The reactor pressure was held at 0.9 Torr for both depositions. Substrate temperature was 300°C and the rf power was 30 and 20 W for the SiN and SiO₂ deposition, respectively. These conditions resulted in growth rate of about 100 Å/min for SiN, and 300 Å/min for SiO₂. Baseline n⁺-p-p⁺ solar cells were fabricated by conventional phosphorus diffusion on the front and Al treatment

on the back of P-type (0.2 ohm-cm) Float Zone (100) silicon substrates. The details of the fabrication procedure are given in reference [36]. The refractive index and thickness of the deposited films were measured by an ellipsometer. The solar cells were characterized by a combination of light and dark I-V, reflectivity, spectral response, and internal quantum efficiency measurements before and after the AR coating to evaluate the change in the cell parameters. Several 1x1 cm cells were fabricated on 3" diameter wafers and were isolated by mesa etching. A few cells on each wafer were coated with MgF_2/ZnS while others were coated with SiO_2/SiN for the controlled comparison of the two coatings. Thus all the cells experienced the same fabrication sequence, except for the difference in the AR coating at the end. During the physical evaporation of MgF_2/ZnS and PECVD deposition of SiO_2/SiN , selected areas on the wafers were covered by thin glass plates to simultaneously obtain AR coated glass plates. In order to assess the effect of photon absorption in the coatings, the IQE of the same cell was measured three times, first with an uncoated glass plate on the top of the cell, and then with the glass plates coated with MgF_2/ZnS and SiO_2/SiN coatings, respectively. Since the reflectance effects are removed in the IQE measurement, any change in the IQE of the cell corresponds to the absorption in the coating.

5.3.3. Results and Discussions

The refractive index of PECVD SiN was adjusted by controlling the

NH_3/SiH_4 gas flow ratio. We were able to vary the index in the range of 3.5 - 1.9 in our reactor. Since an index of 2.4 is desirable, this flexibility allowed PECVD SiO_2/SiN to be effectively used as a double layer AR coating. It was found that the use of higher index SiN in the SiO_2/SiN coating significantly reduced the reflection losses (Figure 5-7), but it also resulted in higher absorption loss due to the silicon rich SiN film. Thus a compromise has to be made between the reflection and absorption losses to optimize the index of AR coating. AR coating model calculations showed that 590 Å thick SiN with an index of 2.3, in conjunction with 950 Å thick SiO_2 with an index of 1.45, should give fairly low average reflectance over the entire solar spectrum. It was confirmed experimentally in this study that a 590 Å thick SiN film with refractive index of about 2.3, underneath a 950 Å PECVD SiO_2 with an index of 1.45, indeed gave the highest J_{sc} . Use of higher index (>2.3) SiN film resulted in lower reflectance in the short wavelength range but higher reflection in the long wavelength range, along with higher absorption loss. Figure 5-7 shows a comparison of the reflectance data for a single layer SiN film ($n=2.0$, $T=700$ Å); a double layer SiO_2/SiN , ($n=1.45$, $T=950$ Å)/($n=2.3$, $T=590$ Å); and a double layer MgF_2/ZnS ($n=1.38$, $T=1100$ Å)/($n=2.3$, $T=550$ Å). Figure 5-7 shows that both the double layer coatings have excellent antireflection properties, with less than 5% reflection in the entire wavelength range of 400 - 1100 nm. The SiO_2/SiN coating shows a slightly higher reflection than the MgF_2/ZnS coating in the range of 450 - 700 nm, partly because SiO_2 has higher

refractive index (1.45) than MgF_2 (1.38). Unlike the PECVD SiN, the refractive index of PECVD SiO_2 is difficult to change, especially below 1.4.

Table 5-3 shows a comparison of the effects of the two AR coatings on Si cells, without the SiO_2 surface passivation. Several runs were made to check the reproducibility of these results. Table 5-3 shows a typical change in the cell parameters and clearly demonstrates that this novel SiO_2/SiN coating gives remarkably large increase in the cell parameters, 57% in J_{sc} , 8% in V_{oc} , and 66% in Eff of the unpassivated cells. The counterpart MgF_2/ZnS gave only 50% improvement in J_{sc} , 2% in V_{oc} and 54% in Eff.

The maximum improvement in J_{sc} , $(\Delta J_{sc}/J_{sc})$ due to an antireflection coating, assuming IQE does not change, can be estimated by

$$\frac{\Delta J_{sc}}{J_{sc}} = \frac{R-R'}{1-R} \quad (3)$$

where R and R' are the average reflectivities before and after the coating, respectively. If we assume $R = 35\%$ for the uncoated Si, based on our reflectivity measurements, and $R' = 0$, the maximum improvement due to perfect AR coating should be only 53%. Therefore, the observed 57% improvement in the J_{sc} in Table 5-3 suggests that defect/surface passivation due to SiO_2/SiN might contribute toward greater than 53% improvement in J_{sc} . The passivation due to SiO_2/SiN coating was indeed confirmed by the measurement of saturation current density J_0 from the detailed dark I-V

analysis. Table 5-3 shows a significant reduction in the J_o due to the PECVD SiO_2/SiN which also accounts for the remarkably high increase in V_{oc} . Assuming a near ideal float zone silicon cell, the increase in V_{oc} can be estimated by

$$\Delta V_{oc} = \frac{KT}{q} \left[\ln\left(\frac{J'_{sc}}{J_{sc}}\right) + \ln\left(\frac{J_o}{J'_o}\right) \right] \quad (4)$$

where J_{sc} and J_o represent the short circuit and reverse saturation current densities before AR coating, and J'_{sc} and J'_o are the corresponding values after the coating. The calculated improvement in V_{oc} of 15 mV for MgF_2/ZnS coating and 44mV for SiO_2/SiN coating, using measured J_{sc} and J_o , are in good agreement with the measured increase in V_{oc} of 12mV and 48mV, respectively. It should be noted in Table 5-III that the improvement in V_{oc} and J_o is much greater for the SiO_2/SiN coated cells compared to the MgF_2/ZnS coated cells.

Table 5-4 shows improvement in cell parameters of those cells which had thin SiO_2 surface passivation prior to the AR coating. It is interesting to note that the absolute value of J_{sc} was virtually same after both the AR coatings, even though the SiO_2/SiN coating has slightly higher reflection. Equally important is the fact that the PECVD SiO_2/SiN coating again gave larger improvements in V_{oc} and J_o , even when the cells had oxide passivation. However, the relative improvement was much smaller than the case when no oxide passivation layer was present.

The external spectral response (SP) of the cells, before and after deposition of SiO_2/SiN and MgF_2/ZnS coatings, is shown in Figure 5-8. As expected, coated cells showed much better external spectral response. It is noteworthy that the coated cells have a slightly lower response in the wavelength range of 300 - 375 nm due to the absorption in both the coatings at higher energy. In order to separate antireflection and defect passivation effects, internal quantum efficiency (IQE) was calculated ($\text{IQE} = \text{SP}/(1-R)$), which is independent of the reflection properties. Figure 5-9 shows the comparison of the IQE of SiO_2/SiN and MgF_2/ZnS coated cells. Note that the IQE of MgF_2/ZnS coated cell is much higher in the wavelength range of 300 - 500 nm, but the IQE of SiO_2/SiN cell is slightly higher beyond the 500 nm, including higher maximum (IQE_{max}). The observed higher IQE of the MgF_2/ZnS cell in the short wavelength region could result from either lower front surface recombination in the MgF_2/ZnS coated cell or higher absorption loss in the SiO_2/SiN coated cell. If the former were true, it would be difficult to explain the higher IQE_{max} in the SiO_2/SiN coated cell, which is strongly related to the surface recombination [37]. Therefore, absorption due to the higher refractive index SiN is the more probable cause. To confirm this hypothesis, IQE of a cell was measured three times, first by covering the cell with a glass plate, and then by covering it with glass plates coated with the SiO_2/SiN and MgF_2/ZnS double layer coatings, respectively. Since the same cell was used in these three measurements, surface and bulk recombination should be identical and should

not contribute to the observed difference in IQE. Most likely the cause of any perceived difference should be the absorption in the films. Figure 5-10 shows that both the coated plates have higher absorption than the uncoated plate in short wavelength range, below 400 nm. The IQE data in Figure 5-10 clearly shows that much higher absorption occurs in the SiO_2/SiN coating compared to MgF_2/ZnS coating below 500 nm. However, the absorption is very low for the wavelengths above 600 nm, which agrees with an independent absorption measurement by multiple angle ellipsometry at a wavelength of 630 nm. These results confirm that the lower IQE of SiO_2/SiN cell in the short wavelength region is caused by the absorption. The surface passivation effect of SiO_2/SiN is unable to counterbalance the absorption loss in the short wavelength; therefore, a crossover occurs in the IQE response. The higher maximum value of IQE for the SiO_2/SiN coated cell supports the notion of SiO_2/SiN induced defect/surface passivation.

Figure 5-7. Reflectance as a function of wavelength for silicon cells with (a) SiN AR coating, (b) double layer MgF_2/ZnS coating, and (c) SiO_2/SiN AR coating. The thickness and refractive index of the films are in text.

Figure 5-8. The spectral response of the silicon cells: (a) without AR coating, (b) with the double layer SiO_2/SiN coating, and (c) with MgF_2/ZnS coating.

Figure 5-9. The internal quantum efficiency (IQE) of the SiO₂/SiN and MgF₂/ZnS coated cells.

Figure 5-10.

The measured IQE of the same cell covered with: (a) a clear glass plate, (b) glass plate coated with the SiO₂/SiN, and (c) glass plate coated with the MgF₂/ZnS double layer AR coating.

Table 5-3. Change in Cell Parameters of the Unpassivated Solar Cells after the SiO_2/SiN and MgF_2/ZnS Antireflection Coatings.

MgF ₂ /ZnS coating					
ID	J _{sc} (mA)	V _{oc} (V)	FF	Eff(%)	J _o (A)
before	22.71	0.600	0.78	10.63	6.3x10 ⁻¹³
after	34.29	0.612	0.771	16.34	5.2x10 ⁻¹³
improvement	50%	2%		54%	

SiO ₂ /SiN coating					
ID	J _{sc} (mA)	V _{oc} (V)	FF	Eff(%)	J _o (A)
before	22.42	0.602	0.781	10.53	6.0x10 ⁻¹³
after	35.47	0.650	0.76	17.52	1.7x10 ⁻¹³
improvement	57%	7.9%		66%	

Table 5-4. Change in Cell Parameters of the Oxide Passivated Cells after the SiO_2/SiN and MgF_2/ZnS Coatings.

MgF ₂ /ZnS coating					
ID	J _{sc} (mA)	V _{oc} (V)	FF	Eff(%)	J _o (A)
before	24.32	0.630	0.756	12.19	₁₃ 2.58x10 ⁻
after	35.71	0.642	0.807	18.55	₁₃ 2.48x10 ⁻
improvement	46.8%	1.9%		52%	

SiO ₂ /SiN coating					
ID	J _{sc} (mA)	V _{oc} (V)	FF	Eff(%)	J _o (A)
before	24.14	0.633	0.7959	12.16	₁₃ 2.47x10 ⁻
after	35.69	0.657	0.804	18.87	₁₃ 1.46x10 ⁻
improvement	47.8%	3.7%		55%	

5.3.4 Conclusion

A novel PECVD SiO_2/SiN double layer antireflection coating has been developed which gives greater than 55% improvement in the efficiency of the oxide passivated single crystal Si cells, and about 66% increase in the performance of the unpassivated cells. The optimized PECVD SiO_2/SiN coating consists of 590 Å thick SiN with an index of 2.3 under a 950 Å thick SiO_2 with an index of 1.45. The properties of this novel coating are compared with one of the best and frequently used MgF_2/ZnS double layer AR coating. The reflectivity of the SiO_2/SiN coating is slightly higher but comparable to that of the MgF_2/ZnS coating. The defect/surface passivation due to the PECVD SiO_2/SiN deposition was supported by the decrease in J_0 , and increase in V_{oc} and IQE. Even though the SiO_2/SiN coating has higher absorption and reflection losses compared to the MgF_2/ZnS coating, the passivation effect of the PECVD films results in higher V_{oc} and overall cell efficiency. The passivation feature of the PECVD coating significantly reduces the gap between the oxide passivated and unpassivated cells. Therefore; it is possible to realize both passivation and AR coating by the PECVD technique proposed in this paper for a commercial cell process. Finally, cell efficiency improvement due to the SiO_2/SiN coating depends on the front surface recombination velocity, S_f , before the AR coating deposition. The larger the S_f , the higher the relative improvement due to the PECVD coating.

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6.0 STATUS OF EDUCATIONAL ACTIVITIES AND ESTABLISHMENT OF ESP LAB

The Center's fabrication laboratories are situated on the ground floor of the Van Leer building which houses the department of electrical and computer engineering. This clean room space is shared with the surface sciences laboratory and the MBE material growth laboratory. A floor plan of the Van Leer Facility is shown in Figure 6-1. The Center laboratory is divided into two segments. The first is the silicon fabrication lab. This lab is 729 square feet and contains all the necessary equipment for processing solar cells. The majority of the fabrication for the work covered in this report was carried out in this lab.

Figure 6-2 shows the layout for the new Education Support Lab. This lab will add an additional 810 square feet of processing area to our existing capability. The majority of the equipment for the lab has been procured and delivered. Some of the smaller pieces have even been installed in areas such as the fabrication lab so that they can be used until the ESP lab is completed. A list of the equipment its approximate dollar value and its status is listed in Table 6-1. The addition of this facility to the existing capability represents a total of over 2,700 square feet at Georgia Tech dedicated to research and development for photovoltaic materials and devices. This also represents over one million dollar investment by Georgia Tech toward research in photovoltaics.

When operational, this lab will maintain 18-20% efficient cell fabrication line, provide hands-on training to the graduate and undergraduate students, and assist other qualified university PV research programs in the country. A

brochure that details the centers objectives, programs and capabilities, has been prepared and distributed to interested parties. Appendix B is a copy of the brochure.

Van Leer Clean Room Facility

Figure 6-1. Floor plan of the Van Leer Clean Room Facility at Georgia Tech.

Educational Support Lab (810 Square Feet Usable Area)

Figure 6-2. Schematic diagram of proposed layout for new Educational Support Lab.

Table 6-1. ESP Lab Equipment

Equipment	Status
CVC Evaporator (118K)	Delivered
Tystar 4-Stack Furnace (121K)	Delivered
Technic Plating Station (10K)	Delivered, Placed in lab
Quintel Aligner/Exposure (33K0	Delivered, Installed (temporary)
SPEC Wet Processing Station (15K)	In production
Tempress 602 Dicing Saw (5K)	Delivered, Installed
Solitec Spinner (Donated)	Delivered
SCS Spinner (5.3K)	Delivered

In addition to the ESP lab and training provided a graduate level course is taught on solar cells. Appendix C is an outline for the course. Undergraduate projects are assigned to demonstrate PV applications and there are currently 10 PhD students associated with the PV research activities.

As part of its educational activities the center has received a number of visits from investigators representing companies and educational institutions in Europe, Australia, Japan, and India. A list of these visitors can be found in Table 6-2. The University PV Center also hosted two visiting scientists, one from Japan and one from the Netherlands. In addition, Georgia Tech has formed a working relationship with others from within the international PV community. A listing is given in Table 6-3. These relations and visits have resulted in fruitful collaborations. The results are expected to be published at various conferences and publications in the coming months.

Table 6-2. Visitors to the Center in 1993.

5-25-92 to 3-24-93	Dr. Kiyoshi Yasutake Dept. Precision Engineering Osaka University Osaka, Japan	Interface density of states for PECVD oxides and nitrides on silicon.
1-21-93 to 1-22-93	Dr. Rob A. Steeman Dr. Peter Lollgen Netherlands Energy Research Foundation ECN	Quantification of back surface fields for poly and single crystal silicon.
2/93	Dr. B.D. Sharma Bharat Heavy Electricals New Dehli, India	Thin film photovoltaic materials for modules.
2-5-93	Dr. Brent Sorensen Roskilde University Roskilde, Denmark	Modeling of photovoltaic mod- ules.
3-13-93 to 4-3-93	Cor Leguit Graduate Student Netherlands Energy Research Foundation ECN	Surface passivation using PECVD deposited films.
5-17-93	Dr. Andrew Blakers Australian National University Canberra, Australia	High efficiency solar cells.
5-17-93	Professor Martin Green Australian National University Kensington, Australia	High efficiency solar cells and modules.
5-17-93	Dr. Joachim knobloch and Dr. Roland Schindler Franhofer Institute for Solar Energy Systems	Single and multicrystalline silicon solar cells.
5-15-93 to 5-16-93	Dr. Tsuyoshi Uematsu Hitachi Research Laboratory Tokyo, Japan	Single and multicrystalline silicon solar cells.

Table 6-3. External Collaborations

Name	Affiliation
J. Levine	Texas Instruments
J.P. Kaljes, R. Bell	Mobil Solar Corporation
M. Narayanan, R. Arya	Solarex Corporation
J. Gee, P. Basore, D. Ruby	Sandia National Labs
B. Sopori, K. Emery, T. Cisek	National Renewable Energy Labs
K. Mitchell	Seimens Solar
V. Kumer	IUP
R. Schwartz	Purdue University
D. K. Schroeder	Arizona State University
P. Logan, C. Leguit	Netherlands Energy Research Foundation, ECN
K. Misra	MEMC Corporation
H. Nussbaumer	University of Konstanz, Germany
K. Kenko	Osaka Titanium
S. Estreicher	Texas Tech
A.W. Smith	Georgia Tech Research Institute

APPENDIX A

Process Sequence for Simple Base Line Cells (SBLC)

- Step 1. Sample Identification
- Step 2. Initial Sample Cleaning
- Step 3. Phosphorus Diffusion
- Step 4. Emitter Etch Back
- Step 5. Wafer Cleaning for Aluminum Treatment
- Step 6. Aluminum Evaporation on the Back Side
- Step 7. Aluminum Treatment
- Step 8. Lift-off for Front Metallization
- Step 9. Back Metallization
- Step 10. Silver Plating
- Step 11. Anneal
- Step 12. Mesa Etch
- Step 13. Test
- Step 14. AR Coating
- Step 15. Test

Run ID

- Run ID:
- Engineer/Student:
- Starting Date:
- Finish Date:

- Purpose of the run:

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- Preliminary Information:

It is recommended to wear a pair of glasses, face mask and two pairs of gloves
Never mix the solvents and acids
Never pour water into concentrated acid
Only quartz, teflon, or plastic containers should be used throughout the fabrication sequence
Teflon beakers should be used during cleaning processes involving HF
Never clean "Lerloy" tweezers with sulfuric acid (explosion)
Make sure DI water resistivity always reads greater than 18 MΩ
Make sure the hood is on
Cover the hood work area with clean wipers before you start processing
Always keep tweezers in a clean beaker with DI water
Never pour the solvents in the sink
Pour the solvents in the proper container for disposal
Solvents include Acetone, Methanol, TCE, Chlorobenzene,...
Water should be running in the sink when you pour the solution out
Rotate the beakers as you pour the acid solution in the sink
After cleaning, wafers should not be exposed to air too long
Never use acids near silverplating solution
Always clean after yourself
Return your beakers to the proper place
Always sign in and sign out for all equipment that you use
If you make a mistake you should tell the process engineer

1. Sample Identification

At the beginning of all runs the samples are to be identified with a number or other identification scribed on the unpolished side.

- Number of Wafers.....
- Samples ID.....

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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Beaker Cleaning

1. Rinse the beaker with DI water for 5 min.
2. Rinse the beaker in 20:1 H₂O:HF for 2 min.
3. Rinse the beaker with DI water for 5 min.

If your are using the beakers for the first time clean them with 3:1 HCL:HNO₃ FOR 1 hour.

2. Initial Sample Cleaning

a) DI rinse		3 min.	
b) $H_2SO_4 : H_2O_2$	4:1	5 min.	
c) DI rinse		3 min.	
d) $HF:HNO_3$	1:20	7 min.	Teflon beaker
e) DI rinse		3 min.	
f) $H_2O:H_2O_2:HCl$	5:2:2	15 min.	Boiling
or ($H_2O:H_2O_2:HCl$)	1:1:1	15min	Boiling
g) DI rinse		3 min.	
h) $HF:H_2O$	1:10	2 min.	Teflon beaker
i) DI rinse		3 min.	

2.1 Wafer Clean Before Any Diffusion

a) DI rinse		3 min.	
b) $H_2SO_4 : H_2O_2$	4:1	5 min.	
c) DI rinse		3 min.	
f) $H_2O:H_2O_2:HCl$	5:2:2	5 min.	Boiling
or ($H_2O:H_2O_2:HCl$)	1:1:1	5min	Boiling
g) DI rinse		3 min.	
h) $HF: H_2O$	1:50	5 sec	Teflon beaker
i) DI rinse		3 min.	

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

3. Phosphorus Diffusion

- Use the proper rod for phosphorus diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Move the dummy wafers to the sides of the boat
- Load your wafers with front side facing the phosphorus source
- Use a high resistivity wafer between two sources (diffusion on both sides)
- The high resistivity wafer is used to check lifetime and J_{oe} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Leave the end cap loose
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

● Baseline diffusion:

Insert at 500° C and ramping up to 930° C

Diffusion at 930° C for 25 min.

Measured sheet resistance should be around 20 $\Omega/\square$

- Sheet resistance after phosphorus diffusion:..... $\Omega/\square$
- PCD lifetime of high resistivity phosphorus diffused sample

- a. Effective lifetime μsec
- b. Bulk Lifetime μsec
- c. J_{oe} A/cm^2

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

4. Etch Back

HNO₃:HF(diluted 100 times) 10:1

Sheet resistance after etch back should be around 70-80 Ω/□

● Measured sheet resistance.....Ω/□

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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5. Wafer Cleaning for Aluminum Treatment

a) DI rinse		3 min.	
b) $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2$	4:1	5 min.	
c) DI rinse		3 min.	
d) $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$	5:2:2	15 min.	Boiling
or ($\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$)	1:1:1	15min	Boiling
e) DI rinse		3 min.	
f) $\text{HF}:\text{H}_2\text{O}$	1:10	2 min.	Teflon
g) DI rinse		3 min.	

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

6. Aluminum Evaporation on the Back Side

- Use aluminum designated plate for Al evaporation
- Use the proper boat for Al evaporation
- Cut Al wires using a clean cutter seven inches in length
- Put the Al designated plate in the evaporator and evaporate Al on it, then open the bell jar and turn the plate so that the Al deposited side (clean side) facing up
- Put the wafers on the top of the clean side of the plate
- Follow the Bio-rad evaporator manual
- For best result the pressure should be below 5×10^{-7} torr
- Evaporate 1.0-1.5 μm aluminum

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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7. Aluminum Treatment

- Use the proper rod for aluminum diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Use a high resistivity wafer to check the lifetime of aluminum furnace
- Use a high resistivity wafer with aluminum evaporated on both sides
- The high resistivity wafer is used to check lifetime and J_{ob} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert in Oxygen at 875°

Diffusion at 875° C, 10 min. O₂ , 30 min. N₂

Ramping down to 400° C in N₂

Annealing in Forming Gas for 60 min. at 400° C

- PCD lifetime of high resistivity aluminum diffused sample

- a. Effective lifetime μ sec
- b. Bulk Lifetime μ sec
- c. J_{oe} A/cm²

- Evaporate Al on the back side

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

8. Lift-off for Front Metallization

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) ;spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer,"1400-31 Shipley"
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C , 30 min.
 - f) UV Expose; 50 sec.
 - g) Chlorobenzene (Fisher Scientific) ; 10 min., Nitrogen blow dry
 - h) Soft Bake; 95° C , 10 min.
 - i) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - j) DI rinse, Blow dry
 - k) Soft Bake; 95° C , 10 min.
 - l) BOE Etch; 60-90 sec.
 - m) DI rinse, Blow dry
 - n) Soft Bake; 95° C , 2 min.
 - o) Evaporate titanium and silver:
 - Use the proper plate and boat
 - Put two silver shots in each boat
 - For best result the pressure should be below 5×10^{-7} torr
 - Evaporate Ti 600 Å/pd 400 Å/Silver 600 Å on the back surface
 - p) Lift-off with Acetone
 - q) Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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9. Back Metallization

- Use the proper plate and boat
- Put two silver shots in each boat
- For best result the pressure should be below 5×10^{-7} torr
- Evaporate Al/Ti 600 Å/pd 400Å/Silver 600 Å on the back surface

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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10. Silver Plating

- Be very careful plating solution is toxic
- Do not use acids near the plating bath
- Measure the area of the wafer that is going to be plated (Front + Back)
 $A_{\text{total}} = A_{\text{front}} + A_{\text{back}}$
- calculate plating current:
Plating current (mA) = $2.5 \times A_{\text{total}}$
- Turn on the agitator
- Connect the positive of power supply to the Anode
- Connect the negative of the power supply to the plating clip
- Connect the plating clip to the sample
- Submerge the sample in the plating solution
- Turn on the power supply
- Set the current to the calculated current
- Plat for 20 minutes
- Turn off the power supply and the agitator
- Rinse your sample with DI water
- Blow dry your sample
- The thickness of the plated silver should be 4-6 μm

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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11. Anneal

Insert at 400° C

Annealing at 400° C for 30 min. in Forming Gas

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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12. Mesa Etch

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C, 10 min.
 - c) HMDS coat; Primer (Shipley) , back side
spin 3000 rpm, 60 sec.
 - d) Photoresist coat: 1 layer, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; front side , same as (c)
 - g) Photoresist coat 3 layers , 1400-31 (Shipley)
spin 2000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with mesa mask; 60 sec.
 - j) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) Silicon Etch; 44:26:29 HF:HNO₃:CH₃COOH
at 5° C; etch time: 5-10 sec.; etch rate: .5 μ m/sec.
(use ice/water bath to cool down to 5°C)
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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13. Test

Run ID:

Temperature:

Date:

[illegible]

Comments:.....

14. AR Coating

- Make sure that the proper boat is chosen
- Check the connections of boats to electrodes
- Check the thickness monitor crystal lifetime
- Choose the proper material density on thickness monitor
- Following information may be useful

Material	Melting point (°C)	Density (g/cm ³)	Refractive index
MgF ₂	1395	3.00	1.38
ZnS	1900	4.09	2.30

- To do evaporation follow the manual
- Clean the wafers with Acetone, Methanol (or IPA), DI rinse
- Blow dry and dry in the oven (120° C) for 10 minutes.
- Evaporate:
 - ZnS: 450-550 Å
 - MgF₂: 950-1050 Å

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

Run ID:
Temperature:
Date:

[illegible]

Comments:.....

Process Sequence for Advanced Base Line Cell (ABLC)

- Step 1. Sample Identification
- Step 2. Initial Sample Cleaning
- Step 3. Oxidation and Oxide Pattern
- Step 4. Grid Phosphorus Diffusion and Deglaze
- Step 5. Field Oxide Pattern
- Step 6. Field Phosphorus Diffusion and Deglaze
- Step 7. Passivation Oxide Growth
- Step 8. Oxide Pattern and Back Al Evaporation
- Step 9. Al Treatment
- Step 10. Lift-off for Front Metallization
- Step 11. Back Metallization
- Step 12. Silver Plating
- Step 13. Sinter
- Step 14. Test
- Step 15. AR Coating
- Step 16. Test

Run ID

- Run ID:
- Engineer/Student:
- Starting Date:
- Finish Date:
- Purpose of the run:

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- Preliminary Information:
 - It is recommended to wear a pair of glasses, face mask and two pairs of gloves
 - Never mix the solvents and acids
 - Never pour water into concentrated acid
 - Only quartz, teflon, for plastic containers should be used throughout the fabrication sequence
 - Teflon beakers should be used during cleaning processes involving HF
 - Never clean "Lerloy" tweezers with sulfuric acid (explosion)
 - Make sure DI water resistivity always reads greater than 18 MΩ
 - Make sure the hood is on
 - Cover the hood work area with clean wipers before you start processing
 - Always keep tweezers in a clean beaker with DI water
 - Never pour the solvents in the sink
 - Pour the solvents in the proper container for disposal
 - Solvents include Acetone, Methanol, TCE, Chlorobenzene
 - Water should be running in the sink when you pour the solution out
 - Rotate the beakers as you pour the acid solution in the sink
 - After cleaning, wafers should not be exposed to air too long
 - Never use acids near silverplating solution
 - Always clean after yourself
 - Return your beakers to the proper place
 - Always sign in and sign out for all equipment that you use
 - If you make a mistake you should tell the process engineer

1. Sample Identification

At the beginning of all runs the samples are to be identified with a number or other identification scribed on the unpolished side.

Number of Wafers.....

Samples ID.....

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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Beaker Cleaning

1. Rinse the beaker with DI water for 5 min.
2. Rinse the beaker in 20:1 H₂O:HF for 2 min.
3. Rinse the beaker with DI water for 5 min.

If you are using the beakers for the first time clean them with 3:1 HCL:HNO₃ FOR 1 hour.

2. Initial Sample Cleaning

a) DI rinse		3 min.	
b) $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2$	4:1	5 min.	
c) DI rinse		3 min.	
d) $\text{HF}:\text{HNO}_3$	1:20	7 min.	Teflon beaker
e) DI rinse		3 min.	
f) $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$	5:2:2	15 min.	Boiling
Or($\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$)	1:1:1	15 min.	Boiling
g) DI rinse		3 min.	
h) $\text{HF}:\text{H}_2\text{O}$	1:10	2 min.	Teflon beaker
i) DI rinse		3 min.	

2.1 Wafer Clean Before Any Diffusion

a) DI rinse		3 min.	
b) $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2$	4:1	5 min.	
c) DI rinse		3 min.	
f) $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$	5:2:2	5 min.	Boiling
Or($\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$)	1:1:1	5 min.	Boiling
g) DI rinse		3 min.	
h) $\text{HF}:\text{H}_2\text{O}$	1:50	5 sec	Teflon beaker
i) DI rinse		3 min.	

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

3. Oxidation

Insert at 700° C and ramping up to 1050°C

Oxidation at 1050° C for 180 min

Ramping down to 700° C and take the wafers out

To check the lifetime Ramp down to 450° C and run FG for 30 min

3.1. Oxide Pattern for Grid Diffusion

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) , **back side**
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; **front side** , same as (c)
 - g) Photoresist coat; 1 layer , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with Gride mask; 60 sec.
 - j) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse, Blow dry
 - o) Wafer clean

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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4. Grid Phosphorus Diffusion

- Use the proper rod for phosphorus diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Move the dummy wafers to the sides of the boat
- Load your wafers with front side facing the phosphorus source
- Use a high resistivity wafer between two sources (diffusion on both sides)
- The high resistivity wafer is used to check lifetime and J_{00} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Leave the end cap loose
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert at 500° C and ramping up to 930° C

Diffusion at 930° C for 25-30 min.

Measured sheet resistance should be around 10-20 $\Omega/\square$

- Sheet resistance after phosphorus diffusion:..... $\Omega/\square$
- PCD lifetime of high resistivity phosphorus diffused sample
 - a. Effective lifetime μsec
 - b. Bulk Lifetime μsec
 - c. J_{00} A/cm^2

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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5. Oxide Pattern for Field Diffusion

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) , **back side**
spin 3000 rpm, 60 sec.
 - d) Photoresist coat: 1 layer, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; **front side** , same as (c)
 - g) Photoresist coat; 1 layer , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with Field mask; 60 sec.
 - j) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse, Blow dry
 - o) Wafer clean

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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6. Field Phosphorus Diffusion

- Use the proper rod for phosphorus diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Move the dummy wafers to the sides of the boat
- Load your wafers with front side facing the phosphorus source
- Use a high resistivity wafer between two sources (diffusion on both sides)
- The high resistivity wafer is used to check lifetime and J_{oe} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Leave the end cap loose
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

● Baseline diffusion:

Insert at 500° C and ramping up to 820-840° C

Diffusion at 820-840° C for 25-30 min.

Measured sheet resistance should be around 150-400 $\Omega/\square$

- Sheet resistance after phosphorus diffusion:..... $\Omega/\square$
- PCD lifetime of high resistivity phosphorus diffused sample
 - a. Effective lifetime μsec
 - b. Bulk Lifetime μsec
 - c. J_{oe} A/cm^2

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

7.Passivation Oxide Growth

- Insert at 700° C and ramping up to 1050°C
- Oxidation at 1050° C for 90 min
- Ramping down to 700° C and take the wafers out
- To check the lifetime Ramp down to 450° C and run FG for 30 min

7.1. Oxide Pattern for Back Al Point Contact Lift Off

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) , **front side**
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; **back side** , same as (c)
 - g) Photoresist coat; 1 layer , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with point contact mask; 60 sec.
10 min Chlorobenzene soak
10 min bake at 95 C, 30 min.
 - j) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Blow dry
 - o) Wafer clean

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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8. Aluminum Evaporation on the Back Side

- Use aluminum designated plate for Al evaporation
- Use the proper boat for Al evaporation
- Cut Al wires using a clean cutter seven inches in length
- Put the Al designated plate in the evaporator and evaporate Al on it, then open the bell jar and turn the plate so that the Al deposited side (clean side) facing up
- Put the wafers on the top of the clean side of the plate
- Follow the Bio-rad evaporator manual
- For best result the pressure should be below 5×10^{-7} torr
- Evaporate 0.5-1.0 μm aluminum
- Lift the Al in acetone (Q-tip and ultrasonic maybe helpful to speed the lift-off process) , methanol (or IPA), DI rinse

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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9. Aluminum Treatment

- Use the proper rod for aluminum diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Use a high resistivity wafer to check the lifetime of aluminum furnace
- Use a high resistivity wafer with aluminum evaporated on both sides
- The high resistivity wafer is used to check lifetime and J_{oe} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert in N₂ at 800° C

Al treatment at 800° C, 30 min. N₂

Ramping down to 400° C in N₂

Annealing in Forming Gas for 60 min. at 400° C

- PCD lifetime of high resistivity aluminum diffused sample

- a. Effective lifetime μ sec
- b. Bulk Lifetime μ sec
- c. J_{oe} A/cm²

- Evaporate Al on the backside

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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10. Lift-off for Front Metallization

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) ;spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer, "1400-31 Shipley"
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C , 30 min.
 - f) UV Expose; 50 sec.
 - g) Chlorobenzene (Fisher Scientific) ; 10 min., Nitrogen blow dry
 - h) Soft Bake; 95° C , 10 min.
 - i) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - j) DI rinse, Blow dry
 - k) Soft Bake; 95° C , 10 min.
 - l) BOE Etch; 60-90 sec.
 - m) DI rinse, Blow dry
 - n) Soft Bake; 95° C , 10 min.
 - o) Evaporate titanium and silver:
 - Use the proper plate and boat
 - Put two silver shots in each boat
 - For best result the pressure should be below 5×10^{-7} torr
 - Evaporate Ti 600 Å/pd 400 Å/Silver 600 Å on the back surface
 - p) Lift-off with Acetone (Q-tip and ultrosonic may be helpful to speed the lift-off process)
 - q) Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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11. Back Metallization

- Use the proper plate and boat
- Put two silver shots in each boat
- For best result the pressure should be below 5×10^{-7} torr
- Evaporate Ti 600 Å/pd 400 Å/Silver 600 Å on the back surface

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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12. Silver Plating

- Be very careful; plating solution is toxic
- Do not use acids near the plating bath
- Measure the area of the wafer that is going to be plated (Front + Back)
 $A_{total} = A_{front} + A_{back}$
- Calculate plating current:
Plating current (mA) = $2.5 \times A_{total}$
- Turn on the agitator
- Connect the positive of power supply to the Anode
- Connect the negative of the power supply to the plating clip
- Connect the plating clip to the sample
- Submerge the sample in the plating solution
- Turn on the power supply
- Set the current to the calculated current, the voltage should be around 0.5 volt
- Wait for 25 minutes
- Turn off the power supply and the agitator
- Rinse your sample with DI water
- Blow dry your sample
- Check the thickness with profiler if need more plating repeat the process

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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13. Sinter

Insert at 400° C

Annealing at 400° C for 30 min. in Forming Gas (N₂:H₂ 90:10)

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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Run ID:
Temperature:
Date:

[illegible]

A-33

15. AR Coating

- Make sure that the proper boat is chosen
- Check the connections of boats to electrodes
- Check the thickness monitor crystal lifetime
- Choose the proper material density on thickness monitor
- Following information may be useful

Material	Melting point (°C)	Density (gr/cm ³)	Refractive index
MgF ₂	1395	3.00	1.38
ZnS	1900	4.09	2.30

- To do evaporation follow the manual
- Clean the wafers with Acetone, Methanol (or IPA), DI rinse
- Evaporate:
 - ZnS: 450-550 Å
 - MgF₂: 950-1050 Å

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

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16. Test

Run ID:
Temperature:
Date:

[illegible]

Comments:.....

Process Sequence for Texture Base Line Cell (TBLC)

- Step 1. Sample Identification
- Step 2. Initial Sample Cleaning
- Step 3. Oxidation and Oxide Pattern
- Step 4. Texture
- Step 5. Oxidation and Oxide Pattern for Grid Diffusion
- Step 6. Grid Phosphorus Diffusion and Deglaze
- Step 7. Field Oxide Pattern
- Step 8. Field Phosphorus Diffusion and Deglaze
- Step 9. Passivation Oxide Growth
- Step 10. Oxide Pattern and Back Al treatment
- Step 11. Life-off for Front Metallization
- Step 12. Back Metallization
- Step 13. Silver Plating
- Step 14. Sinter
- Step 15. Test

Run ID

- Run ID:
- Engineer/Student:
- Starting Date:
- Finish Date:

- Purpose of the run:

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- Preliminary Information:

It is recommended to wear a pair of glasses, face mask and two pairs of gloves
Never mix the solvents and acids
Never pour water into concentrated acid
Only quartz, teflon, or plastic beakers should be used throughout the fabrication sequence
Teflon beakers should be used during cleaning processes involving HF
Never clean "Lerloy" tweezers with sulfuric acid (explosion)
Make sure DI water resistivity always reads greater than 18 MΩ
Make sure the hood is on
Cover the hood work area with clean wipers before you start processing
Always keep tweezers in a clean beaker with DI water
Never pour the solvents in the sink
Pour the solvents in the proper container for disposal
Solvents includes Acetone, Methanol, TCE, Chlorobenzene,...
Water should be running in the sink when you pour the solution out
Rotate the beakers as you pour the acid solution in the sink
After cleaning wafers should not be exposed in the air too long
Never use acids near silverplating solution
Always clean after yourself
Return your beakers to the proper place
Always sign-in and sign-out for every equipment that you use
If you make a mistake you should tell the process engineer

1. Sample Identification

At the beginning of all runs the samples are to be identified with a number or other identification scribed on the unpolished side.

- Number of Wafers.....
- Samples ID.....

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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Beaker Cleaning

1. Rinse the beaker with DI water for 5 min.
2. Rinse the beaker in 20:1 H₂O:HF for 2 min.
3. Rinse the beaker with DI water for 5 min.

If your are using the beakers for the first time clean them with 3:1 HCL:HNO₃ FOR 1 hour.

2. Initial Sample Cleaning

a) DI rinse		3 min.	
b) $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2$	4:1	5 min.	
c) DI rinse		3 min.	
d) $\text{HF}:\text{HNO}_3$	1:20	7 min.	Teflon beaker
e) DI rinse		3 min.	
f) $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$	5:2:2	15 min.	Boiling
or ($\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$)	1:1:1	15 min.	Boiling
g) DI rinse		3 min.	
h) $\text{HF}:\text{H}_2\text{O}$	1:10	2 min.	Teflon beaker
i) DI rinse		3 min.	

2.1 Wafer Clean Before any diffusion

a) DI rinse		3 min.	
b) $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2$	4:1	5 min.	
c) DI rinse		3 min.	
f) $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$	5:2:2	5 min.	Boiling
or ($\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$)	1:1:1	5 min.	Boiling
g) DI rinse		3 min.	
h) $\text{HF}:\text{H}_2\text{O}$	1:50	5 sec	Teflon beaker
i) DI rinse		3 min.	

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....

3.Oxidation and Oxide Pattern

- PECVD oxide or the following can be used
- Insert at 700 C and ramping up to 1000
- Oxidation at 1000 C for 120 min
- Ramping down to 700 C and take the wafers out
- To check the lifetime Ramp down to 450 C and run FG for 30 min
- Turn off the white lights
- Turn on the vacuum of spinner

- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat ;Primer(Shipley) , back side
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; back side, 1 layers, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; front side , same as c
 - g) Photoresist coat; front side, 1 layers , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with Gride mask; 15 sec.
 - j) Develop; "Developer 351 Shipley"
Developer:H₂O (2:7) for 20-40 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 3 min to remove the oxide
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse,

4. Texture

- DI rinse 3 min
- H₂O:KOH:IPA 1100:18:80 25-40 min at 70°C
- DI rinse 3 min

- NOTE texturing solution usually WORKS (depening upon good temp control and proper laminar flow in the hood)in the following range:
H₂O:KOH:IPA 1100:17-20:70-85 25-40 min at 70°C-80 C

5. Oxidation and Oxide Pattern for Grid Diffusion

- Insert at 700°C and ramping up to 1050°C
- Oxidation at 1050°C for 180 min
- Ramping down to 700°C and take the wafers out
- To check the lifetime Ramp down to 450°C and run FG for 30 min

4.1. Oxide pattern for Grid diffusion

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat ;Primer(Shipley) , back side
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; back side, 1 layers, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; front side , same as c
 - g) Photoresist coat; front side, 1 layers , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with Gride mask; 40 sec.
 - j) Develop; "Developer 351 Shipley"
Developer:H₂O (2:7) for 20-40 sec.(25 sec)
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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6. Grid Phosphorus Diffusion

- Use the proper rod for phosphorus diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- move the dummy wafers to the sides of the boat
- Load your wafers with front side facing the phosphorus source
- Use a high resistivity wafer between two sources (diffusion on both sides)
- The high resistivity wafer is used to check lifetime and J_{oe} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Leave the end cap loose
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert at 500° C and ramping up to 930° C

Diffusion at 930° C for 25-30 min.

Measured sheet resistance should be around 10-20 $\Omega/\square$

- Sheet resistance after phosphorus diffusion:..... $\Omega/\square$
- PCD lifetime of high resistivity phosphorus diffused sample
 - a. Effective lifetime μsec
 - b. Bulk Lifetime μsec
 - c. J_{oe} A/cm^2

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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7. Oxide Pattern for Field Diffusion

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat ;Primer(Shipley) , back side
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; back side, 1 layers, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; front side , same as c
 - g) Photoresist coat; front side, 1 layers , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with Field mask; 60 sec.
 - j) Develop; "Developer 351 Shipley"
Developer:H₂O (2:7) for 30-60 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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8. Field Phosphorus Diffusion

- Use the proper rod for phosphorus diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- move the dummy wafers to the sides of the boat
- Load your wafers with front side facing the phosphorus source
- Use a high resistivity wafer between two sources (diffusion on both sides)
- The high resistivity wafer is used to check lifetime and J_{00} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Leave the end cap loose
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert at 500° C and ramping up to 820-840° C

Diffusion at 820-840° C for 25-30 min.

Measured sheet resistance should be around 150-400 $\Omega/\square$

- Sheet resistance after phosphorus diffusion:..... $\Omega/\square$
- PCD lifetime of high resistivity phosphorus diffused sample

- a. Effective lifetime μsec
- b. Bulk Lifetime μsec
- c. J_{00} A/cm^2

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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9. Passivation Oxide growth

- Insert at 700°C and ramping up to 1050°C
- Oxidation at 1050°C for 90 min
- Ramping down to 700°C and take the wafers out
- To check the lifetime Ramp down to 450°C and run FG for 30 min

9.1. Oxide pattern for back Al point contact lift off

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat ;Primer(Shipley) , front side
spin 3000 rpm, 60 sec.
 - d) Photoresist coat;1 layers, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; back side , same as c
 - g) Photoresist coat; 1 layers , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with point contact mask; 60 sec.
10 min Chlorobenzene soak
10 min bake at 95 C, 30 min.
 - j) Develop; "Developer 351 Shipley"
Developer:H₂O (2:7) for 30-60 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse and Blow dry

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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10. Backside Aluminum Evaporation and Al Diffusion

- Use aluminum designated plate for Al evaporation
- Use the proper boat for Al evaporation
- Cut Al wires using a clean cutter in seven inch length
- Put the Al designated plate in the evaporator and evaporate Al on it, then open the bell jar and turn the plate so that the Al deposited side (clean side) facing up
- Put the wafers on the top of the clean side of the plate
- Follow the Bio-rad evaporator manual
- For best result the pressure should be below 5×10^{-7} torr
- Evaporate 0.5-1.0 μm aluminum
- Lift the Al in acetone (ultrasonic and Q-tip maybe helpfull to speed the process), methanol (or IPA), Di rinse
- Use the proper rod for aluminum diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Use a high resistivity wafer to check the lifetime of aluminum furnace
- Use a high resistivity wafer with aluminum evaporated on both sides
- The high resistivity wafer is used to check lifetime and J_{00} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert in N₂ at 800°
Al treatment at 800° C, 30 min. N₂
Ramping down to 400° C in N₂
Annealing in Forming Gas for 60 min. at 400° C

- PCD lifetime of high resistivity aluminum diffused sample
 - a. Effective lifetime μsec
 - b. Bulk Lifetime μsec
 - c. J_{00} A/cm²

- Evaporate Al all over the back side

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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11. Lift-off for Front Metallization

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat ;Primer(Shipley) ;spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layers,"1400-31 Shipley"
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C , 30 min.
 - f) UV Expose; 50 sec.
 - g) Chlorobenzene (Fisher Scientific) ; 10 min., Nitrogen blow dry
 - h) Soft Bake; 95° C , 10 min.
 - i) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - j) DI rinse, Blow dry
 - k) Soft Bake; 95° C , 10 min.
 - l) BOE Etch; 60-90 sec.
 - m) DI rinse, Blow dry
 - n) Soft Bake; 95° C , 10 min.
 - o) Evaporate titanium and silver:
 - Use the proper plate and boat
 - Put two silver shots in each boat
 - For best result the pressure should be below 5×10^{-7} torr
 - Evaporate Ti 600 Å/pd 400 Å/Silver 600 Å on the back surface
 - p) Lift-off with Acetone (ultrasonic and Q-tip maybe helpfull to speed the process)
 - q) Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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12. Back Metallization

- Use the proper plate and boat
- Put two silver shots in each boat
- For best result the pressure should be below 5×10^{-7} torr
- Evaporate Ti 600 Å/Silver 600 Å on the back surface

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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13. Silver Plating

- Be very careful plating solution is toxic
- Do not use acids near the plating bath
- Measure the area of the wafer that is going to be plated (Front + Back)
 $A_{\text{total}} = A_{\text{front}} + A_{\text{back}}$
- calculate plating current:
Plating current (mA) = $2.5 \times A_{\text{total}}$
- Turn on the agitator
- Connect the positive of power supply to the Anode
- Connect the negative of the power supply to the plating clip
- Connect the plating clip to the sample
- Submerge the sample in the plating solution
- Turn on the power supply
- Set the current to the calculated current
- Wait for 25 minutes
- Turn off the power supply and the agitator
- Rinse your sample with DI water
- Blow dry your sample
- Check the thickness with profiler if need more plating repeat the process

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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14. Sinter

Insert at 400° C

Annealing at 400° C for 30 min. in Forming Gas

If any samples were broken during this step, give the sample ID's of the broken wafer here:

Comments:.....
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Run ID:
Temperature:
Date:

[illegible]

Comments:.....

Process Sequence for Inverted Pyramid Base Line Cell (IBLC)

- Step 1. Sample Identification
- Step 2. Initial Sample Cleaning
- Step 3. Oxidation and Oxide Pattern
- Step 4. Inverted Pyramid Etch
- Step 5. Oxidation and Oxide Pattern
- Step 6. Grid Phosphorus Diffusion and Deglaze
- Step 7. Field Oxide Pattern
- Step 8. Field Phosphorus Diffusion and Deglaze
- Step 9. Passivation Oxide Growth
- Step 10. Oxide Pattern and Back Al treatment
- Step 11. Lift-off for Front Metallization
- Step 12. Back Metallization
- Step 13. Silver Plating
- Step 14. Sinter
- Step 15. Test

Run ID

- Run ID:
- Engineer/Student:
- Starting Date:
- Finish Date:

- Purpose of the run:

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- Preliminary Information:

It is recommended to wear a pair of glasses, face mask and two pairs of gloves
Never mix the solvents and acids
Never pour water into concentrated acid
Only quartz, teflon, or plastic beakers should be used throughout the fabrication sequence
Teflon beakers should be used during cleaning processes involving HF
Never clean "Lerloy" tweezers with sulfuric acid (explosion)
Make sure DI water resistivity always reads greater than 18 M Ω
Make sure the hood is on
Cover the hood work area with clean wipers before you start processing
Always keep tweezers in a clean beaker with DI water
Never pour the solvents in the sink
Pour the solvents in the proper container for disposal
Solvents includes Acetone, Methanol, TCE, Chlorobenzene
Water should be running in the sink when you pour the solution out
Rotate the beakers as you pour the acid solution in the sink
After cleaning, wafers should not be exposed to air too long
Never use acids near silverplating solution
Always clean after yourself
Return your beakers to the proper place
Always sign in and sign out for all equipment that you use
If you make a mistake you should tell the process engineer

1. Sample Identification

At the beginning of all runs the samples are to be identified with a number or other identification scribed on the unpolished side.

● Number of Wafers.....

● Samples ID.....

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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Beaker Cleaning

1. Rinse the beaker with DI water for 5 min.
2. Rinse the beaker in 20:1 H₂O:HF for 2 min.
3. Rinse the beaker with DI water for 5 min.

If your are using the beakers for the first time clean them with 3:1 HCL:HNO₃ FOR 1 hour.

2. Initial Sample Cleaning

a) DI rinse		3 min.	
b) $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2$	4:1	5 min.	
c) DI rinse		3 min.	
d) $\text{HF}:\text{HNO}_3$	1:20	7 min.	Teflon beaker
e) DI rinse		3 min.	
f) $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$	5:2:2	15 min.	Boiling
or ($\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$)	1:1:1	15 min.	Boiling
g) DI rinse		3 min.	
h) $\text{HF}:\text{H}_2\text{O}$	1:10	2 min.	Teflon beaker
i) DI rinse		3 min.	

2.1 Wafer Clean Before Any Diffusion

a) DI rinse		3 min.	
b) $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2$	4:1	5 min.	
c) DI rinse		3 min.	
f) $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$	5:2:2	5 min.	Boiling
or ($\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$)	1:1:1	5 min.	Boiling
g) DI rinse		3 min.	
h) $\text{HF}:\text{H}_2\text{O}$	1:50	5 sec	Teflon beaker
i) DI rinse		3 min.	

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

3. Oxidation and Oxide Pattern

- PECVD oxide or the following can be used
- Insert at 700° C and ramping up to 1000°
- Oxidation at 1000° C for 120 min
- Ramping down to 700° C and take the wafers out
- To check the lifetime Ramp down to 450° C and run FG for 30 min
- Turn off the white lights
- Turn on the vacuum of spinner

- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) , back side (you can skip this if you want the backside to be etched)
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; front side , same as (c)
 - g) Photoresist coat: 1 layer , 1400-31 (Shipley)
spin 6000 rpm, 30 sec,(or spin 4000 rpm)
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with Gride mask; 2 sec, (or 8 sec for 4000rpm)
 - j) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec, check under microscope.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse, Blow dry

4. Inverted Pyramid Etch

- DI rinse 3 min
- DI:KOH 1100:240 10-20 min at 70 C
- DI rinse 3 min
- HNO₃:HF 40:1 2 MIN
- DI rinse 3 min
- HF:H₂O 1:10 3 min
- DI rinse 3 min

5.Oxidation and Oxide Pattern for Grid Diffusion

- Insert at 700° C and ramping up to 1050°
- Oxidation at 1050° C for 180 min
- Ramping down to 700° C and take the wafers out
- To check the lifetime Ramp down to 450° C and run FG for 30 min
- Turn off the white lights
- Turn on the vacuum of spinner

- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) , back side
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; front side , same as (c)
 - g) Photoresist coat; 1 layer , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with Gride mask; 40 sec.
 - j) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec. (35 sec)
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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6. Grid Phosphorus Diffusion

- Use the proper rod for phosphorus diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Move the dummy wafers to the sides of the boat
- Load your wafers with front side facing the phosphorus source
- Use a high resistivity wafer between two sources (diffusion on both sides)
- The high resistivity wafer is used to check lifetime and J_{00} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Leave the end cap loose
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert at 500° C and ramping up to 930° C

Diffusion at 930° C for 25-30 min.

Measured sheet resistance should be around 10-20 $\Omega/\square$

- Sheet resistance after phosphorus diffusion:..... $\Omega/\square$
- PCD lifetime of high resistivity phosphorus diffused sample
 - a. Effective lifetime μsec
 - b. Bulk Lifetime μsec
 - c. J_{00} A/cm^2

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....

7. Oxide pattern for Field diffusion

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) , back side
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; front side , same as (c)
 - g) Photoresist coat; 1 layer , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with Field mask; 60 sec.
 - j) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Acetone, Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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8. Field Phosphorus Diffusion

- Use the proper rod for phosphorus diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Move the dummy wafers to the sides of the boat
- Load your wafers with front side facing the phosphorus source
- Use a high resistivity wafer between two sources (diffusion on both sides)
- The high resistivity wafer is used to check lifetime and J_{oe} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Leave the end cap loose
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert at 500° C and ramping up to 820-840° C

Diffusion at 820-840° C for 25-30 min.

Measured sheet resistance should be around 150-400 $\Omega/\square$

- Sheet resistance after phosphorus diffusion:..... $\Omega/\square$
- PCD lifetime of high resistivity phosphorus diffused sample
 - a. Effective lifetime μsec
 - b. Bulk Lifetime μsec
 - c. J_{oe} A/cm^2

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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9. Passivation Oxide Growth

- Insert at 700° C and ramping up to 1050°C
- Oxidation at 1050° C for 90 min
- Ramping down to 700° C and take the wafers out
- To check the lifetime Ramp down to 450° C and run FG for 30 min

9.1. Oxide Pattern for Back Al Point Contact Lift Off

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) , front side
spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer, 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C, 10 min.
 - f) HMDS coat; front side , same as (c)
 - g) Photoresist coat; 1 layer , 1400-31 (Shipley)
spin 3000 rpm, 30 sec.
 - h) Soft Bake; 95° C, 30 min.
 - i) UV expose with point contact mask; 60 sec.
10 min Chlorobenzene soak
10 min bake at 95 C, 30 min.
 - j) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - k) DI rinse, Blow dry
 - l) Hard Bake; 120° C, 15 min.
 - m) BOE for 5 min to remove the oxide
 - n) DI rinse, Blow dry

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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10. Oxide Pattern and Back Al Treatment

- Use aluminum designated plate for Al evaporation
- Use the proper boat for Al evaporation
- Cut Al wires using a clean cutter seven inches in length
- Put the Al designated plate in the evaporator and evaporate Al on it, then open the bell jar and turn the plate so that the Al deposited side (clean side) facing up
- Put the wafers on the top of the clean side of the plate
- Follow the Bio-rad evaporator manual
- For best result the pressure should be below 5×10^{-7} torr
- Evaporate 0.5-1.0 μm aluminum
- Lift the Al in acetone (Q-tip and ultrosonic mabe helpfull to speed up the lift-off process), methanol (or IPA), Di rinse
- Use the proper rod for aluminum diffusion furnace
- Use the elephant to transfer the boat to the loading station
- Wait 10 minutes to cool down
- Use a high resistivity wafer to check the lifetime of aluminum furnace
- Use a high resistivity wafer with aluminum evaporated on both sides
- The high resistivity wafer is used to check lifetime and J_{ob} of your diffusion
- Use the elephant to transfer the boat to the furnace
- Push the boat in with the proper rod at a very slow rate
- Use the proper program (refer to the manual)

- Baseline diffusion:

Insert in N₂ at 800° C

Al treatment at 800° C, 30 min. N₂

Ramping down to 400° C in N₂

Annealing in Forming Gas for 60 min. at 400° C

- PCD lifetime of high resistivity aluminum diffused sample

- a. Effective lifetime μsec
- b. Bulk Lifetime μsec
- c. J_{oe} A/cm²

- Evaporate 0.5-1.0 μm aluminum on the back side

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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11. Lift-off for Front Metallization

- Turn off the white lights
- Turn on the vacuum of spinner
- Process baseline:
 - a) Clean; Acetone, Methanol (or IPA), DI rinse, Blow dry
 - b) Prebake; 120° C , 10 min.
 - c) HMDS coat; Primer (Shipley) ;spin 3000 rpm, 60 sec.
 - d) Photoresist coat; 1 layer, "1400-31 Shipley"
spin 3000 rpm, 30 sec.
 - e) Soft Bake; 95° C , 30 min.
 - f) UV Expose; 50 sec.
 - g) Chlorobenzene (Fisher Scientific) ; 10 min., Nitrogen blow dry
 - h) Soft Bake; 95° C , 10 min.
 - i) Develop; "Developer 351 Shipley"
Developer: H₂O (2:7) for 30-60 sec.
 - j) DI rinse, Blow dry
 - k) Soft Bake; 95° C , 10 min.
 - l) BOE Etch; 60-90 sec.
 - m) DI rinse, Blow dry
 - n) Soft Bake; 95° C , 2 min.
 - o) Evaporate titanium and silver:
 - Use the proper plate and boat
 - Put two silver shots in each boat
 - For best result the pressure should be below 5×10^{-7} torr
 - Evaporate Ti 600 Å/pd 400 Å /Silver 600 Å on the back surface
 - p) Lift-off with Acetone (Q-tip and ultrasonic maybe helpful to speed up the lift-off process)
 - q) Methanol (or IPA), DI rinse, Blow dry

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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12. Back Metallization

- Use the proper plate and boat
- Put two silver shots in each boat
- For best result the pressure should be below 5×10^{-7} torr
- Evaporate Ti 600 Å/pd 400 Å /Silver 600 Å on the back surface

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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13. Silver Plating

- Be very careful; plating solution is toxic
- Do not use acids near the plating bath
- Measure the area of the wafer that is going to be plated (Front + Back)
 $A_{\text{total}} = A_{\text{front}} + A_{\text{back}}$
- Calculate plating current:
Plating current (mA) = $2.5 \times A_{\text{total}}$
- Turn on the agitator
- Connect the positive of the power supply to the Anode
- Connect the negative of the power supply to the plating clip
- Connect the plating clip to the sample
- Submerge the sample in the plating solution
- Turn on the power supply
- Set the current to the calculated current
- Plat for 25 minutes
- Turn off the power supply and the agitator
- Rinse your sample with DI water
- Blow dry your sample
- Check the thickness with profiler; if more plating is needed repeat the process

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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14. Sinter

Insert at 400° C

Annealing at 400° C for 30 min. in Forming Gas

If any samples were broken during this step, give the sample IDs of the broken wafer here:

Comments:.....
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15. Test

Run ID:

Temperature:

Date:

Cell ID	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF	N	Efficiency (%)	R_s (Ω -cm ²)	R_{sh} (K Ω - cm ²)	J_{o1} (A/cm ²)	J_{o2} (A/cm ²)	OCD Lifetime (μ sec)
Standard Cell...										

Comments:.....
.....

APPENDIX B

Georgia Tech

*University Center of Excellence
for
Photovoltaics Research and Education*

Dr. Ajeet Rohatgi

Director, University Center of Excellence for
Photovoltaics Research and Education
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA 30332-0250 USA
TEL: 404•894•7692 / FAX: 404•853•9171

**UCEP:
Helping To Create A New Energy Source for the
21st Century**

Dominant conventional energy sources—oil, coal, natural gas, and nuclear power—are accompanied by problems of air and water pollution, resource depletion, and the greenhouse effect, all of which are becoming increasingly unacceptable and unaffordable. In the 21st century, photovoltaics (PV)—direct conversion of sunlight into electricity—can potentially meet the rapidly growing demand for electricity with minimal environmental consequence. The real challenge lies in reducing the cost of solar cells while raising their efficiencies. Research and education on advanced PV materials and devices will play a major role in accelerating the development of cost-effective PV.

To address these issues, the Department of Energy (DOE) has established a University Center of Excellence for Photovoltaics Research and Education (UCEP) at Georgia Tech, one of two such centers in the United States. The Center, under the direction of Dr. Ajeet Rohatgi, reports through Georgia Tech's Office of Interdisciplinary Programs. The mission of the Center is to improve the fundamental understanding of the science and technology of advanced PV devices, to fabricate record high efficiency solar cells, to provide training and enrich the educational experience of students in this field, and to give the U.S. a competitive edge by providing guidelines to industry and DOE for achieving cost-effective and high-efficiency PV devices.

Major Focus Areas

The Center reports to Sandia National Laboratories in Albuquerque, New Mexico, a DOE facility. Funding by Sandia encourages and provides the opportunity to conduct basic and applied PV research in collaboration with other universities, government agencies, PV industries, and experts from other nationally and internationally known PV organizations. Listed below are some major focus areas for UCEP.

- Establish an Educational Support Program (ESP) Laboratory to fabricate efficient silicon solar cells and to assist other university PV programs in the U.S. Any university that meets the ESP prerequisites is eligible to participate in this program. ESP prerequisites for a university participant is that the

university offer a course on solar cells or on semiconductor device fabrication.

- Develop a solar cell technology curriculum and recruit faculty and students into the PV field
- Improve fundamental understanding of the loss mechanisms and the role of defects in promising photovoltaic materials
- Perform solar cell modeling to develop novel high efficiency cell designs and fabricate record high efficiency solar cells
- Establish guidelines for industry and government to help PV become a cost-effective, viable, and environmentally clean source of electrical energy
- Assist and interface with other university and industry PV programs in the U.S.

Facilities

UCEP facilities are housed in Tech's School of Electrical Engineering and Microelectronics Research Center. These facilities range from materials growth, materials characterization, solar cell modeling, process development, solar cell fabrication, and solar cell testing. The Center has facilities in the following areas:

- Material characterization, including techniques such as DLTS, SPV, FTIR, C-V, I-V, SR, HALL, PL, PCD, OCVD, EBIC, SEM, AES, ESCA, SIMS, and doping profiler
- Complete silicon solar cell fabrication, including approximately 1,000 square feet of clean room space, oxidation, diffusion, metallization, plating, AR coating, sputtering, PECVD, RTP, and lithography
- Electrical and optical testing and analyses of PV devices, including light and dark I-V, cell efficiency, carrier transport, reflection, and quantum efficiency measurements
- Computer modeling and design of high efficiency solar cells

Accomplishments in Photovoltaics

Before being named a center of excellence by the DOE, Georgia Tech faculty and students already had a strong track record in PV materials research and in design and fabrication of high efficiency solar cells. In addition to significant government and industry collaboration, Georgia Tech's PV program currently has nine Ph.D. students, seven research engineers, and in excess of 100 publications and presentations. Other notable PV accomplishments include:

- Development of a new and improved DLTS system, specifically designed for transient analysis and for analyzing defects in PV materials
- Fabrication of 17.7 percent efficient polycrystalline silicon solar cells
- Fabrication of ~21 percent efficient single crystal silicon cells
- Development of a user friendly and sophisticated ray tracing program for the PV community to model and improve optical confinement in cells
- Development of an improved PCD lifetime tester along with a methodology to separate and quantify various lifetime limiting mechanisms in silicon
- Development of novel designs for Si and GaAs solar cells with efficiencies exceeding 25 percent
- Achievement of a record high carrier lifetime (6 mS) in oxidized MCZ silicon
- Development of a novel and improved PECVD grown double layer anti-reflection coating for Si cells
- Development of a low-temperature PECVD grown high quality oxide on silicon with record low interface state density

This brochure was funded by the
U.S. Department of Energy/Sandia National Laboratories,
Georgia Power Company, and the Georgia Institute of Technology

APPENDIX C

EE 6456

SOLAR CELLS

Fall 1992

INSTRUCTOR: Ajeet Rohatgi
Office 121
Phone 894-7692

OFFICE HOURS: Tu, Th 2:00 - 3:30

COURSE OBJECTIVES: To introduce various aspects of solar cells including opto-electronic properties of photovoltaic materials, basic operating principles of solar cell device, modelling and design factors for high efficiency solar cells, fabrication of solar cells, and design of photovoltaic systems.

TEXT: Solar Cells: Operating Principle, Technology, and Systems Application, M.A. Green, Prentice Hall, Inc., NJ (1982).

LECTURE OUTLINE

<u>Topics</u>	<u>Description</u>	<u>Estimated Number of Lectures</u>
Chap. 1	Introduction - General Description of Course	1
Chap. 2	Review of Semiconductor Properties	2
Chap. 3	Generation and Recombination	3
Chap. 4	p-n Junction Diodes	2
Chap. 5	Efficiency Limits, Losses, and Measurement	2
Chap. 6	Standard Silicon Solar Cell Technology	1
Chap. 7	Improved Silicon Cell Technology	2

Chap. 8	Design of Silicon Solar Cells	3
Chap. 9	Other Device Structure	2
Chap. 10	Other Semiconductor Materials	1
Chap. 11	Concentrator Cells	1
Chap. 12 and 14	PV Systems	1

GRADES & EXAMS

Final grades will be given on the basis of:

1.	Hourly Exam #1	30%	October
2.	Term Paper or
Hourly Exam #2	30%	November
3.	Final Exam	40%	
4.	Homework		

ATTENDANCE

You are responsible for all topics, assignments, and announcements given during regular call meetings.

SMOKING, EATING AND DRINKING

Prohibited in the classroom by Institute rules.

Alpha Solarco
Attn: Anco Blazev
6507 South Hardy Drive
Tempe, AZ 85283

American Optical Corporation
Attn: Clark Grendol
14 Mechanic Street
Southbridge, MA 01550

Amonix, Inc. (2)
Attn: Sewang Yoon, Vahan Garboushian
3425 Fujita Street
Torrance, CA 90505

Applied Solar Energy Corp. (2)
Attn: Frank Ho and Henry Yoo
15251 East Don Julian Road
City of Industry, CA 91746

Arizona Public Service Company
Attn: Thomas Lepley
Mail Stop 9110
Post Office Box 53999
Phoenix, AZ 85072-3999

Arizona Public Service Company
Star Facility
Attn: Peter Eckert
1500 East University
Tempe, AZ 85281

Arizona State University (3)
College of Engineering
Attn: Robert Hammond, Charles Backus,
and Dieter Schroder
Tempe, AZ 85287-5806

Ascension Technology, Inc.
Attn: Miles Russell
P. O. Box 314
Lincoln Center, MA 01773

AstroPower
Attn: Allen Barnett
Solar Park
Newark, DE 19716-2000

Bechtel National, Inc.
Attn: Walter J. Stolte
P. O. Box 3965
Mail Stop 50/15/D17
San Francisco, CA 94119-3965

Black and Veatch
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P. O. Box 8405
Kansas City, MO 64114

Blue Mountain Energy
Attn: Kay Firor
59943 Comstock Road
Cove, OR 97824

Boeing Aerospace
Attn: Dr. John W. Yerkes
High Technology Center
P. O. Box 3999, MS 7J-71
Seattle, WA 98124-2499

California Energy Commission
Attn: Alexander Jenkins
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Sacramento, CA 95814

Mr. Clement Chiang
GE Aerospace, MS NP-2K
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West Windsor, NJ 08543-800

City of Austin Electric Department
Attn: John E. Hoffner
P. O. Box 1088
Austin, TX 78767

Cleveland State University
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Dept. of Electrical Engineering
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Crystal Systems
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Cummings Engineering
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7329 Meadow Court
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Jet Propulsion Lab (2)
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Massachusetts Institute of Technology
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77 Massachusetts Avenue
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Midway Laboratories
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77 West Wacker
Chicago, IL 60601

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Four Suburban Park Drive
Billerica, MA 01821

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Bhushan Sopori, Ted Ciszek, John Benner
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Pacific Gas and Electric (4)
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Wenger, Tammie Candelaria
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San Ramon, CA 94583

Photonic Power Systems, Inc.
Attn: Jan Werthan
550 California Avenue
Palo Alto, CA 94306

Public Service Company of New Mexico
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Alvarado Square, MS 0150
Albuquerque, NM 87158

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Mr. Ronald Sinton
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San Jose, CA 95129

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Dallas, TX 75354-0636

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Narayanan
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Morrison, CO 80465

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Bedford, MA 01730

SunPower Corp.
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Suntracker
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3M Center
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University of New South Wales
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School of Electrical Engineering
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Joint Research Centre, ESTI
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Fraunhofer Institute for Solar Energie
Systeme
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Instituto de Energia Solar
Ciudad Universitaria, s/n
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ETSI Telecomunicacion (UPM)
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