1 of 1

DEC 13 1993
OSTI

Los Alamos National Laboratory is operated by the University of California for the United States Department of Energy under contract W-7405-ENG-36.

TITLE: THE DESIGN AND CONSTRUCTION OF A DOUBLE-SIDED SILICON
MICROVERTEX DETECTOR FOR THE L3 EXPERIMENT AT CERN

AUTHOR(S): Jon S. Kapustinsky, Thomas E. Coan, W. Wayne Kinnison,
Geoffrey B. Mills, Melynda L. Brooks, David M. Lee,
Timothy C. Thompson

SUBMITTED TO: IEEE 1993 Nuclear Science Symposium, San Francisco, CA,
November 2-6, 1993

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

By acceptance of this article, the publisher recognizes that the U.S. Government retains a nonexclusive, royalty-free license to publish or reproduce the published form of this contribution, or to allow others to do so, for U.S. Government purposes.

The Los Alamos National Laboratory requests that the publisher identify this article as work performed under the auspices of the U.S. Department of Energy

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

Los Alamos Los Alamos National Laboratory
Los Alamos, New Mexico 87545

MASTER

The Design and Construction of a Double-Sided Silicon Microvertex Detector for the L3 Experiment at CERN

A.Adam^d, S.Ahlen^c, G.Ambrosi^p, E.Babucci^p, A.Baschirottoⁿ, R.Battiston^{e,p}, A.Bay^j, G.Y.L.Bencze^f, B.Bertucci^p, M.Biasini^p, G.M.Bilei^p, G.J.Bobbink^o, M.Bosettiⁿ, M.L.Brooks^l, J.Busenitz^b, W.J.Burger^j, C.Camps^a, M.Caria^p, G.Castelliniⁱ, B.Checcucci^p, A.Chen^q, T.E.Coan^l, V.Commichau^a, D.DiBitonto^b, P.Duinker^o, S.Easo^p, P.Extermann^j, E.Fiandrini^p, A.Gougas^k, K.Hangartner^a, C.Hauviller^e, A.Herve^e, S.Hou^q, I.Josa^e, J.S.Kapustinsky^l, D.Kim^k, W.W.Kinnison^l, J.Kornis^f, V.R.Krastev^p, G.Landi^h, M.Lebeau[†], P.Lecomte^g, D.M.Lee^l, R.Leiste^{e,s}, E.Lejeune^m, W.T.Lin^q, W.Lohmann^s, A.Marin^c, R.Masetti^p, G.B.Mills^l, H.Nowak^s, G.Passaleva^{h,p}, T.Paul^k, M.Pauluzzi^p, S.Pensottiⁿ, E.Perrin^j, P.G.Rancoitaⁿ, M.Rattaggiⁿ, A.Santocchia^p, M.Sachwitz^s, P.Schmitz^a, B.Schoenisch^s, L.Servoli^p, G.F.Susinno^j, G.Terziⁿ, T.C.Thompson^l, F.Tonisch^s, J.Toth^f, G.Trowitzsch^s, G.M.Viertel^g, H.Vogt^s, S.Waldmeier^g, R.Weill^m, S.C.Yeh^r, B.Zhou^c

Presented by Jon S Kapustinsky, Los Alamos National Laboratory

a)III. Physikalisches Institut, RWTH, Aachen, Germany

b)The University of Alabama, Tuscaloosa, USA

c)Boston University, Boston, USA

d)Physical Institute/Technical University, Budapest, Hungary

e)CERN, Geneva, Switzerland

f)KFKI/Research Institute for Particle and Nuclear Physics, Budapest, Hungary

g)ETH Zurich, Switzerland

h)INFN/Universita di Firenze, Italy

i)INFN/IROE Firenze, Italy

j)University of Geneva, Switzerland

k)Johns Hopkins University, Baltimore, USA

l)Los Alamos National Laboratory, Los Alamos, USA

m)University of Lausanne, Switzerland

n)INFN/Universita di Milano, Italy

o)NIKHEF, Amsterdam, Netherlands

p)INFN/Universita di Perugia, Italy

q)NCU, ChungLi, Taiwan

r)National Tsing Hua University, Hsinchu, Taiwan

s)DESY -IFH, Zeuthen, Germany

Abstract

A Silicon Microvertex Detector (SMD) has been commissioned for the L3 experiment at the Large Electron-Positron colliding-beam accelerator (LEP) at the European Center for Nuclear Physics, (CERN). The SMD is a 72,672 channel, two layer barrel tracker that is comprised of 96 ac-coupled, double-sided silicon detectors. Details of the design and construction are presented.

1. INTRODUCTION

A new detector, the Silicon Microvertex Detector, has been constructed and installed into the L3 experiment at CERN prior to the 1993 running period of the LEP accelerator. The

design and construction phase of the project lasted only two years, following the upgrade approval in 1991. To meet the challenging schedule, we made use of extensive development work done on silicon strip detectors by other collider detector groups [1, 2].

The SMD is a two-layer, barrel tracker. The average radii of the layers are 6 and 8 cm. It is comprised of 96 double-sided silicon sensors from which 48 independent detectors, called half-ladders, have been built. These half-ladders are, in turn, assembled into 24 full ladders. The ladders are the unit mechanical building blocks of the SMD. The 12 inner ladders of the detector are oriented parallel to the central axis of the SMD. These ladders are shingled, creating an overlapping region that helps to align the detector with particle tracks. The 12 outer ladders are oriented with a 2° tilt relative to the inner layer to help resolve tracking ambiguities. Both sides, R-phi and Z, of the sensors are read out to give a 3-dimensional measurement of charged particle tracks. The SMD covers the

† Permanent address: LAPP, Annecy, France

polar angle from 22° to 158°, and covers the full azimuth. The total number of readout channels is 72,672.

2. SILICON SENSORS

The SMD silicon sensors are based on an INFN-Pisa design for Aleph [1] and are fabricated at the Swiss Center for Electronics and Microtechnology (CSEM)[3]. Each sensor is approximately $4 \times 7 \text{ cm}^2$ and 300 μm thick. The p-implantation strips on the junction side run the length of the sensor, and are oriented parallel to the beam direction. These strips measure the R-phi coordinate. On the ohmic side, n-type strips are implanted orthogonal to the p-strips, and these measure the Z coordinate. The strip and readout pitch on the p-side is 25 μm and 50 μm , respectively. The strip and readout pitch on the n-side is 50 μm and 150 or 200 μm , depending on polar angle. A double n+ implantation surrounds the strips on the p-side. This metallized implant is both a guard and a bias ring. The biasing mechanism on the p-side is the punch-through method [4]. The bias ring brings both the readout and the intermediate interpolation strips to the same voltage potential, thus creating a uniform electric field below all the strips. This enhances the spatial resolution that is achievable by capacitive charge division. A similar ring structure, but in p+, is implanted on the ohmic side of the sensor. The bias connection on this side is made via accumulation resistors. P-stops are implanted between each pair of n strips to provide good interstrip resistivity.

The sensors are ac-coupled to the front-end electronics through separate 128-element, 48 μm pitch capacitor chips [1], which are also produced at CSEM. The capacitors are polysilicon-polysilicon structures separated by a silicon dioxide layer, and fabricated on a quartz substrate to minimize parasitic capacitance. The capacitors are 150 pf with a typical breakdown voltage of 45V. In normal operation the voltage potential across the capacitors is, at most, a few volts, and breakdown damage is not a concern. However, to protect against abnormal voltage transients, protection diodes have been added between each capacitor and a common guard ring. In the event of a large transient voltage, which can occur, for example because of an accidental beam loss, the diodes will break down at about 8V and effectively short the transient to the guard ring before the capacitor is destroyed.

3. FRONT-END ELECTRONICS

The SVX-H is the SMD front-end readout chip. The SVX was designed by S. Kleinfelder *et al.* [5] at Lawrence Berkeley Laboratory (LBL) for the Collider Detector at Fermilab (CDF). An SVX is a 128 channel chip. A readout channel is comprised of a charge sensitive amplifier, followed by a sample and hold stage, a comparator and latch, and digital logic to control the serial multiplexed readout. The SVX can be operated in a zero suppression mode, also referred to as sparse mode readout. The power dissipation is about 175 mW per chip.

The SVX-H was fabricated at United Technologies Microelectronics Center (UTMC)[6] in a 1.2 μm , radiation-hard CMOS process. Four 5-inch wafers of SVX were produced for the SMD. Test die on each wafer were irradiated at UTMC with a collimated x-ray source to qualify the electronics to greater than 1 Mrad of ionizing radiation dose. The wafers were then probed using a test station at LBL. Each die was tested for functionality, gain, noise, threshold level, and linearity. The test results were recorded in a data base and used to select die for attachment to the hybrid circuits. The average single channel gain over the 96 hybrids that were selected for the SMD was 25.0 mV/fC with an RMS of 0.6mV/fC, or 2.4%. The equivalent noise charge was measured with zero input capacitance, and averaged 527 electrons with an RMS value of 150 electrons. We measured the signal-to-noise (S/N) performance of the SVX-H in a 50 GeV pion test beam [7], coupled to a prototype half-ladder. The result was 17:1 S/N for the R-phi side and 16:1 S/N for the Z side, or 1400 and 1500 equivalent electron charges of noise.

The die were also selected on the basis of uniformity of sparse threshold response. This was done by varying a test charge, and creating a distribution of the charge values at which each channel was activated 50% of the time. The RMS value of this distribution was 10% for all selected die. The wafer yields following the selection criteria were 60%, 73%, 72%, and 52%.

FIG. 1 Z-side assembly with kapton, capacitors, and hybrid.

FIG. 2 The half-ladder assembly sequence, small vertical lines represent wire bonds on the kapton.

We mount the SVX die on multilayer hybrid circuit boards (Fig. 1). The SMD hybrid design derives from the initial work done by C. Haber *et al.* [2] for CDF. The hybrids are printed on an aluminum nitride (AlN) substrate which was chosen for its excellent thermal conductivity; $180 \text{ W/m}^2\text{K}$. The SVX's are die-attached with conductive epoxy to large area gold bond pads that have good thermal contact to the substrate. The die are wire bonded to the hybrid with $25 \mu\text{m}$ gold wire. The hybrid circuit is printed in a standard thick film process using inks that are specially formulated for compatibility with AlN. The circuitry is built up in 34 screen prints, involving 103 process steps. The hybrid yield was 91% for a lot of 125 pieces. The hybrids were printed and assembled at Promex [8].

The assembled hybrids were extensively tested before and after shipment to CERN, and at various stages of the assembly. Details are reported in Reference [9]. The inner and outer layer hybrids are identical, each has six SVX chips per board, or 768 channels. Custom kapton cables carry the bi-directional signals between the hybrids and an intermediate electronics board called the converter. The converter contains an analog amplifier, voltage regulators for the SVX power, and bi-directional line drivers for the signal/control bus. A pair of hybrids from either the R-phi or the Z side of two adjacent ladders are multiplexed on, and readout through the converter.

4. LADDERS

Each of the $\sim 20 \text{ cm}$ long silicon half-ladders is built from two 7 cm silicon sensors that are edge-glued with epoxy. The R-phi strips on the junction side of a pair of sensors are connected by wire bonding the corresponding strips across the glue joint. The Z-side strips, which are oriented at an angle orthogonal to the R-phi strips, are wire bonded to a thin kapton foil [10] that is glued on top of the ohmic side of the sensor.

The kapton is $50 \mu\text{m}$ thick with $2.5 \mu\text{m}$ of electroplated copper. The foil is etched to form a circuit that extends the Z-strips to the end of the half-ladder via L-shaped traces. The circuit places the electronics unit, which reads out both sides, R-phi and Z of the sensor, at the end of the half-ladder. Placing the readout at the ends of the ladders keeps unnecessary material out of the sensitive region of the detector. It also makes it easier to remove the heat generated by the electronics. Most importantly, however, the kapton foil is an elegant alternative to fabricating silicon sensors with double-metal traces.

Each electronics unit is comprised of two integrated capacitor assemblies, and two SVX hybrids. The capacitor assemblies are glued to, and separated by a thin quartz plate, called the thermal break. The quartz thermal break puts a high impedance heat path between the hybrid electronics and the silicon sensors. The two SVX hybrids, are glued to, and separated by a thin AlN plate, called the thermal tongue. The thermal tongue extends 10 mm aft of the hybrids. It is the mounting ear for the ladder, as well as a low impedance path for heat generated by the SVX. Two additional pieces of AlN are glued to the thermal tongue, building it up to nearly the same thickness as the hybrid sandwich to give the assembly greater mechanical strength. Conductive epoxy was used in this part of the assembly. The steps to build the half-ladder assemblies are shown schematically in Figure 2. A unique precisely machined custom vacuum jig was required for each of the assembly steps.

Two half-ladders become a full ladder when they are joined silicon to silicon and with the half-ladder electronics located at opposite extremities. The joint is held with small plates of fiber glass that are glued to the sensors and which span the joint. A $250 \mu\text{m}$ thick, 31.4 cm long carbon fiber rib with a trapezoidal cross section is then glued to the junction side of

FIG. 3 An exploded view of an SMD half-support.

the detector, with an insulating strip of kapton between. The rib was designed to match the coefficient of thermal expansion for silicon. It gives mechanical rigidity to the ladder assembly, which would otherwise sag unacceptably. The rigidity comes at the expense of increased sensitivity to assembly tolerances. The SMD ladder was modeled with a finite element code by a mechanical engineering group, MEE-12, at Los Alamos National Laboratory (LANL). They found that the SMD ladder assembly without the rib could withstand 3 mm deflection for a pure bending condition, and 4° angle of twist for the pure torsion condition before reaching the critical yield strength for the silicon. With the addition of the rib, the limits were reduced to 1.8 mm and 0.6° respectively, however, even these smaller limits are well outside the designed assembly tolerances.

On the end of the ladder called the fixed end, mounting holes are milled out of the thermal tongue, one of which is a precision locator. On the other end of the assembly, called the free end, two open slots are milled to allow for thermal expansion of the ladder length. One of these slots is also a precision locator. There are two types of ladder, a straight assembly for the inner layer, and an offset assembly for the outer layer. All assembly was done by the University of Perugia and the University of Geneva.

5. THE SMD MECHANICAL SUPPORT

The SMD mechanical support is designed to hold 24 silicon ladders, 48 converter boards with cooling screens, 25 thermal sensors, 6 capacitive alignment heads and 8 water cooling pipes (Figure 3). The mechanical support was designed by the engineering group, TA1 at CERN, with consultation from MEE-12, at LANL. The mechanical support was machined and assembled at NIKHEF. The one meter long

support is built from two halves. Each half-support is a glued assembly comprised of three hemi-cylindrical sections joined together by two aluminum ladder half-rings. Each section is made from two $300\ \mu\text{m}$ sheets of $0^\circ\text{-}90^\circ\text{-}0^\circ$ carbon fiber facing, separated by a 3 mm thick NOMEX honeycomb. A section is 0.26% of a radiation length. The two outer sections support the converters and alignment capacitors. The silicon ladders are mounted to the ladder half-rings, and span the middle section. All three sections are covered with aluminum foil to make the electrical connection that keeps the support at a fixed voltage potential. The final part was surveyed after machining and assembly. The accuracy of the main dimensions was found to be good to $\sim 10\ \mu\text{m}$.

Two aluminum half-flanges are glued to the extremity of each outer section, and are called suspension flanges. After installation, the SMD is supported at each end on three points located on the suspension flanges. The SMD is electrically isolated from the support flange on ruby spheres.

The SMD support becomes mechanically rigid only after the two halves are joined and locked by a second pair of aluminum flanges, called the closing flanges. A finite element program, CASTEM, was used to model the support under mechanical loading. The maximum deflection of the ladder ring was predicted to be $160\ \mu\text{m}$ for the unlocked assembly, but only $20\ \mu\text{m}$ for the closed and locked assembly.

6. THE COOLING SYSTEM

The total heat load generated on the 96 SVX hybrids is $\sim 100\text{W}$. The SMD is water cooled to maintain good thermal stability. The aluminum ladder rings contain a water cooling channel that is 1 mm high by 10 mm wide. The small aspect ratio of the width to the height of the cooling channel minimizes the thermal boundary layer, and hence results in a

much lower temperature differential between the fluid and the aluminum wall. This effectively lowers the operating temperature of the electronics. The cooling channels were machined in the ladder half-rings by an electro-erosion process, and then sealed by electron beam welding. Each half-ring supports and cools 6 inner and 6 outer electronic units, or 24 hybrids.

The AlN hybrids and the thermal tongue provide a heat conduction path to the cooled ladder half-ring. The results of a finite element simulation run by the MEE-12 group at LANL, however, suggested that it was necessary to have an additional conduction path closer to the heat source to reduce the SVX operating temperature, and hence the temperature in the region of the silicon sensors. It is desirable to keep the temperature at the silicon as close to assembly-room temperature as possible in order to avoid over stressing the thin glue joints. We laid out the hybrid with a 3 mm strip across the width, free of any components. When the ladder is assembled onto the support, this area is positioned 0.5 mm above a corresponding flat that is machined on the ladder ring. The gap between the flat and the hybrid is filled with a heat sink compound. Several products were evaluated experimentally. Dow Corning 340 silicone compound [11] was chosen on the basis of its thermal conductivity, which the manufacturer specifies at $0.42 \text{ W/m}^2\text{K}$, and because of its long term viscosity characteristics. The finite element model predicts that approximately 50% of the heat flow from the SVX to the ladder rings is through the grease. The remaining 50% is channeled through the aft connection made by the thermal tongue to the ring (Fig. 4).

FIG. 4 A cross-sectional view of a half-support ring.

The temperature predicted in the region of the silicon sensors by the model is 22°C , given 18°C input water. We currently input approximately 14°C cooling water to the SMD and record a temperature of $\sim 18.5^\circ\text{C}$ in the region near the silicon sensors, which is consistent with the model. The average temperature of 10 sensors located on the mechanical support near the electronics units is 17°C . During stable running conditions, the temperature at these locations has been stable to a few tenths of a degree C.

The converter electronics dissipate an additional 100 W of power. These boards are cooled by thermal screens designed by the University of Lausanne. The screens are made with thin aluminum plates soldered to a U-shaped 2.5 mm diameter cooling tube. They are positioned 1.0 mm above the converter.

The average temperature measured on the support near the converters is 23.5°C .

An external screen covers the outside of the SMD. The screen is made from a laminate of two 200 μm thick carbon fiber sheets, separated by a 300 μm thick sheet of cardboard. The laminate is formed into a half-cylinder under heat and pressure over a mandrel. Inner and outer surfaces of the screen are covered with aluminum foil. The screen shields the outside world against residual radiant heat from the SMD, and protects the SMD against external electromagnetic pickup.

7. METROLOGY

Optical survey of the SMD was performed with an Olivetti Inspector Maxi 900V [12] 3-D coordinate measuring machine at CERN. The precision of the measurement coordinates in X and Z, the transverse and longitudinal directions of the machine, were determined to be better than 2 μm . The precision in the Y coordinate, the direction normal to the ladder plane, depends on the magnification lens that is used, but in all cases is better than 20 μm . Each silicon ladder was surveyed before assembly on the support. The sigma of the residuals distribution of the measured coordinates Vs their design coordinates was 4.5, 8.2 and 11.7 μm for the inner ladders and 5.0, 5.2 and 9.1 μm for the outer ladders in X, Z and Y, respectively [13].

FIG. 5 The SMD on the metrology stage.

A similar measurement was made on the outer layer of the fully assembled SMD, which was oriented vertically for the survey (Figure 5). The sigma of the residuals distribution of the measurements made on the mounted ladders Vs the measurements made on the unmounted ladders was 2.0, 2.3, and 12 μm in X, Z, and Y respectively. These numbers give us an estimate of the rigid-body performance of the ladders, and of the precision of the assembly to the support structure. Most of the 12 μm spread in the Y distribution is actually beneficial, because a slight outward bow in the unmounted ladders is corrected by placing them on the structure. The inner ladders were not surveyed on the assembled SMD.

8. ASSEMBLY AND INSTALLATION

The SMD was assembled by halves. A special tool was designed to hold the half-support, and rotate it through 360°, pinning it in place at any 15° increment. The ladders were placed on the ladder rings by hand. The holes and slots on the fixed and free ends of the ladder fit over threaded metal location pins that were glued to the ring. Small screws and nylon washers secure the ladders. The assembly clearance for the shingled inner ladders was particularly tight. The wire bonds from the Z side of a placed ladder had a nominal distance of 500 μm to the wire bonds of the overhanging R-phi side of the adjacent ladder. The two sets of wire bonds carry the full bias voltage difference of the two sides of the sensor. We coated the wire bonds in these critical areas with a transparent, room-temperature-curing junction coat compound; Dow Corning 3-6550 [11]. The coating was effective for both mechanical and electrical protection.

The two halves of the SMD were assembled around the beam pipe on a custom designed tool that was built around a SFERAX [14] precision rail system. The assembled halves were pinned and locked with the closing flanges. The full SMD was held cantilevered off a sliding carriage and eased into position in the opening between the beam pipe and the support flange. The nominal clearance from the outer radius of the SMD to the support flange was 1.2 mm. The nominal clearance from the SMD inner radius to the beam pipe was 2 mm.

Two independent displacement monitoring systems were installed to track the long term mechanical stability of the SMD. One is a laser-based system. Optical heads were glued to a reference surface around the SMD. Infrared light is directed onto the outer layer silicon sensors through holes in the electromagnetic screen. The centroid of the light spot is calculated and monitored to detect movement in the structure. The other system is capacitive, and it measures the relative displacement between probes located on the SMD and ground targets located on a reference surface. We expect the long term resolution of these systems to be better than 10 μm .

9. SUMMARY

A 72,672 channel microvertex detector, the SMD was assembled and installed into the L3 detector in early 1993.

Preliminary analysis of metrology data indicates that both the ladder and the detector assembly meet the original design goals. Temperature measurements on the SMD mechanical support are consistent with a finite element model, and indicate that the cooling system is effective in removing the nearly 200W of heat generated by the electronics. The SMD has been operational and writing data to tape for most of the LEP 1993 run.

A. Acknowledgement

We gratefully acknowledge J.G.Boissevain (LANL) for the design of the custom kapton cables for the hybrid.

We also thank O. Runolfsson (Opal), and B. Boulter (Delphi) for thier assistance in wire bonding parts of the silicon ladder assemblies.

10. REFERENCES

- [1] Batignani *et al.*, " Development and performance of double sidedsilicon strip detectors" Nucl. Instr. and Meth. A310 (1991) 160-164
- [2] C. Haber *et al.* " Aluminum Nitride thick film hybrids for a silicon microstrip vertex detector", The Intl. Journal for Hybrid Microelectronics, Vol. 14, No. 4, (1991) 129-135
- [3] Swiss Center for Electronics and Microtechnology, Neuchatel, Switzerland
- [4] J. Ellison *et al.*, "Punch-through currents and floating strip potentials in silicon detectors," IEEE Trans. on Nucl. Science, Vol. 36, No 1, (1989) 267-271
- [5] S. Kleinfelder, *et al.*, " A flexible 128 channel silicon strip detector instrumentation integrated circuit with sparse data readout,"IEEE Trans. on Nucl. Science, Vol 35, No.1, (1988) 171-175
- [6] United Technologies Microelectronics Center, Colorado Springs, Co., USA
- [7] M.Biasini *et al.*, "Performance on test beam of the L3 double-sided silicon microstrip detector," presented at the "3rd London Conference on Position Sensitive Detectors," Uxbridge, England, (1993)
- [8] Promex, Santa Clara, Ca., USA
- [9] B. Bertucci *et al.*, "Experience with the SVX-H chip in the construction of the L3 Silicon Microvertex Detector," Presented at the "Topical Seminar on Experimental apparatus for High Energy Particle Physics and Astrophysics", San Miniato, Italy, (1993)
- [10] D. Dibitonto *et al.*, " Ultra-thin, high precision flex cable for the L3 Silicon Microvertex Detector," L3 note # 1453, CERN. Submitted to Nucl. Instr. and Meth.
- [11] Dow Corning Corporation, Midland, Mi., USA
- [12] Olivetti and Co. SpA, Ivrea, Italy
- [13] V. Krastev, "Analysis of the Spring 1993 SMD- Metrology Data," L3 note # 1484, CERN.
- [14] SFERAX SA, Contailod, Switzerland

**DATE
FILMED**

1 / 26 / 94

END