I_{DDQ} Testing and Defect Classes - A Tutorial

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Abstract

I_{DDQ} testing of CMOS ICs is a technique for production quality and reliability improvement, design validation, and failure analysis [1]. The origin and basic concepts of I_{DDQ} testing are reviewed. The relationship of I_{DDQ} testing to other test methods is considered in the context of the whole IC life cycle from design, fabrication, and test through end use. A comprehensive test strategy is described that uses defect classes based on defect electrical properties rather than traditional fault models [2].

Introduction

Continued advances in the design and fabrication of CMOS ICs provide exciting challenges. Figure 1 shows an example of this [3]. The detection and elimination of short and open circuits within and between complex, multiple interconnection layers is an increasing concern. Quiescent power supply current (I_{DDQ}) testing significantly improves the quality and decreases the production cost of state-of-the-art CMOS ICs. It is being merged successfully with conventional Boolean approaches, such as functional or stuck-at fault testing, to improve the detection of defects and failure mechanisms early in the manufacturing process. As an important part of quality manufacturing, it provides information required for process evaluation metrics and corrective action. When combined with optical and electron beam diagnostic techniques, it is also useful for failure mechanism identification and defect localization [4]. In addition, I_{DDQ} testing is very effective for design verification and first silicon characterization, reducing time to market.

Fault models were used in the 1970-80 era for generating test patterns and evaluating "test coverage" for ICs. A fault is a hypothesis of improper circuit behavior (logical or electrical failure). A stuck-at-fault (SAF) is usually assumed to describe a node that behaves as if it were permanently stuck at logic 0 or logic 1, but this definition has not been formalized by any standards organization. SAF coverage evolved as the de facto test metric for many companies in the 1980s. Despite extensive use of SAF coverage as a quality metric, no data proving that 100% SAF testing guarantees

Fig 1. Five level interconnection with CMP planarization (photo courtesy of Mike Chisholm, Texas Instruments).

zero defects for CMOS ICs have been published. In fact, data from manufacturers show SAF coverage to be a relatively poor test metric for IC, board, and system defect levels [5-10]. These production and field results are consistent with increasing evidence that most defects are detected more effectively by I_{DDQ} and certain other test methods than by SAF tests [11-34]. High SAF coverage is expensive and difficult for many manufacturers to achieve. SAF coverage cannot even be determined for many ICs.

The term "defects", as used here, refers to physical and electrical imperfections, whether due to design or layout errors, fabrication flaws, failure mechanisms, or other causes. Defects are the objective of the test process. A comprehensive test strategy is described here that uses defect classes based on measured defect electrical properties. Defect classes differ from traditional fault models. The defect class approach requires that the test strategy match the defect electrical properties, as opposed to fault model method which requires that IC defects match the fault definition. I_{DDQ} and some methods of Boolean testing are combined to quantify defect coverage, providing an approach for minimizing defects by eliminating test escapes.

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Background

I_{DDQ} testing is linked to the history of CMOS IC design and fabrication. In 1963, a few months after starting work for Fairchild Semiconductor, Frank Wanlass originated and published the concept of complementary-MOS (CMOS) logic circuitry [35]. It occurred to him that a CMOS circuit "would use very little power" and that "in standby, it would draw practically nothing, just the leakage current." The first demonstration circuit, a two transistor inverter, consumed just a few nanowatts of standby power. Equivalent bipolar and PMOS gates consumed milliwatts of power even when in standby mode. CMOS shrank the standby power consumption by six orders of magnitude. It was therefore a fact that CMOS circuits with standby power consumption greater than a few nanowatts were "defective."

I_{DDQ} Testing

I_{DDQ} is the symbol for the quiescent power supply current in MOS circuits. In addition to "standby current" and "leakage current", I_{DDQ} has been referred to with other terms and symbols. I_{DDQ} (I_{SSQ}) testing measures the current of the V_{DD} (V_{SS}) power supply in the quiescent logic condition (the stable condition between logic state transitions). Fig. 2 shows the basic principles of I_{DDQ} testing. In this figure, a generalized IC has a gate oxide defect in a p -channel transistor of an internal logic gate. When the input to the logic gate changes from a logic 1 to a logic 0, the power supply current (i_{DD}) increases to a high value during the logic state transition and then decreases. When i_{DD} has stabilized, the I_{DDQ} measurement is made, as indicated by the vertical arrow on the time axis. The magnitude of I_{DDQ} changes from a low value before the logic state change to an elevated value after it due to the gate oxide short. If the gate oxide short did not exist, I_{DDQ} would have returned to the initial low value. For carefully designed, defect-free ICs, I_{DDQ} can be in the 1 to 100 nA range.

Fig 2. Generalized CMOS IC with V and I waveforms.

In the mid-1970s, some manufacturers, such as Philips in the Netherlands and Sandia National Labs [10] in the United States, began to use extended I_{DDQ} testing to improve defect detection and enhance the reliability of their ICs. A strong correlation between high I_{DDQ} and functional or dynamic test failure was often observed [36]. Nelson and Boggs found a correlation between elevated I_{DDQ} and increased propagation delay [37]. I_{DDQ} tests were usually performed slowly, using a precision measurement unit or simple custom circuitry. However, the I_{DDQ} test time was acceptable because the number of test vectors was usually low. In 1983 Toshio Maruyama designed a faster circuit that became the first capability specifically marketed for I_{DDQ} testing by a commercial IC test equipment company (Advantest). Other companies now provide I_{DDQ} test options. Circuits have been developed that enable measurements below 1 μ A at test rates above 100 kHz [38]. In 1993, the Quality Test Action Group (QTAG) was formed to develop an IEEE standard for I_{DDQ} production test fixtures [39-40].

For production, a pass/fail I_{DDQ} test is often used because it is usually faster than measuring and storing the I_{DDQ} values. Simple tests with only a few vectors and a relatively high 0.5-1.0 mA limit have been shown to be effective for detecting defects not caught by conventional scan design testing even with 99.6% stuck-at fault coverage [7]. Limits in the 1 μ A range have been shown to be effective for sea-of-gate ASICs with three metallization layers and 0.55 micron effective channel length [8]. A limit of 70 nA has been used for 1.5 micron technology SRAMs [41]. Reducing the I_{DDQ} test limit improves defect detection.

Research in the mid-1980s on the effects of common CMOS IC defects, such as gate oxide shorts, improved the selection of test vectors for defect detection [11-13]. Researchers also considered the use of I_{DDQ} test patterns for stuck-at, stuck-open, and delay fault coverage [16,42-43]. Improved methods for I_{DDQ} test pattern selection have been developed recently. A software tool, QUIETEST, can select a small subset of I_{DDQ} test vectors from a large functional test set and achieve the same leakage fault coverage as the entire functional test set [44]. Versions of the QUIETEST approach are being used successfully in commercial software tools for I_{DDQ} test pattern generation and grading.

Companies have successfully implemented I_{DDQ} testing in various ways. Recent examples include using it to reduce manufacturing costs by over 50%, to improve assembly line and field quality beyond that achieved by conventional scan design testing with higher than 99% stuck-at fault (SAF) coverage, and to cut burn-in failures in half [7,45].

IC Design

ICs designed to the original definition of CMOS logic (100% static and complementary circuitry) have very low power dissipation in the quiescent state (typically nanowatts). These "conventional" CMOS ICs are inherently I_{DDQ} testable. However, many "CMOS" ICs are actually modified or hybrid CMOS designs. Modified CMOS ICs may have circuitry, such as dynamic or domino logic elements, altered for lower silicon area or increased performance (speed) [46]. Hybrid CMOS or mixed signal ICs may have nonCMOS elements such as resistors, depletion transistor loads, or bipolar transistors. I_{DDQ} tests can be performed on ICs that are not completely conventional CMOS logic designs [47-49]. For example, 80C51 8-bit microcomputers with dynamic precharge circuitry were evaluated with I_{DDQ} tests at 50 kHz using 20,000 vectors from the vendor's test program. About 300 design-related high current states were found. For production testing, I_{DDQ} was simply ignored for these high current states using a software mask in the test vector patterns.

High I_{DDQ} logic states often result when IC power dissipation is not considered or is ranked lower than other design criteria (speed, area, etc.). For example, microprocessors may have logic states during which the internal data bus is not used. In these states, the bus may not be driven or may be driven simultaneously by more than one driver. These are logical "don't care" states for the bus, but the floating inputs of the data bus receivers or the contention of the multiple drivers can cause high I_{DDQ} . As another example, memories may have pullup resistors instead of p -channel transistors in the array. These ICs may be described in their data sheets as static CMOS, but I_{DDQ} will be milliamperes when the IC is enabled due to the noncomplementary design of the memory cell. Despite designed-in high current logic states due to pull-up resistors, I_{DDQ} testing has been used to identify shorts that caused timing delays in 256K SRAMs [50]. ICs with intentional or unintentional high current conditions can result from design practices that originated with higher power dissipation technologies such as TTL and NMOS. Examples include pull-up resistors in input buffers and single pass transistors (without feedback latching) instead of complementary transmission gates. Low power alternatives simply may have not been considered.

It is also common to hear the **issue of silicon area overhead** mentioned as a reason for not designing 100% static, complementary CMOS circuits. Experience at Sandia Labs has shown that overhead penalties, if they exist, are outweighed by the benefits of complete CMOS designs. For example, Sandia's CMOS emulation of National Semiconductor's 32C016 16/32 bit NMOS microprocessor has about 65,000 transistors, nearly the same number as in

the 32C016. Because Sandia's version is a conventional CMOS design, very high defect coverage can be achieved using less than 3000 I_{DDQ} test vectors, an accomplishment that would be impossible using conventional techniques for the NMOS design. Similarly, Sandia's 80C51 emulation has very high defect coverage using I_{DDQ} testing with the vendor's test set, but the SAF coverage of the commercial 80C51 could not even be determined because conventional fault simulation was estimated to take over 21 years using a MACH 1000 hardware accelerator.

The microprocessor and memory examples demonstrate that the capabilities of I_{DDQ} testing do not inherently diminish as the IC complexity increases. The number of transistors increases as the IC complexity grows, but the size of the transistors and their junctions usually decreases with technology advancements. Thus, the background junction leakage current can remain substantially unchanged with higher levels of integration. It has also been shown that designing for I_{DDQ} testability is compatible with modified CMOS circuitry for critical speed or area requirements. Josephson demonstrated that I_{DDQ} testing can be accomplished for a RISC architecture microprocessor with about 1 million transistors that operates above 75 MHz [48-49].

It is important to ensure that the logic is implemented in a manner that maintains the low power dissipation capability of CMOS. This requires that design targets and margins for parameters such as thin and thick oxide threshold voltage be appropriately chosen. If, for example, the thin oxide threshold voltage drops to about 0.5 V or less, the transistor off-state leakage of some technologies may begin to exceed the reverse-biased junction leakage. If the background current increases, it becomes more difficult to detect design and defect problems.

In addition to increased defect and fault coverage, I_{DDQ} testing enables rapid identification of many design, layout, and fabrication problems (i.e., processing problems of a nondefect nature, such as excessive lateral diffusion). For some companies, the value of I_{DDQ} testing has been proven by quickly identifying design errors during validation/verification testing of the first wafer lot (first silicon). One gate array company uses I_{DDQ} testing routinely to identify routing errors that leave logic gate inputs unconnected. The unconnected, floating inputs cause elevated I_{DDQ} that is readily detected with a few test vectors.

IC Fabrication

Difficulties with processes critical to CMOS IC manufacturing, such as good coverage of oxide steps by metallization, have routinely plagued the industry. Intelligent decisions for process improvement require

specific information on defects and failure mechanisms. I_{DDQ} testing is a very sensitive method for identifying defects [13-14]. As a pass/fail production test, I_{DDQ} testing provides a better quality metric for physical defects than testing based solely on the unrealistic assumption that all IC abnormalities produce internal stuck-at faults or incorrect logic outputs. For failure analysis, I_{DDQ} techniques can provide rapid failure mechanism identification and physical localization. These include the use of $I_{DDQ} - V_{DD}$ transfer curve signatures, analysis of the relationship between I_{DDQ} test vectors and the logic structure of the IC, and digital processing of electron beam voltage contrast images [11,41,51-55]. Also, optical measurements of light emission from the IC for high I_{DDQ} logic states can be used for defect localization [56].

I_{DDQ} testing for common CMOS IC defects and failure mechanisms during manufacturing is relatively well understood. These include gate oxide shorts, interconnect bridges, and interconnect open circuits. The effect of these on logic behavior may be complex and time variant. Physical shorts and their related fault models bring to mind an image of a circuit schematic with two nodes bridged by a low value "ideal" resistor (e.g., $< 50 \Omega$). In reality, shorts in ICs often have resistances greater than 1 k Ω or have nonlinear characteristics. Interconnect bridging shorts have been shown to have node to node resistances ranging from several hundred ohms to greater than 20 k Ω due to the geometry or contact characteristics of the bridging material [29,50,57-59]. Gate oxide shorts commonly exhibit diode behavior due to the polysilicon and substrate silicon doping differences [11-12,41,60-61].

Open circuits may not behave as "ideal" circuit discontinuities. Some interconnect "open" circuits have unstable, high resistances at contact interfaces [18] and nonlinear electrical characteristics [20]. Open circuit defects have been observed to cause node voltages that turn on p - and n -channel transistor pairs, thus elevating I_{DDQ} .

Defects and failure mechanisms often initially cause increased I_{DDQ} without logical malfunction (functional failure). It may seem costly to reject ICs that have increased quiescent power supply current but are still performing their logic functions. However, it has been demonstrated that the defects and mechanisms responsible for elevated I_{DDQ} often greatly reduce reliability [12,45,62-63]. Also, high I_{DDQ} can cause premature failure of battery (power-limited) systems. In addition, there are quality and yield concerns. High I_{DDQ} can be symptomatic of a significant processing problem that may not be in control. Defects and failure mechanisms may worsen in time, resulting in major yield or reliability problems. Ignoring these defects and mechanisms can produce a false sense of security due to inaccurate quality or performance metrics.

IC Test Methods

Most companies adopt individual test approaches since there is not yet general agreement on an optimal (low defect level) test strategy that can be quantified and accepted by both customer and supplier. Most companies use some combination or subset of the following tests. These tests apply to CMOS ICs (complementary, static designs) and to ICs with hybrid CMOS circuitry (resistor loads, dynamic logic, etc.), depending upon the particular design.

Parametric tests. These tests range from simple continuity and leakage current measurements to complex timing tests (e.g., rise/fall, prop delay, setup and hold times, etc.). They may be performed with a short functional test during the initial part of the test program to assure basic circuit operation or may involve extensive and lengthy tests to verify critical logic path performance.

Boolean tests. These tests use voltage sensing to verify logic functionality and include the following types of tests: at-speed functional, delay fault, random pattern, SAF, V_{IL}/V_{IH} , and f_{MAX} testing [64]. A functional test uses a large test sequence designed to functionally verify operation at the design frequency (at-speed) or at lower frequencies to provide margin information (e.g., with input and output levels set at 20% and 80% of V_{DD}). The functional test vector count can become exceedingly large for modern ICs (many millions of vectors). The SAF test provides Boolean controllability and observability. Delay fault tests use a gate level, two-vector pair to measure circuit propagation delay. The first vector sets the logic output with an initializing vector and the second vector (state change vector) provides the controllability and observability for the targeted path or gate. These tests can be included as part of the timing tests. V_{IL}/V_{IH} testing finds the minimum high logic input voltage (for V_{IH}) and maximum low input voltage (for V_{IL}) for all inputs (and input conditions on I/O pins) for correct circuit operation at a fixed frequency. The f_{MAX} test uses a functional test set and repeats this set for increasing clock frequency until the IC fails.

I_{DDQ} (I_{SSQ}) tests. Many companies perform some type of I_{DDQ} testing, such as power down tests, with a small set of test patterns (vectors). I_{DDQ} testing does not require propagation of logic values to the primary outputs, resulting in small vector sets with high defect coverage. The I_{DDQ} pseudo stuck-at-fault (PSAF) test applies a SAF vector pattern to the input nodes of each logic gate, but only propagates the signal to that gate's output node [65-66]. The PSAF test vector set has a small vector count compared to a SAF test set. PSAF tests provide I_{DDQ} node coverage for six bridge defects of each transistor in the logic gate and for certain open circuit defects [44].

Defect Classes

To develop a test strategy, the electrical behavior of defects is used to define three general categories. These three categories of defect classes are: (A) bridge, (B) open circuit, and (C) parametric defects causing delay that may not be bridge or open circuit defects. Within these general categories are defect classes denoted as type-1, type-2, etc. Bridge defect classes were partially chosen by their natural links to either Boolean or I_{DDQ} testing. Open defect classes were characterized by more distinctive electrical properties that can require both testing methods to guarantee detection. The parametric delay defect class has unique and difficult detection properties. Supporting data and an extensive set of references for defect electrical behavior are provided in [2].

A. Bridge Defect Category. Bridge defects at transistor node, logic gate I/O, and power bus circuit hierarchies may occur in, or with, a combinational or sequential circuit. Bridge defects include all defects and failure mechanisms that cause unintended electrical connections across two or more circuit nodes. Bridges have nonlinear or linear (ohmic) I - V properties with resistance from near zero to >1 M Ω . Nonlinear bridge defects include most types of gate oxide shorts, soft pn junctions, transistor punchthrough, and some particulate bridge shorts. Ohmic shorts also occur in IC patterning defects that leave "bridges" of metal (or polysilicon) and in certain forms of gate oxide shorts [11].

Bridge defect resistance is the dominant factor in evaluating bridge detection methods. For I_{DDQ} testing, bridge resistance $> \sim 5$ M Ω can be detected with the proper test pattern, depending on the limit ($< \sim 1$ μ A). Correct Boolean functionality exists for signal node bridge defects when the defect exceeds a *critical resistance* [61]. Critical resistance is a function of the contending transistor current drive strengths and therefore varies with circuit design, logic input levels to contending logic gates, and process variation. Critical resistance may lie in a range as low as 10 Ω to about 5 k Ω . Vierhaus *et al.* found that critical resistance decreases as transistor size decreases [67]. For one bridge defect location, they found that critical resistance dropped from 6 k Ω to 4 k Ω when comparing a 1.5 μ m to a 1.0 μ m technology. They made a related observation that there is a critical resistance associated with Boolean delay error measurements. Hao and McCluskey simulated resistive gate-source (GS) and gate-drain (GD) shorts and found critical resistances of about 1 k Ω and 600 Ω [60]. Critical resistance varied with width/length (W/L) ratios and input logic patterns.

Bridge Type-1 Combinational Defect Class. This defect class includes defects that cause the six transistor node bridges (all bridge possibilities between the gate, source, drain, and substrate nodes) [44], logic gate I/O signal node to power

bus bridges, and power bus-to-power bus bridges. These defects have various physical causes and include ohmic and nonohmic shorts. However, they have similar I_{DDQ} and Boolean responses, share a common test pattern for their detection, and are thus considered as a single defect class.

Bridges can occur from signal nodes to the V_{DD} or V_{SS} power bus. Segura *et al.* studied bridge defects in test chips from a signal node to the V_{DD} bus. They found a critical resistance between an inverter node output and V_{DD} of about 3 k Ω [61]. I_{DDQ} was elevated over a range of defect resistance and transistor W/L ratios to about 50 μ A for defects of 100 k Ω . Bridges can also occur between power buses. Power bus bridges (V_{DD} to V_{SS}), such as well to substrate soft breakdowns, are regarded as Boolean insensitive but are easily detected with I_{DDQ} testing for any vector.

This defect class therefore includes nine types of defects: (1) six nodal defects per transistor, (2) two defects between signal nodes and the V_{DD} or V_{SS} power bus, (3) one defect between one power bus and another. These defects are insensitive to Boolean tests unless the resistance is low, e.g., below about 1 k Ω . All nine types of defects are 100% detected by I_{DDQ} pseudo SAF test patterns.

Bridge Type-2 Layout Defect Class. These defects occur at a variety of locations and, as opposed to the type-1 class, they require identification from the layout. These defects include bridges between two or more logic gate signal nodes or between logic gate I/O to transistor nodes. This defect class shows similarities to the type-1 defect class in having a relatively low critical resistance that affects Boolean functionality. This critical resistance is a function of the relative current strength of the contending transistors and is thus a function of the input logic values of the contending gates.

Bridge defects between certain internal nodes of a sequential logic element and a node of another logic element can cause unique behavior [31,33,68]. Rodriguez *et al.* found a sequential cell critical resistance of about 2 k Ω for their technology [31]. They also identified 37 total bridges from an inductive fault analysis. I_{DDQ} testing detected 100% of these defects when the defect resistance was above 2 k Ω and 92% when the defect resistance was less than 2 k Ω . When the defect resistance was less than 2 k Ω , the external gate **could change the stored state** of the sequential circuit so I_{DDQ} was not increased. This suggests that tests for bridge defects in sequential elements, such as in scan circuits, should include I_{DDQ} and Boolean vectors.

Most layout dependent bridge defects are easily detected by I_{DDQ} tests with patterns covering all likely bridges. These defects are insensitive to Boolean tests unless the resistance is low (e.g., below about 1 k Ω). They may also be insensitive

to Boolean delay testing if the bridge resistance exceeds about 100 Ω . Type-2 defects require identification of only those nodes having a reasonable likelihood of bridging. Otherwise, for n nodes, the possible number of node to node bridges would be $(n^2 - n)/2$, a very large number. VLSI circuits are too large for possible bridge nodes to be identified manually so software, such as VLASIC [69] or CARAFE [70], must be used. Others have used a capacitance extractor to identify potential bridges in the same interconnection layer [66].

Bridge Type-3 Sequential Defect Class. This defect class includes transistor node bridges of sequential circuits. These bridge defects can be detected by a four pattern I_{DDQ} test performed with sequential elements, such as flip-flops, in both clock phases for both logic states. Each design style of sequential circuitry must be individually analyzed since some designs contain nodes that are not I_{DDQ} testable. Circuit scan chains would typically be tested with the flush and shift tests recommended by Bennetts [71] while measuring both I_{DDQ} and Boolean responses. The flush test initializes the scan chain with logic 1s (0s) and then clocks 0s (1s) through the chain. The shift test uses a 00110011... sequence through the chain to place each flip-flop in all combinations of its present and next states. I_{DDQ} would be measured for both clock states at both logic values. The I_{DDQ} test will normally detect all bridges except a bridge from the latch to an external gate while the Boolean tests observing the scan chain will detect those that I_{DDQ} misses [31-33,68].

B. Open Circuit Defect Category. Open circuit defects are unintentional electrical discontinuities. They can cause electrical behavior that may vary greatly and be difficult to predict. These defects include open contacts (missing metal or unopened oxide), metallization opens (patterning, improper etching, electromigration, or stress voiding), or opens in diffusion or polysilicon (mask or fabrication errors). Open circuit defect properties depend primarily on defect size, defect location, local electrical structure, and process variables [15,18,20,23-26,28,34,50,72-73]. Production and test IC data are used to define six open circuit defect classes that account for all open circuit behavior.

Open Type-1 Transistor-On Defect Class. An open defect can cause a transistor to be permanently on or on for certain logic states. This defect class is 100% detectable with I_{DDQ} testing using PSAF patterns. Boolean testing for this class is difficult because defects in this class can cause delay attributed to a single transistor. The delay signal may be small and the delay fault test pattern must target individual transistors.

Open Type-2 Transistor Pair-On Defect Class. An open defect can cause a transistor pair (e.g., a p -channel transistor and an n -channel transistor with a common gate signal) to be

permanently on. This defect class is 100% detectable with I_{DDQ} PSAF patterns. It is also detectable with Boolean SAF or delay fault patterns.

Open Type-3 Transistor Pair-On/Off Defect Class. An open defect can cause one transistor of a transistor pair to be on and the other transistor to be off. This defect class is detected with a Boolean test set and the test patterns may be either delay fault or SAF. I_{DDQ} is usually not increased for this defect class.

Open Type-4 Sequential Open Defect Class. Large open circuit defects in sequential circuits cause either degraded voltages (with or without Boolean error) or strong clamping to a supply voltage [31-33,68]. Degraded voltages are detected by I_{DDQ} tests and nodes clamped to a supply voltage are detected by Boolean tests.

Open Type-5 Transistor-Off Defect Class. An open defect can cause a transistor to be permanently off or off for certain logic states. This type of defect can cause a combinational circuit to have sequential circuit behavior. Detection of this "memory" effect is difficult to quantify. A 2-pattern Boolean test that targets each transistor is the only test that guarantees 100% detection but this test can be numerically intractable due to the need to prevent glitches on other inputs of the gate. This defect can be detected by chance with Boolean and I_{DDQ} tests.

Open Type-6 Delay Defect Class. This defect class includes the delay effect caused by slow charge transfer across small discontinuities, such as metal electromigration or stress voids. These small defects can transfer charge primarily by tunneling rather than capacitive coupling [20]. Detection depends upon the quality of the delay defect test patterns and their ability to examine all possible interconnect open situations. I_{DDQ} testing does not target this type of defect, but by chance may detect them when the additional signal rise or fall times cause increased I_{DDQ} coincident with the measurement strobe. The defect influence may be small so the voltage or current effects can be near or at the circuit noise level, making 100% detection difficult.

While the response of certain open circuit defects is not always predictable, the possible responses are bounded. Therefore, test strategies for open circuit defects can take account of all six possibilities.

C. Parametric Delay Defect Category. A special defect class is not defined for all defects causing delay since some defects that fall into the bridge or open defect classes also cause delay. For example, resistive bridges above a critical resistance (e.g., 1 $k\Omega$) cause delay. The parametric delay defect category defines a broad class of defects that typically are not suited for any of the bridge or open defect classes. It

is a difficult defect class to detect. Delay defect properties are discussed, followed by a defect definition.

Defects cause delay in CMOS ICs in two ways: (1) weakening of logic levels, (2) alteration of parameters in signal transmission paths such as via resistance, transistor thresholds, W/L variations, etc. Weak logic gate voltages have an interesting relation to propagation delay. Vierhaus *et al.* studied the effect of bridge defect resistance on Boolean functionality, delay error, and I_{DDQ} [67]. They found for several combinational logic circuits that delay testing was feasible up to critical defect resistances from about 5 k Ω to 10 k Ω while I_{DDQ} testing was feasible up to resistances of 5 M Ω . Above 5 k Ω to 10 k Ω , the delay signal required finer resolution of the timing error in the range of 10%-20% percentage error. They concluded: "... zero-defect based testing clearly is impossible without I_{DDQ} -based methods, delay fault testing cannot be used as a substitute. This does not affect the necessity for path-based delay fault testing covering distributed fault effects." Lanzoni *et al.* studied bridge defect delay and I_{DDQ} properties using a voltage controlled transistor to vary a bridge resistance on a test chip [74]. They found that the relative increase in the propagation delay due to the resistance could be small and difficult to detect with Boolean delay testing.

I_{DDQ} leakage to, or from, a signal node weakens node voltages and affects rise and fall times if the leakage path is to a power bus. SPICE simulations show that transition times become significantly degraded when leakage currents exceed approximately 10% of the current strength of the pull down transistors.

Many defects causing delay are I_{DDQ} detectable. However, a class must be defined for defects that cause delay error and do not elevate I_{DDQ} . These include defects that cause abnormal R_{via} , V_T , W/L , etc. The voltage error signal may be in the tester noise. Accordingly, this defect class is defined as the parametric delay defect class. It occurs in combinational and sequential circuit elements. Its nontarget (or accidental) detection by Boolean delay defect test patterns may be low. Unique test approaches need to be developed for this defect class.

Defect Class Test Paradigm

Three general defect classes have been described. How are these classes used to construct a test methodology or paradigm? Each defect class and its electrical properties allow judgment of the type of test or combinations of tests to use.

Table I summarizes the CMOS IC defect classes. The data justify whether Boolean tests, I_{DDQ} tests, or a combination of tests can achieve 100% detection.

Table I. CMOS IC Defect Classes.

Defect Class	Description	Test Method	100% Detect
Bridge Type-1	Transistor node, interlogic gate, logic gate to power bus, power bus-to-bus	I_{DDQ} Boolean	Yes No
Bridge Type-2	Layout-identified bridges	I_{DDQ} & Boolean	Yes
Bridge Type-3	Sequential intranodal	I_{DDQ} & Boolean	Yes
Open Type-1	Transistor-on	I_{DDQ} Boolean	Yes No
Open Type-2	Transistor pair-on	I_{DDQ} Boolean	Yes Yes
Open Type-3	Transistor pair-on/off	Boolean I_{DDQ}	Yes No
Open Type-4	Sequential	Boolean & I_{DDQ}	Yes
Open Type-5	Transistor-off (Memory)	I_{DDQ} Boolean	No No
Open Type-6	Delay	I_{DDQ} Boolean	No No
Parametric Delay	R_{via} , V_T , $\Delta(W/L)$	Boolean I_{DDQ}	No No

Several defect classes are 100% detectable. I_{DDQ} is the dominant test for bridge defect classes with Boolean patterns used for certain bridge defects linked to sequential circuit nodes. The PSAF I_{DDQ} pattern detects 100% of the type-1 bridge and types-1 and -2 open defect classes. Boolean test patterns (SAF or delay) will detect 100% of the type-3 open defect class (achieving 100% SAF or delay coverage may be very difficult). The type-2 bridge defect class is 100% detectable using combined I_{DDQ} and Boolean patterns for layout-identified bridges. The type-3 bridge defect class is 100% detectable using combined I_{DDQ} and Boolean flush and shift patterns with I_{DDQ} measured for all logic states of I/O and control signals. The type-4 open defect class is detectable with these same pattern combinations. These defect classes can be graded for coverage using present pattern generation capabilities.

The test detection overlap of some defect classes allow development of an efficient test paradigm. Table II regroups the defect classes into common test methods. The first I_{DDQ} test uses PSAF patterns supplemented by layout-identified bridge defects to detect four of the ten defect classes. This test has good nontarget detection of the open type-5 defect class. A sequential test pattern including I_{DDQ} and Boolean patterns detects most of the bridge and open defects. The Boolean test using SAF or delay fault patterns detects the open type-3 defect class.

The difficult defect classes, open type-5 and -6 and parametric delay, are listed in Table II as <100% detected for available test methods having nontarget detection capability. Available methods are variations of delay fault [75-76], BIST, f_{MAX} , and functional test methods.

Table II. Test Paradigm.

Test Method	Defect Class	Coverage
1. I_{DDQ} (PSAF and layout bridge patterns)	Bridge Type-1	100%
	Bridge Type-2	100%
	Open Type-1	100%
	Open Type-2	100%
	Open Type-5	<100%
2. I_{DDQ} & Boolean (Sequential Patterns)	Bridge Type-3	100%
	Open Type-4	100%
3. Boolean (SAF or Delay Patterns)	Open Type-3	100%
	Open Type-5	<100%
4. At-Speed Boolean (Delay Fault, BIST, f_{MAX} , functional)	Parametric Delay	<100%
	Open Type-6	<100%
	Open Type-5	<100%

Conclusions and Comments

CMOS ICs have increased testability when design guidelines include: (1) design for low background quiescent and transient currents (or have a test mode that supports low current), and (2) scan design. Low power designs are promising for their test benefits as well as for improved reliability and reduced heat dissipation [77]. High performance ICs can be designed for low quiescent current and a testability penalty is paid when they are not. In general, the challenges and deficiencies of CMOS IC testing

have been known for many years [78]. Data presented here show that most bridge and many open circuit defects require I_{DDQ} testing. Scan design allows efficient test vector generation and delivery for both Boolean and I_{DIX} patterns, especially for sequential circuits. Without scan, complete sequential circuit controllability and Boolean observability are challenging problems.

Defect classes provide a more accurate metric for evaluating defect detection. CMOS IC test strategies using these defect classes can reduce cost and lower defect levels. With this paradigm, tests are matched to defect properties, enabling more direct assessment of defect detection. For the test paradigm to be effective at raising the quality and reliability of ICs delivered to customers, several important factors must be considered. The relationship(s) between the predicted defect coverage for the various defect classes and their actual coverage must be understood. The types of defects and failure mechanisms that exist in the ICs directly influence this relationship as well as the cost of the test approach. The types of defects and failure mechanisms in CMOS ICs are dependent on the design, layout, and process technology and therefore can vary not only from vendor to vendor but from wafer lot to wafer lot. For one process, bridge defects may dominate while, for a different process, open circuits may prevail. The nature and stability of the defects must be considered because the behavior of some defects, such as gate oxide shorts, can change with time. This is a factor for the selection of the I_{DDQ} limit because the impact of any particular defect may go beyond simply the magnitude of current it causes.

Decisions about targeting the test approach for defect categories (bridge, open, and parametric delay) and classes within these categories are best made with as much knowledge as possible about the entire IC manufacturing process and about customer requirements. The development of the capability to grade defect coverage by defect class is the first step. Improving CMOS IC quality and reliability through improved design and test methods clearly presents many opportunities for research and technical advances.

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