Research on High-Efficiency, Large-Area, CuInSe_2 -Based Thin-Film Modules

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EXECUTIVE SUMMARY

Siemens Solar Industries (SSI) began a 3-year, 3-phase cost-shared contract on May 1, 1991 to demonstrate 12.5% aperture efficient, large area (3900 cm²) encapsulated thin film CuInSe₂ (CIS) photovoltaic modules. During Phase 2 (originally 5/1/92-4/30/93), the duration of the investigation was increased from 36 to 45 months due to fiscal constraints in the polycrystalline program at NREL. Phase 2 now spans from 5/1/92 through 8/15/93. During Phase 2, SSI met all performance milestones and program deliverables.

The module design consists of 53 series-connected ZnO/CdS/CIS/Mo/glass cells fabricated on a 4141 cm² (128.6 x 32.2 cm) glass substrate with a nominal aperture area of 3895 cm² (127.3 x 30.6 cm). Prior to the contract, SSI demonstrated a 14.1% active-area efficient, 3.4 cm² ZnO/thin CdS/CIS/Mo/glass cell and fabricated monolithic integrated modules with unencapsulated aperture efficiencies of 11.2% on 940 cm² and 9.1% on 3900 cm². The best encapsulated large area CIS module power output prior to the contract was 33.7 W, 8.7% aperture efficiency (verified at NREL) over a 3883 cm² aperture area.

Four CIS modules were shipped to NREL to meet the M3 deliverable. One module (#483-11) broke and was replaced with #308-05. The performance parameters for these modules are summarized in Table 1. The power outputs are in the 31-36 watt range. The CIS circuits are laminated behind tempered glass. Framing and termination are achieved using an extruded aluminum frame and plastic junction box (except #308-05, which utilizes a reaction injection molded frame and a two-conductor cable). M4 deliverable requirements were met with the earlier M2 deliverable module of 37.7 watts (within 3% of the 38.8 watt milestone). Furthermore, champion cell performance improved to 16.2% on 3.3 cm² active area test devices.

Table 1. Parameters for CIS modules delivered to NREL.

Module #	P _{max} (W)	I _{sc} (A)	V _{oc} (V)	FF
483-11*	37.1	2.45	24.4	.621
482-11	35.8	2.45	23.4	.624
482-8	35.4	2.49	23.5	.606
482-9	35.0	2.47	23.4	.607
308-05*	31.5	2.31	22.8	.570

*Note: Module #483-11 broke and was replaced with module #308-05.

SSI started Phase 2 fabricating large area (3900 cm²) modules pursuing the development of high-performance module processing. The large area parts proved to be a cumbersome test bed for experimentation. A strategic decision was made to utilize smaller substrates (100 cm²) in order to accelerate the progress in solving the types of technical challenges that were discovered in processing large area parts, and to then apply these solutions to larger areas to meet the objectives of the investigation.

The most critical issues determining module yield losses can be grouped into three major categories. The uniformity and reproducibility of the absorber formation process dominates the fundamental performance of the material over a large area. The interaction of the substrate with the films requires appropriate selection criteria and preparation techniques for minimizing defects that lead to shunting and areas of poor photoresponse. Performance losses near interconnects reduce module performance and can cause inadequate performance through module durability testing.

Through the adoption and further refinement of a graded absorber formation process in which the surface layer of CIS incorporates sulfur, combined with the appropriately prepared substrate, mean efficiency for 3.3 cm² test devices was improved from 9% to 14%, with the best cell efficiency of 16.2%. Perhaps more significant is that the occurrence of cells below 10% efficiency has been essentially eliminated.

Alternate techniques for fabricating interconnects were developed during Phase 2 [6]. In these approaches, the interconnects are made after the formation of the absorber and employ the application of insulating and/or conducting materials (typically polymer-based). This approach has produced a module with 11.7% aperture area efficiency, which is an SSI record for a CIS integrated module and represents significant progress toward meeting the efficiency target for the M5 deliverable (11.5% aperture efficiency for an encapsulated 3900 cm² aperture area module).

In addition to scheduled deliverables, thirty-six prototype 1'x4' RIM-framed CIS modules were delivered to NREL for the installation of a one kilowatt array at NREL's outdoor test site. SSI and NREL have also continued to monitor the outdoor performance of CIS prototype modules, demonstrating stability of the material for more than five years.

Table 2 below, a summary of the best SSI CIS performance results to date, demonstrates the potential for CIS to meet the DOE technology goals. Efforts in Phase 3 will continue to address understanding of the mechanisms which control CIS module performance and to define and implement improvements in module design and processing leading towards CIS module aperture efficiencies of 12.5%.

Table 2. SSI CIS Performance Achievements

	Power (W)	Area (cm ²)	Eff (%)	I _{sc} (mA)	J _{sc} (mA/cm ²)	V _{oc} (V)	FF
Test Structure	-	3.3	16.2*	-	41.0	0.558	.71
10x10 cm module plate	.707	60	11.7	136	35.1	7.47	.70
1x1 ft module plate	10.5	938	11.2	641	39.3	25.5	.64
1x4 ft module plate	40.8	3890	10.5	2550	37.0	24.5	.65
1x4 ft module	37.7	3883	9.7	2440	35.5	24.0	.64

(100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C)

*Active Area, reported efficiency

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SECTION 1.0 INTRODUCTION

CuInSe₂-based polycrystalline thin films (CIS) represent a promising family of materials for high-power, low-cost photovoltaics (PV), both as a stand-alone single junction and as the narrow bandgap component of a tandem structure [1-3]. Fig. 1.1 compares the photon currents generated in CIS, CdTe, thin film silicon:hydrogen alloys (TFS), and crystalline Si calculated from the optical absorption coefficients and assuming no reflection losses [4-7]. The photon current increases as a function of optical path length (that is, absorber layer thickness), and $J_{\max}$ is the maximum available photon current density for the material. For CIS with an energy band-gap of about 0.95 eV, 90 percent of the photons are absorbed in a thickness of less than 1 μm , so that CIS films only 1-3 μm thick are sufficient for thin film PV applications.

Figure 1.1. Photon current vs. optical path length for various materials. (100 mW/cm² ASTM AM 1.5 global spectrum, 25°C)

Recently CIS-based device efficiencies have surpassed 15% active area efficiency at several laboratories [8-12] demonstrating significant progress toward reaching 20% efficiency [13-14]. CIS modules are typically fabricated on soda-lime glass substrates, one of the more desirable PV substrate materials available today due to its abundance and low cost. In fact, the highest reported efficiencies for CIS-based modules and devices utilize soda-lime

glass substrates. Thus, CIS-based polycrystalline materials have the potential to address the Department of Energy (DOE) Five Year Plan polycrystalline thin-film milestones, namely the fabrication of stable modules with efficiencies of 15% (150 W/m²) or more made by scalable, low-cost techniques on inexpensive substrates.

1.1 Module Design

The module design, illustrated in Fig. 1.2, consists of 53 series-connected ZnO/CdS/CIS/Mo/glass cells fabricated on a 4141 cm² (128.6 x 32.2 cm) glass substrate with a nominal aperture area of 3895 cm² (127.3 x 30.6 cm). The standard module interconnect region is portrayed in the expanded cross section.

Figure 1.2. Basic design of 0.4 m² CIS module. The details of the standard integrated interconnect are illustrated in the inset.

In the standard module design, the cell spacing is 0.577 cm (.227"). The back electrode isolation scribe, typically .001"-.003" wide, is cut with a 1.06 micron wavelength Nd-YAG laser. The ZnO/Mo interconnect is made through a .001"-.002" wide via created in the CIS. This via is made using either laser or mechanical scribing techniques. The nominal contact resistance is in the range of 0.5-2 mΩ-cm². The ZnO/ZnO isolation scribe is also performed by either mechanical or laser scribing.

Improvements have been implemented to address yield and performance issues related to this particular module design, and are discussed in detail in Section 4.

1.2 Background

Siemens Solar Industries (SSI), formerly ARCO Solar, has pursued the research and development of CuInSe_2 (CIS) thin film PV technology since 1979. Prior to the contract, SSI demonstrated a 14.1% active-area efficient, 3.4 cm^2 $\text{ZnO}/\text{thin CdS}/\text{CIS}/\text{Mo}/\text{glass}$ cell and fabricated monolithic integrated modules with unencapsulated aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2 as noted in Table 1.1 [5,15]. As with all PV technologies, encapsulation is required in order to protect the electrical circuit from environmental exposure. The best encapsulated large area CIS module power output prior to the contract was 33.7 W, 8.7% aperture efficiency (verified at NREL) over a 3883 cm^2 aperture area [6,15]. Performance changes due to lamination and framing of CIS modules is typically on the order of -5%, primarily through the additional optical reflection loss of the front tempered glass encapsulant [15]. Outdoor testing of SSI CIS modules at NREL over a period of more than five years has demonstrated excellent intrinsic module stability [16-18] and is shown in Figure 1.3. Prior CIS research at SSI is also presented in NREL reports from a contract developing tandem cells using CIS as the bottom junction [13,19].

Figure 1.3. Outdoor performance for CIS modules measured at NREL.

Table 1.1. CIS module plate performance at the beginning of the contract.

Module	1x1 ft (55 cells)	1x4 ft (53 cells)
Area** (cm ²)	938	3916
V _{oc} /cell (mV)	464	443
J _{sc} (mA/cm ²)	39.3	37.0
V _{oc} (V)	25.5	23.5
I _{sc} (A)	.641	2.54
FF	.639	.598
Eff** (%)	11.2	9.1
Power (W)	10.5	35.8

* 100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C

** Aperture area

1.3 Objectives

The objectives of this research effort are to achieve the polycrystalline thin-film milestones of the DOE Five Year Plan, that is, the fabrication of stable encapsulated modules with 15% efficiencies made by scalable, low-cost techniques on inexpensive substrates. SSI, as noted above, has previously demonstrated encapsulated, 33.7 W, 8.7% aperture efficient CIS modules. The purpose of this program is to build upon that foundation, to address identified processing difficulties, and to improve materials and device quality over the large areas to achieve the above objectives. In Phase 2, the 3-year duration of the contract was increased to accommodate reduced annual funding levels. The contract performance milestones for encapsulated CIS modules are summarized in Table 1.2.

Table 1.2. CIS module performance milestones.

Parameter	Start	16 month	32 month	45 month
I_{sc} (A)	2.43	2.57	2.71	2.78
J_{sc} (mA/cm ²)	35.7	37.0	39.0	40.0
V_{oc} (V)	23.6	24.4	25.3	26.5
$V_{oc}/cell$ (mV)	445	460	478	500
FF	0.59	0.62	0.65	0.66
P_{max} (W)	33.7	38.8	44.6	48.5
Eff (%)	8.7	10.0	11.5	12.5

Based upon an encapsulated 53-cell, 3883 cm² aperture area module.

1.4 Discussion

In Phase 1, the emphasis of the research effort was on establishing the baseline CIS module fabrication processes including detailed characterization of the cells and interconnects [15].

In Phase 2, the initial focus was to implement the processing and characterization methods demonstrated in Phase 1 to meet the deliverables schedule for the contract and to produce statistically significant quantities of large area modules for verification of performance for both outdoor and accelerated environmental exposure. Over 2300 1'x4' CIS modules have been fabricated since processing began in the Camarillo facility. The performance distribution for these modules is presented in Figure 1.4.

Figure 1.4. Performance distribution for all 1'x4' modules produced at Camarillo facility.

Although the process produced high-efficiency cells and modules, average performance was not adequate for fabrication of representative prototype products. The origin of module reproducibility problems were unclear. Large area module fabrication was temporarily suspended to determine the critical issues affecting yield losses in module fabrication using small area test devices (3.3 cm² active area cells) and modules (60 cm² aperture area) as the experimental test bed. This shift greatly enhanced our ability to identify the root causes of yield loss in module fabrication. The most critical issues determining module yield losses can be grouped into three major categories.

1. The uniformity and reproducibility of the absorber formation process dominates the fundamental performance of the material over a large area. Section 2 describes the results of implementing a graded absorber formation process on both improved champion and average performance and yield.
2. The interaction of the substrate with the films requires appropriate selection criteria and preparation techniques for minimizing defects that lead to shunting and areas of poor photoresponse. Section 3 summarizes the impact of substrate-induced defects and techniques developed for imaging and understanding them.
3. Performance losses near interconnects reduce module performance and can cause inadequate performance through module durability testing. Section 4 details the development of alternate strategies for fabricating interconnects and diagnostics implemented for characterizing and quantifying interconnect performance.

The module deliverables are detailed in Section 5. Conclusions are summarized in Section 6. Future directions are outlined in Section 7. Finally, papers presented during Phase 2 are listed in Appendix A.

SECTION 2.0 ABSORBER MATERIAL

This section summarizes the results of investigations into the impact of the quality and uniformity of the absorber materials on cell and module yield. The fundamentals of the two-step absorber formation process are discussed. Also summarized are results of implementing a graded absorber formation process in combination with improved selection and preparation of substrates. During Phase 2, average active area cell efficiency improved from 9% to 14%, and a new champion cell was produced with 16.2% active area efficiency.

2.1 Absorber Formation Studies

Initial efforts in characterizing module yield concerns focussed on separating material issues from interconnect issues. The repeatability of the basic cell fabrication process was evaluated by producing 6048 3.3 cm² test devices. The performance distribution of these cells is plotted in Figure 2.1, superimposed with the performance distribution of the 2352 modules that were shown in Figure 1.4. The difference between the module and cell distributions are attributed to a combination of active area loss (ca. 7 rel %), series resistance losses due to the increased transfer lengths and interconnect contact resistance in modules (ca. 7% rel), and the averaging effects of large area processing (one module represents the area equivalent of over 1000 test cells) [20]. These results indicate that although high efficiency cells and modules were repeatedly produced, the basic process being used for fabrication of modules would be inadequate to produce high yields of large area modules or to meet the goals and objectives of this contract.

Figure 2.1. Module + Old Baseline Distribution.
(100 mW/cm², ASTM air mass 1.5 global spectrum, 25° C)

Several groups have undertaken research to develop an improved understanding of the reaction pathways and mechanisms for the formation of CIS-based thin film polycrystalline materials as well as an understanding of the behavior and characteristics of the absorber material and the junction that give rise to high-quality solar cells [14,21-28]. The importance of this understanding cannot be overstated; the development of predictive models for device behavior and film formation reaction pathways are critical to enable the scale-up of CIS-based thin film technology.

SSI conducted a series of experiments similar to published information [29], to evaluate the applicability of this work to SSI's two-step process approach. Figure 2.2 illustrates the selenium to metals ratio (based in ICP analysis) for Cu/Ga films, In films, and Cu/In/Ga films as a function of anneal temperature for a 15-minute anneal time in the presence of H_2Se . All films were on molybdenum-coated soda-lime glass substrates. The selenium-to-metals ratios shown for various combinations of possible binaries are based on atomic metals ratios only; they do not represent XRD or other data indicating the presence of these species. We find that Cu/Ga films reach a constant Se/Metals ratio at 300°C, and do not incorporate significantly more selenium until the temperature exceeds 400°C. The indium, on the other hand, exhibits a monotonic increase in selenium incorporation with temperature, as does the composite Cu/In/Ga film. These fundamental reaction pathway investigations will continue in order to provide the insight necessary to understand the nuances and sensitivities of the absorber formation process.

Figure 2.2. Selenium to metals ratio vs. anneal temperature.

2.2 Graded Absorber Structure

For a homogeneous absorber device model, the optimum bandgap for solar cell applications is in the range of 1.4 to 1.5 eV [30], much greater than the bandgap of pure CIS at around 1 eV. A plot of theoretical efficiency versus bandgap is shown in Figure 2.3 (based on Sze [30]). Reasonable efficiencies have been reported for various multinary polycrystalline alloys in the CIS family of materials [31]. There many such alloys from which to choose in the CIS family of materials, many of which are shown in Figure 2.4 [32]. SSI's graded absorber process evolved from work originally aimed at developing high-efficiency wide-bandgap materials.

Figure 2.3. Theoretical maximum efficiency vs. bandgap.

Figure 2.4. Bandgap of CIS-related materials.

Higher efficiencies are theoretically attainable and have been demonstrated by employing inhomogeneous absorbers using various substitutions of gallium and sulfur for indium and selenium [8-14,33-38]. These can be comprised of composite absorbers formed from films with discrete bandgaps, absorbers with a compositional gradient or theoretically with multi-junction devices. The physics of the inhomogeneous absorbers is not yet well understood, and many groups are currently working to understand the behavior of these devices.

SSI's two-step absorber formation process can be tuned to tailor compositional gradients in the absorber layers by substituting sulfur for selenium. One such process substitutes sulfur for selenium near the surface of the device. Figure 2.5 is an Auger depth profile of the composition as a function of depth into a homogeneous absorber layer. Figure 2.6 is the corresponding depth profile for the graded absorber layer, showing the sulfur incorporation near the surface.

Figure 2.5. Homogeneous absorber Auger compositional profile.

Figure 2.6. Graded absorber Auger compositional profile.

2.3 Graded Absorber Performance and Yield

The basic performance benefit from the graded absorber process was an increase in cell voltage with no significant loss in current collection. This characteristic is illustrated in the spectral response for a homogenous absorber cell and a graded absorber cell presented in Figure 2.7.

Figure 2.7. Homogeneous and graded absorber spectral response.

The graded absorber process, combined with substrate selection and preparation (discussed in Section 3), greatly improved the performance and yield of test devices. Figure 2.8 illustrates the progression of cell distribution with modifications to the absorber formation process as the process continues to be optimized. Figure 2.9 contrasts the initial homogeneous absorber cell process with the final graded absorber process. The average performance for the 6139 cells in the homogenous absorber process is 8.6%, whereas the average for the 807 graded absorber cells in the final process is 13.8%. The significant statistical data for these two populations are summarized in Table 2.1. Perhaps more noteworthy than the shift in average performance is that cells with efficiency below 10% have been essentially eliminated.

Fig. 2.8. Absorber development distribution progression.
(100 mW/cm², ASTM air mass 1.5 global spectrum, 25° C)

Figure 2.9. Homogenous vs. graded absorber cell distribution.
(100 mW/cm², ASTM air mass 1.5 global spectrum , 25° C)

Table 2.1. Statistical data for cell efficiency populations
represented in Figure 2.9

	Homogeneous Absorber	Graded Absorber
Mean	8.57	13.76
Standard Deviation	2.79	1.88
Median	9.38	14.10
Sample Count	6139	807

(100 mW/cm², ASTM air mass 1.5 global spectrum , 25° C, 3.3 cm² active area)

The improved average performance attained with graded absorbers also produced several high efficiency cells, with the champion device tested at 16.2% active area efficiency (3.3 cm², V_{oc}=558 mV, J_{sc}=41.0 mA.cm², FF=.708). The I-V curve for this cell is presented in Figure 2.10.

Figure 2.10. Champion graded absorber cell I-V curve.
(100 mW/cm², ASTM air mass 1.5 global spectrum, 25° C)

An improved understanding of the behavior of the absorber and junction in graded absorber devices will be essential in guiding future absorber composition and formation process optimization. Further process optimization through parametric studies will be pursued to continue to improve yield and performance and to develop understanding of the absorber formation reaction pathways and sensitivities. The lessons learned on small areas will be applied to large area processing to meet the objectives and the goals of the contract, leading towards CIS module aperture efficiencies of 12.5%.

SECTION 3.0 DEFECTS

This section summarizes the investigations into substrate-induced defects and the interactions between the substrate and the absorber formation process. The cleanliness and surface condition of the incoming glass substrates can significantly affect the performance and yield of the CIS modules [39]. Phase 2 efforts in this area have been to characterize specific physical defects and correlate them with specific electrical defects, quantify the impact of these defects on module performance, to develop and implement simple diagnostics for evaluating the quality of substrates, and to develop and implement substrate preparation techniques to mitigate the impact of these defects.

3.1 Defect Classification

Much of the focus of Phase 1 of this contract focussed on the classification and determination of the origins of the various defects that give rise to cell and module performance losses. Many of the results of these efforts have been reported elsewhere [16,20,39-41]. There are four primary types of these defects, summarized in Table 3.1.

Table 3.1. Summary of Cell Defect Types.

Defect Type	Affected Area
Particle on the CIS surface suppresses the growth of ZnO	5 μm particle suppresses growth over a 90 μm area
Pinhole in the base electrode propagates through the CIS and the ZnO	6 μm pinhole affects a 200 μm diameter area
Particle at the interface between CIS and the base electrode; no visible defect on the ZnO or CIS	5 μm particle affects a 160 μm diameter area
Scratch in the glass propagates through the Mo, the CIS and the ZnO	0.1 μm scratch affects a 250 μm diameter area

Most of these defects can be seen by the naked eye or under a microscope, and correlate with regions of low photoresponse, represented by the dark areas in the optical beam induced current (OBIC) image shown in Figure 3.1.

A related defect characteristic of monolithically integrated modules that employ an isolation scribe in the base electrode is the poor adhesion in the area near this scribe line. Although the scribe itself is typically only .001"- .003" wide, the affected area

Figure 3.1. OBIC-imaged defects in CIS cells.

can be up as much as .020"-.060" wide. This behavior manifests itself in tape-pull adhesion tests, in which pairs of dark stripes of CIS detach at the CIS-Mo interface on either side of the isolation scribe. In severe cases, the CIS film actually curls up spontaneously from the substrate, causing series, shunt and reliability problems with the interconnect region. A representative tape-pull adhesion test and an optical micrograph of a spontaneously failed base electrode scribe are shown in Figure 3.2.

Figure 3.2. Near-interconnect adhesion failure.

3.2 Impact of Defects

Defects can reduce module output through reduced collection area (such as the lack of transparent conductor), shunting (adhesion failure before or during transparent conductor deposition), and durability (marginal interconnect adhesion). Although prevention of the formation of these defects is the primary thrust of our investigation, most shunting defects can be located and removed from a finished device, with a resultant improvement in device performance. Figure 3.3 shows two I-V curves for the same 60 cm² module before and after such defect microsurgery. For the module in question this resulted in a 9 rel% increase in efficiency. The improvement can be even more dramatic for defect-rich substrates if one has the patience and skill to isolate these defects.

Figure 3.3. Impact of defect repair on modules.

3.3 Defect Diagnostics

Much of the effort in Phase 2 has been to develop diagnostics for evaluating substrates and substrate preparation techniques. One such diagnostic that is extremely powerful is OBIC, but this tool requires fabrication of complete devices, can introduce features that are not substrate-related and is cumbersome.

Annealing Mo-coated substrates in moist air in an oven at 525°C for 10 minutes creates visual images essentially identical to those produced using OBIC. Figure 3.1 is an OBIC image of a cell in which a scratch was made in the glass underneath the base electrode. Evident in both the OBIC image and the air annealed samples are the circular dark spots, many of which exhibit a characteristic concentric "ring" feature. Likewise, in the corresponding scratch in the air-annealed sample and the OBIC near the scratch exhibit the same halo effect along the length of the

scratch.

This imaging technique greatly improves the capability of quickly evaluating various substrates and substrate preparation techniques and has proven to be successful at predicting the behavior of substrates in the fabrication of CIS cells and modules.

3.4 Substrates and Substrate Preparation

The substrate can affect the CIS cells and modules by means of its composition, mechanical properties, surface chemistry, and surface condition. Several groups have begun to study the influence of these various contributors to the behavior of CIS [9,41]. Soda-lime glass is desirable because it is abundant, cheap and reasonably inert. All of the highest efficiency devices reported have been made using soda-lime glass as the substrate material. One of the key objectives of this contract is to achieve the performance milestones utilizing low-cost substrates.

Soda-lime glass can be contrasted with significantly different glasses, such as Corning 7059, to provide some insight as to the opportunities with cheaper glass. Figure 3.4 is an OBIC image of cells made on 7059, in which there are virtually no defect features. Barely visible in this image is a scratch that was made in the substrate (across the left of the picture) that is identical in size to the one imaged in Figure 3.1. Cells made on 7059 glass, however, are typically 20-40% lower in performance, limited by poor voltage.

Figure 3.5 is an SEM image of air-annealed molybdenum-coated soda-lime glass on a scratched substrate. Figure 3.6 is an identical sample on 7059 glass. There are tremendous morphological

Figure 3.4. OBIC image of cells on 7059 substrate.

structural features in the soda-lime glass that are completely absent from the 7059 sample. Figures 3.7 and 3.8 are SEM close-up views of the regions near the scratch for these two substrates.

A number of techniques for substrate preparation, aimed at a low-cost scalable process, are under investigation, including polishing, etching, coating, surface modifiers and wash methods. Substrate samples from various vendors are also being tested. The air annealing technique has greatly improved the ability to screen these samples and techniques and predict the probable occurrence of defects.

In general, substrates that produce few defects in CIS appear defect-free through the air-annealing diagnostic. We are continuing to evaluate the most effective approaches to mitigating substrate-induced defects, and applying these techniques to large-area processing in order to achieve the objectives and goals of this contract.

Figure. 3.5. SEM of air-annealed molybdenum in scratched region on soda-lime glass.

Figure 3.6. SEM of air-annealed molybdenum in scratched region on 7059 glass.

Figure 3.7. SEM Cross-section of air-annealed molybdenum in scribed region on soda-lime glass.

Figure 3.8. SEM cross-section of air-annealed molybdenum in scribed region on 7059 glass.

SECTION 4.0 INTERCONNECTS

This section details the development of alternate strategies for fabricating interconnects and diagnostics implemented for characterizing and quantifying interconnect performance. During Phase 2, a new champion unencapsulated module was produced with 11.7% efficiency for a 60 cm² aperture area 14-cell module.

4.1 Alternate Patterning Strategies

One alternative to solving the near-interconnect adhesion problems for CIS modules is to avoid it. If the interconnect can be formed after the absorber formation process is performed, the problem disappears because there are no patterns. Two such approaches have been demonstrated on CIS modules during Phase 2 [16,20]. Figure 4.1 is a cross-section view of three interconnect strategies for forming a thin film photovoltaic module interconnect.

The Standard interconnect consists of three cuts: an isolation scribe in the base electrode (before absorber formation), an interconnect via through the absorber to the base electrode (before the transparent conductor deposition), and an isolation cut in the transparent conductor (after transparent conductor deposition).

The Post Absorber interconnect consists of three cuts and deposition of a line of insulating material. After the absorber formation process, the entire stack of CIS/Mo is cut with a laser, a line of insulating material (usually a polymer) is applied over the cut to prevent shunting, and the module is completed as in the Standard interconnect: a via is cut through the absorber to the base electrode before the transparent conductor is deposited and an isolation cut in the transparent conductor is made after it is deposited. This approach has the advantage that there are no near-scribe adhesion problems, but has the added complexity of depositing the insulator.

STANDARD INTERCONNECT

POST-ABSORBER INTERCONNECT

POST-DEVICE INTERCONNECT

Figure 4.1. Interconnect cross-sections.

The Post Device interconnect consists of two or three cuts and deposition of two materials: an insulator and a conductor. All patterning steps are performed after the complete device stack is finished. The entire ZnO/CIS/Mo stack is cut with a laser, a via landing/ZnO isolation scribe is performed adjacent to the cut, an insulating material is deposited over the base electrode cut to avoid shunting, and finally a conductive material is deposited over the insulator to connect the transparent conductor of one cell to the base electrode of the next. This approach has the advantage of postponing all patterning handling steps until after all sensitive deposition steps are completed, but has the added complexity of deposition of two extra materials, an insulator and a conductor.

4.2 Unencapsulated Module Results

These techniques have been successfully applied to CIS modules. The best unencapsulated module results utilizing these strategies are shown in Figure 4.2. We are continuing to refine these techniques and materials to scale to larger areas and to verify the durability of the interconnects.

Figure 4.2. Champion module performance for alternate interconnects. (100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C)

4.3 Interconnect Diagnostics

A single very high resistance interconnect can render an entire module unusable; a single open interconnect would prevent any current flow. Control of process parameters such as cutting speed, tip pressure and laser settings is straightforward, but the interconnect via contact resistance is difficult to control because there is no direct feedback measurement tool. Two techniques for evaluating interconnects have been developed and are detailed in this section. The first is a method for quantifying series resistance effects in finished modules, called "dark forward bias voltage mapping", and the second is an alternate structure that can be fabricated to evaluate interconnect performance even through environmental testing in an encapsulated package, called an "interconnect test structure".

4.3.1 Dark Forward Bias

A brief review of this technique was reported during Phase 1 [15,42], but the value and further refinements of the technique warrant further review. A single very high interconnect resistance can render an entire module unusable (taken in the upper limit, a single open interconnect would prevent any current flow). Control of the process parameters such as cutting speed, tip pressure and laser settings is straightforward, but the interconnect via contact resistance is difficult to control with a direct feedback diagnostic because the contact is not made until a later stage in the process. To evaluate the interconnect series resistance, this simple non-destructive diagnostic for modules was developed for initial setup and periodic process qualification. The apparatus is illustrated schematically in Figure 4.3, which employs a power supply and a voltmeter. The power supply is used to flow current through the module circuit in the dark in the forward bias direction near the one-sun short circuit current value. The voltmeter is then used to measure voltage drop from cell to cell. This voltage should be roughly equivalent to the one-sun open-circuit voltage of each cell. Higher values indicate high series resistance. A section of a module that appeared to have a blocking junction (negative curvature in the I-V curve near V_{oc}) (Figure 4.4) was analyzed using this technique, and it was found that the poor fill factor was being caused by several high-resistance interconnects (Figure 4.5). Eliminating these high resistance interconnects greatly improves average module performance.

Figure 4.3. Dark forward bias interconnect diagnostic apparatus.

Figure 4.4. I-V curve of low FF module slice.

Figure 4.5. Dark forward bias voltage data for module in Fig. 4.4.

4.3.2 Interconnect Test Structures

To evaluate interconnect performance independent of cell material effects, and to evaluate the effectiveness of the various components of the alternate interconnect strategies, a number of "interconnect test structures" were developed. These are essentially module plates with double back-to-back interconnects along the current path length of the module, illustrated in Figure 4.6. The structure can then be measured for resistance changes either from one end to the other (through a number of interconnects) or individually. The structure can also be laminated and subjected to environmental testing to evaluate the durability of various interconnects and interconnect materials. Cross-sectional views of the various interconnect test structures that can be used for evaluating the new alternate interconnects are illustrated in Figure 4.7.

Figure 4.6. Standard interconnect test structure.

Mo Contact Test Structure
Measure interface contact resistance (R_{contact}) between conductor and Mo.
Goal: $R_{\text{contact}} < 1 \text{ m}\Omega\text{-cm}^2$

Isolation Test Structure
Measure both cell voltages and cell isolation before and after conductor.

ZnO Contact Test Structure
Measure interface contact resistance (R_{contact}) between conductor and ZnO.
Goal: $R_{\text{contact}} < 1 \text{ m}\Omega\text{-cm}^2$

Figure 4.7. Alternate interconnect test structures.

4.4 Module Durability

Graded absorber materials appear stable through lamination heat and pressure cycles. Figure 4.8 is a distribution plot of the change in performance for 851 cells, split into two groups and subjected to the lamination thermal cycle and thermal+pressure cycle, using mylar as a protective layer to enable retesting of the devices. No statistically significant change in cell performance was noted. Stability data for alternate interconnect modules are not yet available. Demonstration of stable performance of encapsulated module is a key thrust of Phase 3 in order to achieve the objectives and goals of the program.

Figure 4.8. Device performance through lamination cycle.

A topic related to the evaluation of module stability is the peculiar behavior of CIS materials upon exposure to sunlight: many of them improve significantly when exposed to light, and generally better cells exhibit less relative improvement. This phenomena has been observed by several groups [43-45]. As shown in Figure 4.9, there are two basic populations of low-performing cells. The first group shows a monotonic relationship of greater

Figure 4.9. Light soaking effects.

relative improvement on sunsoaking with lower initial performance; the performance of these cells appears to be dominated by absorber/junction behavior. The second exhibits no effect whatsoever; the performance of these cells is dominated by physical defects. The effects are reversible; improvements that are seen in a few minutes disappear over a 24-48 hour period in SSI devices.

The fundamental mechanism for this behavior may hold the key to greatly improved performance of CIS cells and modules. This behavior also points out the extreme caution that must be exercised when attributing changes in performance with environmental testing, etc., in that the testing methodology must correct for these effects.

In addition to NREL's outdoor exposure testing of CIS modules, SSI has continued to monitor a number of CIS modules subjected to outdoor exposure at the Camarillo, California site. Figure 4.10 illustrates the behavior of these modules. Many modules show the same stable behavior as those monitored at NREL, but some do exhibit a loss in performance which is attributed to the interconnect reliability issues highlighted in this section. A major thrust of Phase 3 is to demonstrate stability of the high-performance CIS modules.

Figure 4.10. SSI outdoor module performance summary.
(100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C)

SECTION 5.0 MODULE DELIVERABLES

The primary objective of this subcontract is to demonstrate 12.5% aperture efficient, large area (3900 cm²) encapsulated thin film CuInSe₂ (CIS) modules as part of 3-phase cost shared contract which began on May 1, 1991. To chart the research progress, the milestones defined in the contract are summarized in Table 5.1 below.

Table 5.1. Contract Deliverables.

Milestone	Date	Deliverable
Phase 1 M1	7/31/91	4 encapsulated CIS modules (1 ft ²) for reliability testing at NREL.
M2	4/30/92	An encapsulated 36.5W, 9.4% efficient (aperture area) CIS module.
Phase 2 M3	6/30/92	4 encapsulated CIS modules (1-4 ft ²) for reliability testing at NREL.
M4	6/30/92	An encapsulated 38.8W, 10% efficient (aperture area) CIS module.
Phase 3 M5	12/31/93	An encapsulated 44.6W, 11.5% efficient (aperture area) CIS module.
M6	12/31/93	4 encapsulated CIS modules (1-4 ft ²) for reliability testing at NREL.
M7	1/31/95	An encapsulated 48.5W, 12.5% efficient (aperture area) CIS module.

5.1 CIS Encapsulated Module Deliverables

Four CIS modules were shipped to NREL to meet the M3 deliverable. One module (#483-11) broke and was replaced with #308-05. The performance parameters for these modules are summarized in Table 5.2. The power outputs are in the 31-36 watt range. The CIS circuits are laminated behind tempered glass. Framing and termination are achieved using an extruded aluminum frame and plastic junction box (except #308-05, which utilizes a reaction injection molded frame and a two-conductor cable). M4 deliverable requirements were met with the earlier M2 deliverable module #182-5

of 37.7 watts (within 3% of the 38.8 watt milestone, I-V curve shown in Figure 5.1). Furthermore, champion cell performance improved to 16.2% on 3.3 cm² active area test devices. Champion large area unencasulated module performance remains at 10.5 W for 938 cm² and 40.8 W for 0.4 m². I-V curves for these modules are shown in Figure 5.2.

Table 5.2. Parameters for CIS modules delivered to NREL.

Module #	P _{max} (W)	I _{sc} (A)	V _{oc} (V)	FF
483-11*	37.1	2.45	24.4	.621
482-11	35.8	2.45	23.4	.624
482-8	35.4	2.49	23.5	.606
482-9	35.0	2.47	23.4	.607
308-05*	31.5	2.31	22.8	.570

(100 mW/cm², ASTM air mass 1.5 global spectrum, 25°C)

Figure 5.1. I-V curve for module 182-5.
(100 mW/cm², ASTM air mass 1.5 global spectrum, 25°C)

Figure 5.2. I-V curves for champion large area unencapsulated modules. (100 mW/cm², ASTM air mass 1.5 global spectrum, 25°C)

5.2 CIS Module Measurement Comparison between NREL and SSI

Measurement of performance for large area CIS modules has been excellent between NREL and SSI LAPSS testing equipment. Measurements are presented for comparison for module #182-5 (M2 and M4 deliverable) in Table 5.3. The NREL LAPSS data compares very closely with the SSI data (within .5% of power measurement). J_{sc} data agrees within 1.6%.

Table 5.3 SSI and NREL data comparison for module 182-5.

	Power (W)	Eff (%)	I_{sc} (A)	V_{oc} (V)	FF
SSI R&D LAPSS (Before)	38.1	9.8	2.51	24.3	0.626
SSI R&D LAPSS (After)	37.5	9.7	2.48	24.3	0.624
NREL Spire 240	36.2	9.3	2.31	24.2	0.647
NREL LAPSS	37.7	9.7	2.44	24.0	0.644
NREL LAPSS/SSI Ratio (%)	100.5	100.5	98.4	98.8	103.2

Notes:

1. Efficiency based on 3883 cm² (30.6 x 126.9 cm) aperture area.
2. NREL Spire data has 0.975 spectral mismatch correction. NREL LAPSS was calibrated from the NREL X25 using a CIS minimodule.

5.3 Additional Interactions

In addition to scheduled deliverables, thirty-six prototype 1'x4' RIM-framed CIS modules were delivered to NREL for the installation of a one kilowatt array at NREL's outdoor test site. The array will consist of 34 installed modules in a low-voltage system, with two additional modules: one for a control and one for a spare.

SECTION 6.0 CONCLUSIONS

The most critical issues determining module yield losses have been identified and can be grouped into three major categories.

1. The uniformity and reproducibility of the absorber formation process dominates the fundamental performance of the material over a large area.
2. The interaction of the substrate with the films requires appropriate selection criteria and preparation techniques for minimizing defects that lead to shunting and areas of poor photoresponse.
3. Performance losses near interconnects reduce module performance and can cause inadequate performance through module durability testing.

Through the adoption and further refinement of a graded absorber formation process in which the surface layer of CIS incorporates sulfur, combined with the appropriately prepared substrate, mean efficiency for 3.3 cm² test devices was improved from 9% to 14%, with the best cell efficiency of 16.2%. Perhaps more significant is that the occurrence of cells below 10% efficiency has been essentially eliminated.

Alternate techniques for fabricating interconnects after the absorber formation process were developed during Phase 2. These approaches employ the application of insulating and/or conducting materials (typically polymer-based) to form the module interconnect. This approach has produced a module with 11.7% aperture area efficiency, which is an SSI record for a CIS integrated module and represents significant progress toward meeting the efficiency target for the M5 deliverable (11.5% aperture efficiency for an encapsulated 3900 cm² aperture area module).

In addition to scheduled deliverables, thirty-six prototype 1'x4' RIM-framed CIS modules were delivered to NREL for the installation of a one kilowatt array at NREL's outdoor test site. SSI and NREL have also continued to monitor the outdoor performance of CIS prototype modules, demonstrating inherent stability of the material for more than five years.

Progress at SSI in Phase 2 and CIS performance results to date demonstrate the potential for CIS-based materials to meet the DOE technology goals. Efforts in Phase 3 will continue to address understanding of the mechanisms which control CIS module performance and to define and implement improvements in module design and processing leading towards CIS module aperture efficiencies of 12.5%.

SECTION 7.0 FUTURE PLANS

The current focus of the group is to continue to develop techniques capable of meeting remaining contract deliverables by applying lessons learned in Phase 1 and Phase 2 to large area substrates. Key issue of concern are absorber uniformity and process reproducibility, alternate patterning approaches, glass specification, preparation, handling, and coatings, and evaluation of stability. Collaboration with national laboratories and universities will continue to grow to maximize the synergistic benefits of these interactions.

The performance milestones and deliverables for Phase 3 are not expected to change. Efforts will continue to address understanding of the mechanisms that control CIS module performance, defining improvements in module design and processing leading to aperture efficiencies of 12.5%.

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45. D. Willett, "Investigation of Lamination Induced Metastability in CIS-Based Modules", *Photovoltaic Perf. Rel. Workshop*, Sep 1993.

APPENDIX A

LIST OF PRESENTED PAPERS

- [1] "Recent Progress in Thin Film CuInSe₂ Modules", D. Pier, W. Chesarek, M. Dietrich, S. Kuriyagawa, R. Gay, 11th European PV Solar Energy Conference, 1992, pp. 107-111.
- [2] "I-III-VI₂ Multinary Solar Cells Based on CuInSe₂", J. Ermer, D. Tarrant, 23rd IEEE PVSC, 1993, pp. 372-378.
- [3] "Results of Recent Thin Film CuInSe₂ Module Investigations", C. Fredric, D. Willett, D. Tarrant, R. Gay, 23rd IEEE PVSC, 1993, pp. 437-440.
- [4] "The Effects of Sweep Rate, Voltage Bias and Light Soaking on the Measurement of CIS-Based Solar Cell Characteristics", D. Willett, S. Kuriyagawa, 23rd IEEE PVSC, 1993, pp. 495-500.
- [5] "The Role of Gallium in CuInSe₂ Solar Cells Fabricated by a Two-Stage Method", C. Jensen, D. Tarrant, J. Ermer, G. Pollock, 23rd IEEE PVSC, 1993, pp. 577-580.
- [6] "Manufacturing of Low-Cost High-Efficiency Thin-Film CuInSe₂ Photovoltaic Modules", K. Knapp, C. Eberspacher, D. Tarrant, G. Pollock, 23rd IEEE PVSC, 1993, pp. 1073-1077.
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OTHER PRESENTATIONS

- [8] D. Willett, "Investigation of Lamination Induced Metastability in CIS-Based Modules", Photovoltaic Perf. Rel. Workshop, Sep 1993.

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15. Supplementary Notes NREL technical monitor: H. S. Ullal			
16. Abstract (Limit: 200 words) This report describes work to demonstrate 12.5% aperture efficient, large-area (3900-cm ²) encapsulated thin-film CuInSe ₂ (CIS) photovoltaic modules. The module design consists of 53 series-connected ZnO/CdS/CIS/Mo/glass cells fabricated on a 4141-cm ² (128.6 x 32.2 cm) glass substrate with a nominal aperture area of 3895 cm ² (127.3 x 30.6 cm). Four CIS modules were shipped to NREL under the terms of the subcontract. Phase 2 consisted of fabricating large-area (3900-cm ²) modules for high-performance module processing. The large-area parts proved to be cumbersome, and we decided to use smaller substrates (100 cm ²) to accelerate the progress in solving the types of technical challenges that were discovered in processing large-area parts, and then to apply these solutions to larger areas to meet the objectives of the investigation. The most critical issues determining module yield losses can be grouped into three major categories: (1) the uniformity and reproducibility of the absorber formation process dominates the fundamental performance of the material over a large area, (2) the interaction of the substrate with the films requires appropriate selection criterion and preparation techniques for minimizing defects that lead to shunting and areas of poor photoresponse, and (3) performance losses near interconnects reduce module performance and can cause inadequate performance through module durability testing.			
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