Research on High Efficiency, Large-Area CuInSe₂-Based Thin-Film Modules

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EXECUTIVE SUMMARY

Siemens Solar Industries (SSI) began a 3-year, 3-phase cost shared contract on May 1, 1991 with the objective to demonstrate 12.5% aperture efficient, large area (3900 cm²) encapsulated thin film CuInSe₂ (CIS) modules. During the first year (Phase 1), SSI met all performance milestones and program deliverables. A new world record of 37.7W and 9.7% aperture efficiency for a 3883 cm² (126.9 x 30.6 cm) encapsulated CIS module was demonstrated and verified at NREL. Unencapsulated CIS module plate performance achieved 40.8 W and 10.5% aperture efficiency. Excellent measurement agreement was verified between SSI and NREL.

The module design consists of 53 series-connected ZnO/CdS/CIS/Mo/glass cells fabricated on a 4141 cm² (128.6 x 32.2 cm) glass substrate with a nominal aperture area of 3895 cm² (127.3 x 30.6 cm). Prior to the contract, SSI demonstrated a 14.1% active-area efficient, 3.4 cm² ZnO/thin CdS/CIS/Mo/glass cell and fabricated monolithic integrated modules₂ with unencapsulated aperture efficiencies of 11.2% on 940 cm² and 9.1% on 3900 cm². The best encapsulated large area CIS module power output prior to the contract was 33.7 W, 8.7% aperture efficiency (verified at NREL) over a 3883 cm² aperture area.

Five CIS modules were shipped to NREL to meet the Phase 1 deliverables. Table 1 summarizes their photovoltaic parameters. The best module measured 37.7 watts (9.7% aperture efficiency) at NREL. The remaining four CIS modules were in the 30-31 watt range. The CIS circuits are laminated behind tempered glass and framed using a reaction injection mold (RIM) process. Electrical connection is provided by a two-conductor cable.

Table 1. Parameters for CIS modules delivered to NREL

Module #	P _{max} (W)	I _{sc} (A)	V _{oc} (V)	FF
182-5	37.7	2.44	24.0	0.644
282-5	31.0	2.42	22.7	0.563
324-4	30.9	2.38	22.4	0.580
324-6	30.0	2.38	22.0	0.575
324-16	29.8	2.40	21.9	0.566

Module performance strongly depends on the spatial uniformity of cell and interconnect performance, which in turn depend on the properties of the constituent layers. Initial contract emphasis was on module diagnostics using improved techniques to characterize the cells and interconnects. V_{oc} maps provide information on the

junction quality. Resistance losses due to individual interconnects or ZnO sheet resistance can be determined by mapping the cell voltage drops at a fixed forward bias current. In addition, individual cell I-V curves can be evaluated by measuring the dependence of the voltage drop of each cell on the applied module current. The physical nature of the defects is then correlated using optical beam induced current (OBIC), electron beam induced current (EBIC), scanning electron microscopy (SEM), and other techniques such as tape adhesion testing.

A comparison between V_{oc} maps for a 39W (10.0% efficient) and a 32W (8.2% efficient) module plate shows the voltage is very uniform for the higher power module. In contrast, the cell voltages for the lower power module are both suppressed overall and non-uniform. OBIC studies indicate that the reduced V_{oc} cells have localized areas of low response. One source of low response identified by SEM and EBIC is areas of abnormal ZnO growth associated with "dust" contamination of the surface before the ZnO. Other areas do not correlate with surface features but have reduced adhesion between the CIS and Mo. Interconnect problems can substantially reduce the module fill factor (FF). The low module FF (0.53) of the 32W module results from the poor FF of individual module slices. Comparison of the V_{oc} and forward bias maps show the junctions are fairly uniform but some cells have high voltage drops associated with poor quality interconnects. Research is focusing on improved materials and processing quality.

Table 2 below, a summary of the best SSI CIS performance results to date, demonstrates the potential for CIS meeting the DOE technology goals. Efforts in Phase 2 will continue to address understanding of the mechanisms which control CIS module performance, defining improvements in module design and processing leading towards CIS module aperture efficiencies of 12.5%.

Table 2. SSI CIS Performance Achievements

	Power (W)	Area (cm ²)	Eff (%)	I_{sc} (mA)	J_{sc} (mA/cm ²)	V_{oc} (V)	FF
Test Structure	-	3.5	14.1	-	41.0	0.50 8	0.68
1x1 ft module plate	10.5	938	11.2	641	39.3	25.5	0.64
1x4 ft module plate	40.8	3890	10.5	2550	37.0	24.5	0.65
1x4 ft module	37.7	3883	9.7	2440	35.5	24.0	0.64

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SECTION 1.0 INTRODUCTION

CuInSe_2 (CIS) is a promising material for high-power, low-cost photovoltaics (PV), both as a stand-alone single junction and as the narrow bandgap component of a tandem junction [1-3]. Fig. 1.1 compares the photon currents generated in CIS, CdTe, thin film silicon:hydrogen alloys (TFS), and crystalline Si calculated from the optical absorption coefficients and assuming no reflection losses [4-7]. The photon current increases as a function of optical path length (that is, absorber layer thickness), and J_{max} is the maximum available photon current density for the material. For CIS with an energy band-gap of about 0.95 eV, 90 percent of the photons are absorbed in a thickness of less than 1 μm , so that CIS films 1-3 μm thick are sufficient for thin film PV applications.

Fig. 1.1. Photon current versus optical path length for various semiconductors (100 mW/cm² ASTM 1.5 global spectrum).

Presently CIS device efficiencies approach 15% active area efficiency with the potential of reaching 20% efficiency [4]. CIS modules are typically fabricated on soda-lime glass substrates, one of the lowest cost PV substrate materials available today. Thus, CIS has the potential to address the Department of Energy (DOE) Five Year Plan polycrystalline thin-film milestones, namely the fabrication of stable modules with efficiencies of 15% (150 W/m²) or more made by scalable, low-cost techniques on inexpensive substrates.

1.1 Module Design

The module design, illustrated in Fig. 1.2, consists of 53 series-connected ZnO/CdS/CIS/Mo/glass cells fabricated on a 4141 cm² (128.6 x 32.2 cm) glass substrate with a nominal aperture area of 3895 cm² (127.3 x 30.6 cm). The module interconnect region is portrayed in the expanded cross section.

Fig. 1.2. Basic design of 0.4 m² CIS module. The details of the integrated interconnect are shown in the inset.

The cell spacing is 0.557 cm (227 mils). The Mo isolation scribe, 0.7 mils wide, is cut with a 1.06 micron wavelength Nd-YAG laser. The ZnO/Mo interconnect is made through a 2.4 mil wide via created in the CIS. This via is made using either laser or mechanical scribing techniques. The nominal contact resistance is in the range of 0.2-0.5 milliohm-cm². The ZnO/ZnO isolation scribe is also performed by either mechanical or laser scribing.

1.2 Background

Siemens Solar Industries (SSI), formerly ARCO Solar, has pursued the research and development of CuInSe_2 (CIS) thin film PV technology since 1979. Prior to the contract, SSI demonstrated a 14.1% active-area efficient, 3.4 cm^2 $\text{ZnO}/\text{thin CdS}/\text{CIS}/\text{Mo}/\text{glass}$ cell and fabricated monolithic integrated modules with unencapsulated aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2 as noted in Table 1.1 [5]. As with all PV technologies, encapsulation is required in order to protect the electrical circuit from environmental exposure. The best encapsulated large area CIS module power output prior to the contract was 33.7 W, 8.7% aperture efficiency (verified at NREL) over a 3883 cm^2 aperture area [6]. Table 1.2 shows the impact of lamination and framing on CIS module performance, primarily through the additional optical reflection loss of the front tempered glass encapsulant. Outdoor testing of SSI CIS modules at NREL over a period of more than three years implies excellent intrinsic module stability [7]. Prior CIS research at SSI is also presented in NREL reports from a contract developing tandem cells using CIS as the bottom junction [8, 9].

Table 1.1. CIS module plate performance at the beginning of the contract.

Module	Measurements		Predictions
	1x1 ft (55 cells)	1x4 ft (53 cells)	1x4 ft (53 cells)
Area ** (cm^2)	938	3916	3916
V_{oc}/cell (mV)	464	443	508
J_{sc} (mA/cm^2)	39.3	37.0	41.0
V_{oc} (V)	25.5	23.5	26.9
I_{sc} (A)	0.641	2.54	2.87
FF	0.639	0.598	0.672
Eff ** (%)	11.2	9.1	13.3
Power (W)	10.5	35.8	51.9
* 100 mW/cm^2 ASTM air mass 1.5 global spectrum, 25 C			
** Aperture area			

Table 1.2. Impact of lamination and framing on module performance.

1x4 ft 53 cells	Area* (cm ²)	I _{sc} (A)	V _{oc} (V)	FF	P _{max} (W)	Eff* (%)
Unlaminated Module	3916	2.54	23.5	0.598	35.8	9.1
Framed & Laminated Module	3883	2.43	23.6	0.589	33.7	8.7
Change	-1%	-4%	0%	-2%	-6%	-5%
* Aperture area						

1.3 Objectives

The objectives of this research effort are to achieve the polycrystalline thin-film milestones of the DOE Five Year Plan, that is, the fabrication of stable encapsulated modules with 15% efficiencies made by scalable, low-cost techniques on inexpensive substrates. SSI as noted above has previously demonstrated encapsulated, 33.7 W, 8.7% aperture efficient CIS modules. All of the requisite facilities, equipment and personnel exist. The purpose of this program is to build upon that foundation, to address identified processing difficulties and to improve materials and device quality over the large areas to achieve the above objectives. The contract performance milestones for encapsulated CIS modules are summarized in Table 1.3.

Table 1.3. CIS module performance milestones

Parameter	Start	16 month	27 month	36 month
I _{sc} (A)	2.43	2.57	2.71	2.78
J _{sc} (mA/cm ²)	35.7	37.0	39.0	40.0
V _{oc} (V)	23.6	24.4	25.3	26.5
V _{oc} /cell (mV)	445	460	478	500
FF	0.59	0.62	0.65	0.66
P _{max} (W)	33.7	38.8	44.6	48.5
Eff (%)	8.7	10.0	11.5	12.5

Based upon an encapsulated 53-cell, 3883 cm² aperture area module.

1.4 Discussion

In Phase 1, the first year of a 3-year effort, emphasis has been on establishing the baseline CIS module fabrication processes including detailed characterization of the cells and interconnects. Section 2 describes the results of analysis from a number of improved module diagnostic techniques. Section 3 summarizes several experimental studies, with special emphasis on glass substrate quality and cleaning. The module deliverables are detailed in Section 4. Section 5 presents the conclusions for this first phase while Section 6 describes future plans. Finally, papers presented during Phase 1 are included in Appendix A.

SECTION 2 MODULE DIAGNOSTICS

Improvements in CIS module performance depend critically on the characterization of the material and device properties to guide the research efforts. During Phase 1, several techniques have been implemented or upgraded in order to evaluate the large area (0.4 m²) CIS modules. The following provides a partial list of these analytic techniques:

Light and Dark Current-Voltage

Spectral Response

Open-Circuit Voltage Mapping

- * Forward Bias Voltage Mapping
- * J₀ and Diode Factor Mapping of each Module Cell
- * Interconnect and Sheet Resistance Measurements

Optical Transmission/Reflection/Absorption

Optical Microscopy

Optical Beam Induced Current (OBIC) Analysis

Scanning Electron Microscope (SEM) Imaging

Electron Beam Induced Current (EBIC) Analysis

Auger Surface Analysis and Depth Profiling

- * Atomic Force Microscope (AFM) Imaging
- * Fog Box Imaging

Adhesion Tape Pull Test

* Implemented or upgraded during contract.

This section describes the application of these techniques to the characterization of the CIS modules. The module design has been described in Section 1.1 and illustrated in Fig. 1.2. Module performance depends on the spatial uniformity of cell and interconnect performance, which in turn depends on the properties of the constituent layers. Initial contract emphasis has been on module diagnostics using improved techniques to characterize the cells and interconnects.

2.1 Voltage Mapping

V_{oc} maps, where the module is cut into 10 cm wide strips and the voltages of the 53-cell strips are mapped, provide information on the junction quality. Resistance losses due to individual interconnects or ZnO sheet resistance can be determined by mapping the cell voltage drops at a fixed forward bias current. In addition, individual cell I-V curves can be evaluated by measuring the dependence of the voltage drop of each cell on the applied module current. The physical nature of the defects is then correlated using optical beam induced current (OBIC), electron beam induced current (EBIC), scanning electron microscopy (SEM), and other techniques such as tape adhesion testing.

The V_{oc} maps for a 39W (10.0% efficient) and a 32W (8.2% efficient) module are compared in Fig. 2.1. The voltage is very uniform for the higher power module. In contrast, the cell voltages for the lower power module are both suppressed overall and non-uniform. OBIC studies indicate that the reduced V_{oc} cells have localized areas of low response. One source of low response identified by SEM and EBIC are areas of abnormal ZnO growth associated with "dust" contamination of the surface before the ZnO. Other areas do not correlate with surface features but have reduced adhesion between the CIS and Mo. Interconnect problems can substantially reduce the module fill factor (FF) as evidenced in Fig. 2.2. The 0.53 module FF (Fig. 2.2) results from the poor FF of individual module slices (see Fig. 2.3). Comparison of the V_{oc} and forward bias maps in Fig. 2.4 show the junctions are fairly uniform but some cells have high voltage drops associated with poor quality interconnects.

Fig. 2.1. V_{oc} maps comparing higher and lower power CIS modules.

Fig. 2.2. I-V curve of an unencapsulated 0.4 m^2 CIS module.

Fig. 2.3. I-V curve of one slice of the module of Fig. 2.2.

Fig. 2.4. V_{oc} and dark forward bias voltage measurements of the slice of Fig. 2.3.

An extension of the above voltage mapping techniques is the determination of the individual light and dark cell I-V curves by incrementing the current through the module and measuring the voltages across each of the 53 cells. Fig. 2.5, the 1-sun I-V curve for a module slice which has a low fill factor, has an average cell V_{oc} of 422 mV. Fig. 2.6, the V_{oc} map, indicates a 10% variation in cell V_{oc} 's with lower values for cells 4 through 18 with an average cell V_{oc} of 395 mV. Since the lower illumination for V_{oc} mapping (about 0.6 suns) results in a 25 mV drop in the measured V_{oc} , the average V_{oc} is consistent with that measured at 1-sun. The V_{oc} variations may be caused by localized microshunts due to dust or other contamination or to variations in the CIS stoichiometry.

To determine if the cell V_{oc} 's are consistent with the dark diode behavior, the individual cell I-V curves were extracted by the technique described above and the cell J_0 's and diode factors calculated (Fig. 2.7). From these values, the 1-sun cell V_{oc} 's are calculated (Fig. 2.8). The shape of Fig. 2.8 agrees very well with the shape of Fig. 2.6, demonstrating that the V_{oc} correlates with the cell junction quality.

2.2 Defect Characterization

Optical beam induced current (OBIC), electron beam induced current (EBIC), scanning electron microscope (SEM) imaging, Auger spectroscopy, and adhesion tape pull tests are the primary techniques used to compare cells with different V_{oc} 's and determine the physical nature of the defects.

SEM and EBIC imaging of two different CIS cells (#13 with low V_{oc} and #46 with higher V_{oc} from module slice # 304-8-4) are described in this section. The adhesion test of the module slices was evaluated using a 25 oz/in. tape. As shown in Fig. 2.9, the CIS pulls away within the interconnect region. Most cleavage occurs at the CIS/Mo interface, but along the borders of the cleavage region, separation at the ZnO/CIS interface is also evident. A Mo berm three times the thickness of the Mo layer is immediately adjacent to the laser pattern 1 (Mo isolation scribe) accompanied by a "splatter zone" of resolidified molten Mo 70 to 100 microns wide.

For cell 13 (low V_{oc}), Fig. 2.10 illustrates some features which result in low EBIC response, namely several sites of abnormal ZnO growth associated with "dust" contamination of the surface before the ZnO. Also shown is a very high EBIC response area which correlates with a hole in the ZnO where a ZnO growth defect has broken off, exposing the CIS junction. Cell 46 (high V_{oc}) has fewer ZnO growth defects as shown in Fig. 2.11, but patches of low EBIC response are evident in Fig. 2.11b (the dark areas have 80% of the response of the bright areas). These reduced response areas may correlate with stress in the films or variations in the Cu/In ratio.

Fig. 2.5. I-V curve for low FF module slice (#304-8-4)

Fig. 2.6. V_{oc} map of module slice #304-8-4.

Fig. 2.7. J_0 map (dark I-V fit) for module slice #304-8-4.

Fig. 2.8. Calculated V_{oc} map for module slice #304-8-4.

(a) Cell 13 interconnect after tape test.

(b) High magnification image of selected area of (a).

Fig. 2.9. SEM images of Cell 13 interconnect after tape test.

(a) SEM image.

(b) EBIC image.

Fig. 2.10. Images of a selected top surface area of Cell 13.

(a) SEM image.

(b) EBIC image.

Fig. 2.11. Images of a selected top surface area of Cell 46.

The quality of the incoming glass substrates is another source and promoter of defects in the CIS module. Since photovoltaics presently represents a small market for the glass manufacturers, we are subject to variations in glass quality which are not significant for their primary customers but which impact the quality of our PV product. This requires us to presently tune our cleaning process to the nature of glass contamination from a particular vendor. Fig. 2.12 illustrates how small cracks in the incoming glass surface can lead to abnormal growth of the Mo layer, stress build-up in the Mo layer and subsequent loss of adhesion. We have also found the need to sort the incoming glass on the basis of flatness which effects the uniform heating of the substrate during film deposition. In Section 3, studies investigating the impact of glass cleaning strategies on CIS performance are presented.

2.3 Thin Film CIS and CdS Characterization

Scanning electron microscopy (SEM) and atomic force microscopy (AFM) have been used to evaluate the structure of the CIS layer and subsequent CdS layer. Figs. 2.13a and 2.13b show the general morphology of the CIS surface, indicating a distribution of grain size and some porosity in the film surface. Small nodules of about 0.5 μm size are fused to the surfaces of the underlaying film which has several micron grain size. Fig. 2.14a and 2.14b, AFM images, illustrate the surface features of a CIS grain with and without CdS. The CIS grain surface is featureless on the 500 nm scale before CdS deposition. After CdS, grain structure is evident on the order of 500Å in size.

(a) Side View.

(b) Top View.

Fig. 2.12. SEM images of Mo growth effected by a microcrack in the glass substrate.

(a) Typical CIS surface.

(b) Enlarged image of features in (a).

Fig. 2.13. SEM images of the CIS surface morphology.

Fig. 2.14. AFM images of CIS grain surfaces with and without the CdS layer.

SECTION 3 EXPERIMENTAL STUDIES

This section summarizes several experimental studies that were carried out to correlate large area CIS module performance to the glass substrate properties and to module processing. During Phase 1, several unencapsulated CIS module plates achieved output powers above 40 watts with the best equal 40.8 watts or 10.5% aperture efficiency.

3.1 Glass Substrate Studies

During Phase 1, it became apparent that examination of the incoming glass cleanliness and correlation to defects in the subsequent thin film layers was necessary. The cleanliness (or rather, the lack thereof) of the incoming glass substrates can substantially compromise the performance and yield of the CIS modules.

A new apparatus called a "Fog Box" was fabricated in order to image contamination and other defects on the glass surfaces. The box which supports a 1x4 ft glass plate provides a source of water vapor which condenses on the glass in patterns which highlight the contamination and other features. Findings include:

- 1) As received glass has a number of different patterns of surface contamination associated with it (that vary part-to-part, side-to-side, batch-to-batch). These include glove marks, edge marks and at least two different types of "track" marks (one associated with the vendor's glass handling machine; and another with vendor applied coatings);
- 2) The current glass washing procedures do not remove all of the contamination patterns observed on as-received glass;
- 3) The Siemens Solar glass washer can leave its own set of contamination marks on the glass surface. The patterns are typically identified by their periodic spacing consistent with the wash roller circumference and their orientation relative to the glass edge. The glass washer was rebuilt including new rollers and bearings from the vendor.
- 4) Some patterns of device performance across a module plate correlate with the patterns seen with the "Fog Box";
- 5) Some glass batches have what appears to be oils present around the edges. This was traced back to solvents used during glass cutting by the glass manufacturer to give "clean" cuts.

Fig. 3.1 shows the SEM images of a circular defect in a CIS module. The low magnification image (Fig. 3.1a) shows that the defect influences the surrounding film morphology several hundred micrometers away. At the high magnification (Fig. 3.1b), a crack

(a) Low magnification SEM image.

(b) Enlarged SEM image of defect feature in (a).

Fig. 3.1. SEM image of a defect feature in a CIS module.

is evident in the center of the defect which is associated with a crack in the glass. Figs. 3.2a images a depression in the surface of the ZnO window layer. As shown in Fig. 3.2b, subsequent chemical removal of the ZnO, CIS and Mo layers identify the cause to be a linear crack in the underlying glass substrate. In other studies, optical beam induced current (OBIC) measurements of CIS modules reveal large (500 μm) shunt defects are caused by CIS adhesion failure in a relatively small (30 μm) region around very small (approximately 1 μm) scratches in the glass substrates.

Two parallel strategies were initiated during Phase 1. One was to implement more aggressive substrate preparation/glass cleaning procedures which would reduce our susceptibility to the quality of the as-received glass surfaces. The second was to re-evaluate glass from different vendors in order to review which vendors can deliver consistent quality to produce high performance CIS modules with a good yield. Both strategies are necessary.

3.1.1 CeO_2 Glass Polishing

CeO_2 polishing is one approach to removal of incoming glass contamination. The following table compares the PV module parameters between unpolished and CeO_2 polished glass (5 min electric polisher with CeO_2 powder + DI H_2O):

	P_{max} (W)	V_{oc} (V)	I_{sc} (A)	FF
Not Polished	35.90	23.00	2.53	0.62
	35.40	23.00	2.51	0.61
	34.60	22.60	2.52	0.61
	33.80	22.30	2.53	0.60
	Average 34.93	22.73	2.52	0.61
Polished	37.70	23.70	2.52	0.63
	36.40	23.40	2.52	0.62
	35.60	23.00	2.52	0.62
	35.60	23.20	2.54	0.60
	35.60	23.00	2.51	0.62
Average	36.16	23.26	2.52	0.62

An average module power increase of 1.2W resulted from the polishing due to an improvement in V_{oc} and fill factor. Diagnostics of the module plates indicate that the CeO_2 reduces the number of defects and improves the film uniformities across the module plate. Although the CeO_2 polished glass substrates were found to have a lower density of the large shunt defects, a higher density of small optically-unresponsive (i.e. "dead") areas were evident with OBIC.

3.1.2 Glass Cleaning Matrix Study

To further investigate methods to improve the quality of the glass surface, a matrix of 120 10x10 cm test structures were divided into four groups and processed separately as follows: (1) normal

(a) SEM image showing a depression in the ZnO layer.

(b) Enlarged SEM image of area in (a) with the Mo/CIS/ZnO removed showing an underlying crack in the glass substrate.

Fig. 3.2. SEM of a ZnO surface defect in a CIS module.

baseline detergent wash; (2) polished with CeO_2 before detergent wash; (3) 3 min 5% HF etch before detergent wash; and (4) CeO_2 polish before detergent wash followed by the 3 min 5% HF etch after the detergent wash. The results are summarized in Tables 3.1 and 3.2.

Table 3.1. Overall Average Cell Performance.

	Eff (%)	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF
Baseline	9.68	417	37.0	0.622
HF etch	9.73	422	36.7	0.628
CeO_2 polish	8.93	406	36.1	0.605
CeO_2 + HF	9.48	418	36.5	0.616

Table 3.2. Average Cell Performance without Shunted Cells.

	Eff (%)	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF
Baseline	9.77	421	37.0	0.626
HF etch	9.73	422	36.7	0.628
CeO_2 polish	9.02	408	36.2	0.608
CeO_2 + HF	9.65	422	36.6	0.624

Although the result of the experiment is that there was essentially no effect of the HF etch or the CeO_2 polish plus HF etch on the cell performance distribution, a more detailed evaluation of the data brings out several points of interest. The baseline cell population can be characterized by a bimodal distribution, namely cells with an average efficiency of 9.77% in addition to some cells that are very shunted (1% efficiency range), resulting in an overall average efficiency of 9.68%. HF etching by itself eliminates the number of very shunted cells giving an overall average efficiency of 9.73%. but which is slightly less than the non-shunted baseline average of 9.77%. Polishing alone also reduces the number of very shorted cell (1% efficiency range), but degrades the average non-shunted cell performance to 9.02%, resulting in an overall average for the polished sample population of 8.93%. This is attributed to the removal of large defects and the creation of many very small defects (trading a few large shunts for many small ones). Polishing plus HF etching apparently smooths out these distributed small defects (improving the average non-shunted efficiency to 9.65%), but somehow creates large defects again, possibly by opening up "potential shunts" or defects just below the surface of the glass that would otherwise not be exposed. The result is an overall average efficiency for this group of 9.48%.

The implication of this study for CIS modules is that HF etching the glass substrates should improve the module performance. Since the module consists of 53-series connected cells, very shunted cells significantly degrade the module performance. Based on the test structure results, HF etching eliminates the very shunted cells. Two issues must be addressed: (1) what is the impact of HF etching of the glass substrate on the module interconnects; and (2) what are the environmental and regulatory issues of implementing HF etching on a large scale module manufacturing line. Some form of chemical etching of the glass substrates seems necessary to reduce large shunting defects. Exploration of alternative non-HF chemical etches of glass is appropriate.

3.1.3 Vendor Glass Evaluation

A preliminary comparison split between two glass vendors showed module outputs of 34-36 watts (440 mV average cell V_{oc} 's) for one vendor compared to 30-33.5 watts (425 mV average cell V_{oc} 's). This study was then expanded to include glass samples from several manufacturers. All soda-lime glass samples showed curl of the Mo/CIS at Pattern 1, P1 (Mo isolation laser scribe) and varying width low OBIC response regions adjacent to the interconnect. OBIC losses extend up to 0.5 mm beyond the physical interconnect patterns, reducing module power by about 10 points. In addition, poor adhesion in this near-P1 region can cause shunting which reduces module power by another 10 points.

Chemically treated glass (which changes both the surface morphology and the glass surface chemistry) shows minimal "dead" (low OBIC response) regions. Samples grown on Mo deposited with an air/water leak showed no dead region. In addition, 7059 borosilicate glass and quartz both showed no dead region. The dead regions around the Pattern 1 are believed to be caused either by contamination, film stress, or both. Larger quantities of the chemically treated glass have been ordered and will be evaluated during the Phase 2.

3.2 Module Processing Studies

Two processing studies carried out in Phase 1 were a study of the effect of time delays during CIS module fabrication and an investigation of the impact of background water levels during processing. Four types of processing time delays were evaluated, namely time delays between: (1) Mo and CIS deposition; (2) CIS and CdS deposition; (3) CdS and ZnO deposition; and (4) overall start-to-finish. Figs. 3.3 through 3.6 plot the impact on module V_{oc} and power output for these various delays. Although the data was collected from a large number of different processing studies and scatter exists in the data, trends are apparent. Fig. 3.3 shows that time delays between the Mo and CIS deposition steps have little influence on module performance. For the junction formation steps, a slight loss in V_{oc} due to delays between the CIS and CdS layers (Fig. 3.4) and between the CdS and ZnO layers (Fig. 3.5) is

(a) Module V_{oc} versus time delay.

(b) Module power versus time delay.

Fig. 3.3. Effect of time delay between the Mo/CIS steps.

(a) Module V_{oc} versus time delay.

(b) Module power versus time delay.

Fig. 3.4. Effect of time delay between the CIS/CdS steps.

(a) Module V_{oc} versus time delay.

(b) Module power versus time delay.

Fig. 3.5. Effect of time delay between the CdS/ZnO steps.

(a) Module V_{oc} versus time delay.

(b) Module power versus time delay.

Fig. 3.6. Effect of time delays from Start-to-Finish.

apparent, although there is no significant loss in module power. Delays at these steps would increase the probability of damage or dust and other contamination of the junction interfaces. Finally, except as noted for the junction fabrication steps, Fig. 3.6 shows that there is no significant power loss due to differences in total fabrication time.

Modules fabricated with very high (5 relative % H_2O) partial pressures of water vapor during CIS film deposition resulted in modules with more severe "curl" (that is, CIS delamination from the Mo electrode layer in the region adjacent to Pattern 1. The CIS/Mo adhesion in the cell areas away from the patterns was unaffected. Overall, high water background levels do not seem to have a serious impact on the formation of CIS.

3.3 CIS Unencapsulated Module Performance

During Phase 1, several unencapsulated CIS module plates achieved output powers above 40 watts with the best₂ equal 40.8 watts or 10.5% aperture efficiency based on a 3890 cm² aperture area at 100 mW/cm² ASTM air mass 1.5 global spectrum and 25 C. Fig. 3.7 shows the I-V curve for this best CIS unencapsulated module.

Voc	= 24.5 V	Vmax	= 18.36 V
Isc	= 2.55 A	Imax	= 2.22 A
FF	= 0.654	Pmax	= 40.8 W
Soc	= 0.1355		
Ssc	= 0.0319		

Fig. 3.7. I-V curve for a 40.8 W CIS unencapsulated module.

SECTION 4 MODULE DELIVERABLES

The primary objective of this program is to demonstrate 12.5% aperture efficient, large area (3900 cm²) encapsulated thin film CuInSe₂ (CIS) modules as part of a 3-year, 3-phase cost shared contract which began on May 1, 1991. To chart the research progress, the milestones defined in the contract are summarized in Table 4.1 below.

Table 4.1. Contract Deliverables

Milestone	Date	Deliverable
Phase 1 M1	7/31/91	4 encapsulated CIS modules (1 ft ²) for reliability testing at NREL.
M2	4/30/92	An encapsulated 36.5W, 9.4% efficient (aperture area) CIS module.
Phase 2 M3	7/31/92	4 encapsulated CIS modules (1-4 ft ²) for reliability testing at NREL.
M4	7/31/92	An encapsulated 38.8W, 10% efficient (aperture area) CIS module.
Phase 3 M5	7/31/93	An encapsulated 44.6W, 11.5% efficient (aperture area) CIS module.
M6	7/31/93	4 encapsulated CIS modules (1-4 ft ²) for reliability testing at NREL.
M7	4/30/94	An encapsulated 48.5W, 12.5% efficient (aperture area) CIS module.

4.1 CIS Module Measurement Comparison between NREL and SSI

Verifying agreement between SSI and NREL CIS module measurements was an important issue early in the contract. Prior to the contract, when NREL upgraded their Spire 240A solar simulator during the summer of 1990, the I_{sc} values of the SSI CIS MAR10 modules at NREL measured 7% less than their values before the upgrade. Thus, in May 1991, a laminated/framed CIS module (#182-5) was delivered to NREL for testing. Spectral mismatch correction is required. Without spectral correction, the measured CIS I_{sc} using Si reference cells is low compared to its true value (that is, I_{actual} equals $I_{measured}$ divided by the spectral mismatch factor M, where M equals 0.975). A 20-cell, 10 cm wide CIS minimodule fabricated

at SSI was calibrated on the NREL X25 solar simulator and used to set the LAPSS intensity. The LAPSS has much better illumination uniformity (+/- 0.5%) and measurement electronics than the Spire 240. The NREL Spire 240 measured 7% lower J_{sc} than SSI, consistent with the J_{sc} drop noted for the CIS MAR10 modules. The NREL LAPSS data compares very closely with the SSI. J_{sc} data agrees within 1.6%.

Table 4.2 SSI and NREL data comparison for module 182-5

	Power (W)	Eff (%)	I_{sc} (A)	V_{oc} (V)	FF
SSI R&D LAPSS (Before)	38.1	9.8	2.51	24.3	0.626
SSI R&D LAPSS (After)	37.5	9.7	2.48	24.3	0.624
SERI Spire 240	36.2	9.3	2.31	24.2	0.647
SERI LAPSS	37.7	9.7	2.44	24.0	0.644
SERI LAPSS/SSI Ratio (%)	100.5	100.5	98.4	98.8	103.2

Notes:

1. Efficiency based on 3883 cm^2 (30.6 x 126.9 cm) aperture area.
2. SERI Spire data has 0.975 spectral mismatch correction. SERI LAPSS was calibrated from the SERI X25 using a CIS minimodule.

4.2 CIS Encapsulated Module Deliverables

During Phase 1, SSI met all performance milestones and program deliverables. A new world record of 37.7W and 9.7% aperture efficiency for a 3883 cm^2 (126.9 x 30.6 cm) encapsulated CIS module was demonstrated and verified at NREL. Table 4.3 summarizes the photovoltaic parameters for the 4 CIS modules shipped to NREL to meet the M1 milestone.

Table 4.3. Parameters for CIS modules delivered to NREL

Module #	Power (W)	I_{sc} (A)	V_{oc} (V)	FF
282-5	31.0	2.42	22.7	0.563
324-4	30.9	2.38	22.4	0.580
324-6	30.0	2.38	22.0	0.575
324-16	29.8	2.40	21.9	0.566
182-5	37.7	2.44	24.0	0.644

The individual current-voltage (I-V) curves are shown in Figs. 4.1-4.4. The power outputs are in the 30-31 watt range. The CIS circuits are laminated behind tempered glass and framed using a reaction injection mold (RIM) process. Electrical connection is provided by a two-conductor cable. The 37.7 W, 9.7% aperture efficient CIS module, reported in Section 4.1, fulfilled the M2 milestone of the contract and was shipped to NREL with the M1 milestone deliverables. Its photovoltaic parameters are also included in Table 4.3.

V_{oc}	$= 22.7 \text{ V}$	V_{max}	$= 15.5 \text{ V}$
I_{sc}	$= 2.42 \text{ A}$	I_{max}	$= 2.00 \text{ A}$
FF	$= 0.563$	P_{max}	$= 31.0 \text{ W}$
S_{oc}	$= 0.23$		
S_{sc}	$= 0.029$		

Fig. 4.1. I-V curve for module 282-5.

Voc	= 22.4 V	Vmax	= 15.3 V
Isc	= 2.38 A	Imax	= 2.01 A
FF	= 0.580	Pmax	= 30.9 W
Soc	= 0.19		
Ssc	= 0.048		

Fig. 4.2. I-V curve for module 324-4.

Voc = 22.0 V
 Isc = 2.38 A

Vmax = 15.7 V
 Imax = 1.91 A

FF = 0.575
 Soc = 0.20
 Ssc = 0.040

Pmax = 30.0 W

Fig. 4.3. I-V curve for module 324-6.

VOC = 21.9 V Vmax = 15.1 V
 ISC = 2.40 A Imax = 1.97 A

 FF = 0.566 Pmax = 29.8 W
 SOC = 0.22
 SSC = 0.062

Fig. 4.4. I-V curve for module 324-16.

SECTION 5.0 CONCLUSIONS

A baseline characterization of the CIS modules has been established during Phase 1. Maps of the open circuit voltage provide information on the uniformity of the junction quality. Maps of the cell voltages at a fixed forward bias detail the variations in resistance losses due to individual interconnects or ZnO sheet resistance. Individual cell I-V curves can be evaluated by measuring the dependence of the voltage drop of each cell on the applied module current. The physical nature of the defects is then correlated using OBIC, EBIC, SEM, and other techniques such as tape adhesion testing.

Fabrication of large area CIS modules on 0.4 m² glass substrates (32.2 x 128.6 cm) presents issues of the defect distributions in the incoming low-cost glass substrates, spatial uniformity of large area processing, and defects introduced during module fabrication. The cell interconnects in a monolithic module introduce electrical and morphological issues which are not present in discrete devices. Research is focusing on improved materials and processing quality.

SECTION 6.0 FUTURE PLANS

The performance milestones and deliverables defined in the contract for Phase 2 are not expected to be changed. Efforts will continue to address understanding of the mechanisms which control CIS module performance, defining improvements in module design and processing leading to CIS module aperture efficiencies of 12.5%.

SECTION 7.0
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**APPENDIX A
PRESENTED PAPERS**

1. R. Gay, J. Ermer, C. Fredric, K. Knapp, D. Pier, C. Jensen, D. Willett, "Progress in Large-Area CuInSe₂ Thin Film Modules", *Proc. 22nd IEEE Photovoltaic Specialists Conf.*, Las Vegas, Nevada, October 7-11, 1991, pp 848-852.
2. D. Tarrant, A. Ramos, D. Willett, R. Gay, "CuInSe₂ Module Environmental Durability", *Proc. 22nd IEEE Photovoltaic Specialists Conf.*, Las Vegas, Nevada, October 7-11, 1991, pp 553-556.

PROGRESS IN LARGE-AREA CuInSe₂ THIN FILM MODULES

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ABSTRACT

Prototype modules of CuInSe₂ (CIS) have been fabricated with efficiencies that exceed 10%. The challenge now is to improve the processing yield of these modules to that suitable to advance to pilot manufacturing. A number of analytical tools have been developed to provide insight into the loss mechanisms in these large area monolithic structures. Techniques for characterizing the adhesion of the semiconductors, the device quality, the interconnect quality and the film uniformity are discussed. Improvements in adhesion have eliminated the primary cause of mechanical failure, leading to tighter module efficiency distributions. Similar improvements in the control of interconnect quality have also been achieved, leading to higher yields. Further improvement in the uniformity of the device quality will provide the reproducibility required for CIS pilot manufacturing.

INTRODUCTION

The development of a new photovoltaic product evolves through a series of stages. In the first stage, the emphasis is on the semiconductor, with the goal of demonstrating high energy conversion efficiency. Little emphasis is placed on uniformity, size, or yield issues, although the general approaches are chosen to be compatible with the longer-term needs for low-cost manufacturing. In the next stage, the emphasis is on prototype development. Here the semiconductor process must be scaled up to large areas with good uniformity and reproducibility. The details concerning the circuit and package must be defined with a target product specification in mind. Prototypes are fabricated and subjected to accelerated environmental testing. The next transition is into the pilot manufacturing stage, where the emphasis is on yield and costs. When the yields are sufficiently high and the costs are adequately low, the pilot stage can progress to the fully mature manufacturing technology, where economies of scale are achieved.

Siemens Solar Industries is in the process of developing a new thin film photovoltaic product

based on copper indium diselenide (CuInSe₂ or CIS). The fabrication of CIS modules has been described elsewhere [1,2]. In the evolution of CIS, Siemens Solar is now far into the prototype development stage. For the semiconductor, deposition equipment has been developed to achieve uniform films over large areas. A monolithic structure on a glass substrate with the dimensions 32.2 cm x 128.6 cm was chosen for the circuit, as it is anticipated that this will be the lowest cost approach. Patterning equipment has been developed to cut the films into the desired shapes to construct the circuit. A prototype package has been defined as a tempered glass/ethylene vinyl acetate (EVA)/CIS circuit/substrate laminate with a reaction injection molded (RIM) polyurethane frame to provide the electrical and environmental isolation of the circuit [3-5].

PROTOTYPE PERFORMANCE

Prototypes of this product have been fabricated. An unencapsulated module aperture-area efficiency of 10.4% has been measured [6]. Packaged modules have been subjected to a variety of tests, including outdoor exposure, accelerated environmental testing, and wet high-pot testing [7]. While high efficiency has been achieved, the yields of high-efficiency modules are not yet high enough to begin pilot production. Further, while durable modules have been demonstrated, not all modules pass the accelerated environmental testing.

Figure 1 shows the distribution of a large group of 0.4 m² modules. While efficiencies over 10% are attained, the bulk of the distribution is centered around 7% with a significant population having much lower efficiencies. Many of the lower efficiency modules are suffering from poor adhesion of the CIS to the molybdenum base electrode. In some cases, the adhesion is so poor that the CIS peels off the molybdenum in large patches. This peeling can make the circuit lose electrical continuity. If the peeling occurs before or during the ZnO deposition, the ZnO can shunt the devices. Either failure leads to extensive power loss.

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Fig. 1. Efficiency distribution for CIS modules with poor adhesion.

Factors that affect the strength of the adhesion between the layers in the device stack have been discussed elsewhere [6]. By modifying the circuit fabrication process to improve the adhesion, a significantly tightened distribution was achieved (Fig. 2). While much of the low end of the distribution has been eliminated, the peak efficiency remains at 10% and the average has shifted up to 8.5%. How then can the average be shifted higher?

To respond to this question, it is useful to review and compare the characteristics of CIS cells and modules. Table 1 presents a comparison of the light I-V characteristics of the best single cell devices, the best modules, and the average values for the group of modules with good adhesion shown in Fig. 2.

For the purposes of the current discussion, the most interesting comparison is between the best 0.4 m² module and the average 0.4 m² module. The voltage of the average module is over 9% lower than the voltage of the best module. This difference has the strongest impact on performance. The next most important difference is in the fill factor, which is 8% lower for the average module than the best module. The differences in the short circuit currents are quite small, less than 2%.

Fig. 2. Efficiency distribution for CIS modules with good adhesion.

The I-V curve of a module is created by the current flowing through all of its composite cells. This composite module I-V curve yields little information about the nature of the individual cells that comprise the module. To understand the suppression of the open circuit voltage, a systematic study was undertaken to characterize the uniformity of the voltage over the 0.4 m² modules. To prepare a map of the voltage over the surface of a module, it was cut into a set of nine slices (Fig. 3). The open circuit voltage of every cell on all nine slices was then measured and plotted in the form of a contour plot, or "V_{oc} map".

Fig. 3. CIS module slices.

Table 1. Comparison of light I-V characteristics.

	Best Test Device (1 cell)	Unencapsulated Modules		
		Best 0.1 m ² Module (55 cells)	Best 0.4 m ² Module (53 cells)	Average 0.4 m ² Module (53 cells)
Area ^b (cm ²)	3.5	938	3890	3890
V _{oc} /cell (mV)	508	464	464	421
J _{sc} (mA/cm ²)	41.0	39.3	37.0	36.4
Fill Factor	0.677	0.639	0.652	0.60
Efficiency ^b (%)	14.1	11.2	10.4	8.5
Power (W)	---	10.5	40.4	33.0

^a100 mW/cm² ASTM air mass 1.5 global spectrum, 25°C.

^bActive area for test device; aperture area for modules.

Fig. 4. Voltage maps comparing higher and lower power CIS modules.

In Fig. 4, V_{oc} maps are shown for a 39 watt (10.0% efficient) module and a 32 watt (8.2%) module. The voltage is very uniform for the higher power module. The voltage of the lower power module is not only suppressed overall, but also suffers from a significant reduction in voltage along one side. Measurements made on many modules indicate that, in general, higher voltage modules are achieved through both improved uniformity and enhanced average voltage. The origin of this difference between higher and lower voltage modules has not yet been determined but represents the primary hurdle to improved yields of high efficiency modules.

INTERCONNECTS

While the fill factor of a module does relate back to its voltage, it is also very sensitive to the quality of the interconnects between cells. Figure 5a shows the I-V curve of a module with a poor fill factor (0.530). Again, the composite I-V curve is of little value in determining the problem with the circuit. This module was cut into slices, as previously described. The I-V curve of one of the slices, shown in Fig. 5b, is typical of the rest of the slices and shows an even worse fill factor (0.456). The inverse curvature near open circuit might be interpreted as arising from blocking junctions.

Additional measurements were made on the individual cells in this slice. First, the open circuit voltages were measured, as described above for the V_{oc} maps. In this light-biased measurement, no current flows and the voltage between cells represents the incremental increase in voltage due to the V_{oc} of each cell. This showed only slight variations down the slice.

A second measurement was then made in which the slice was forward biased in the dark so as to flow 240 mA (36 mA/cm²) through the cells (approximately equal to the 1-sun short circuit current density of 38 mA/cm²). The voltage drop between cells now represents the sum of the I-R resistive

Fig. 5a. I-V curve of an unencapsulated 0.4 m² CIS module.

Fig 5b. I-V curve of one slice of the module of Fig. 5a.

Fig. 5c. V_{oc} and dark forward bias voltage measurements of the slice of Fig. 5b.

term from the interconnect plus the voltage required to forward bias the diode to this current. The latter term is approximately equal to the open circuit voltage.

Results of these two measurements are shown in Fig. 5c. Evident in the dark forward bias voltage measurements were a number of cells that showed anomalously high dark forward bias voltage drops. These high voltage drops were likely caused by poor quality interconnects, a suspicion confirmed by detailed inspection. I-V measurements of these interconnects showed them to be rectifying, giving rise to the inverse curvature noted in the slice I-V curve. Once this technique had been developed for detecting poor interconnects, the resulting feedback made it possible to determine the cause of the problem, which was then resolved.

Since poor interconnects can so clearly impact module fill factor, a simple, direct method for measuring interconnect quality is needed. While stepping resistance measurements can be used to obtain a number for the contact resistance, this method measures the contact resistance very locally. An alternate method has been developed in which two interconnect patterns are cut back-to-back, as shown in Fig. 6. An "interconnect test structure" uses the standard module patterning equipment with the standard module spacing to fabricate 53 pairs of interconnects on a module. The modules are cut into the slices described in Fig. 3. Electrical leads are attached to the ends of a slice, and the slice is biased so that about 38 mA/cm² of cell area (typical of 1-sun short circuit current densities) is forced through the entire series of 106 interconnects. The current path, as shown in the figure, travels down the molybdenum, up through one interconnect, across the ZnO, and back through the other interconnect to the molybdenum. This path is repeated through the entire series of interconnects.

A test jig is used to position voltage probes at the cell spacing down the length of the slice. These probes measure the change in voltage across the pair of interconnects. After correcting the voltage drops for the known losses due to the sheet resistance of the molybdenum (0.3 $\Omega/\square$) and the ZnO (5.5 $\Omega/\square$), the remaining loss is a measure of the

interconnect contact resistance. This calculation results in a value of 0.5 m Ω -cm².

Assuming that the measured sheet resistances of the ZnO and molybdenum are uniform, a distributed resistance model may be used to calculate the power losses due to the electrodes and interconnects. The results of such a calculation are shown in Table 2.

Table 2. Analysis of power losses due to distributed resistance.

ZnO (5.5 $\Omega/\square$)	7.0%
Molybdenum (0.3 $\Omega/\square$)	0.5%
Interconnects (0.5 m Ω -cm ²)	0.5%

The losses due to the average interconnect contact resistance are quite small. This is in contrast to the previous example in which the failure of a number of interconnects lead to significant reduction in the fill factor.

However, losses due to the sheet resistance of the ZnO are not small. As has been described elsewhere [8,9], optimization of the ZnO layer balances the trade off between resistive losses due to the sheet resistance against optical and mechanical considerations. The ZnO must be uniform to achieve the desired performance.

ZnO UNIFORMITY

To characterize the uniformity of the ZnO films, witness glass was coated with ZnO using the standard process. The thickness of the ZnO is measured over the surface of the part using a technique based on optical interference. The sheet resistance is measured at the same points using a four-point probe. The results of a typical set of these measurements are shown in Fig. 7. The unifor-

Fig. 6. Interconnect test structure. Arrows show the flow of current.

Fig. 7. The top figure shows the uniformity of the sheet resistance of ZnO; the bottom figure shows the uniformity of the thickness.

mity in thickness is very good; the average thickness is 2.22 μm , with a standard deviation of 4%. The average sheet resistance is 5.1 $\Omega/\square$, with a standard deviation of 16%. There is one point at which the sheet resistance goes as high as 7.3 $\Omega/\square$. The calculated power loss from the distributed resistance model behaves linearly with sheet resistance, so the increased power loss is expected to be proportional in size and magnitude to the increased sheet resistance. In this case, the additional losses would be small.

SUMMARY

The transition from the research phase to the prototype development phase in the evolution of CIS has been made. The "existence proof" of a high efficiency (10.4%) large area (0.4 m^2) CIS module has been demonstrated. A similar existence proof for stable modules of such efficiencies has also been demonstrated. Our goal is now to make these modules reproducibly. This paper describes a number of techniques that have been developed to investigate the uniformity of the devices and the quality of the interconnects and individual layers. These techniques are now part of the toolbox that is being applied to address the issues of reproducibility, uniformity, and yield. Improvements in process control, or a shift to more "robust" processing approaches, are being made to tighten and improve power distributions and allow CIS to complete prototype development and move forward to pilot manufacturing.

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CuInSe₂ MODULE ENVIRONMENTAL DURABILITY

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ABSTRACT

Stability of CuInSe₂ (CIS) modules through outdoor testing and accelerated environmental testing has been demonstrated on 0.4 m² modules. Package durability has been demonstrated for 0.4 m² laminates with polyurethane frames. Although stability has been demonstrated, a distribution of results is common with power changes ranging from slight gains to losses greater than 10%. Correlations and distinctions between the distributions for outdoor and accelerated environmental testing are discussed. During accelerated environmental testing, temperature effects alone, rather than temperature combined with humidity, cause changes in power. An interaction between CIS and the package is not necessary to cause these changes in power. Variations in the CIS cell structure are probably responsible for outdoor testing and accelerated environmental testing results.

INTRODUCTION

Thin film CuInSe₂ (CIS) is a promising high power, low cost photovoltaic material, both as a stand alone single junction circuit and as the narrow band gap component in tandem junction circuits [1-3]. With the demonstration of efficiencies over 14% on small area devices [4], the focus of CIS technology development at Siemens Solar Industries is increasingly directed toward large areas, process uniformity, process reproducibility, and module durability. As a result of the focus on scale up, aperture area efficiencies of over 10% have been achieved, first on 0.1 m² circuits [5] and more recently on large area (0.4 m²) un laminated CIS circuits [6].

In previous environmental durability studies with 0.1 m² modules, groups of modules with no significant power change after 10 humidity-freeze cycles were reported and long term outdoor power stability was demonstrated [7]. Package durability in accelerated environmental testing was also demonstrated for the 0.1 m² part size.

In this paper, outdoor test data and accelerated environmental test data for 0.4 m² modules are presented and discussed in relation to the qualifi-

cation of CIS as a durable photovoltaic material. Stable performance has been demonstrated for outdoor and accelerated testing. However, a distribution of results has been seen for these prototype modules with power changes ranging from slight gains to losses greater than 10%. Correlations and distinctions between outdoor testing and accelerated environmental testing are discussed. Results of preliminary experiments to determine the cause of the distributions are presented.

SUBMODULE FABRICATION

The basic CIS cell structure includes a ZnO front transparent electrode, a thin (less than 50 nm) CdS layer, the CIS layer, a Mo back metal electrode, and a soda lime glass substrate. Gallium is added to the CIS layer in low concentrations to improve cell performance. A detailed description of the CIS cell structure and an analysis of CIS junctions are presented elsewhere [8,9].

Monolithic, integrated CIS submodules (complete circuits before lamination and framing) are fabricated on 4140 cm² glass substrates 32.2 cm x 128.6 cm. A submodule is divided into 53 cells, each 0.577 cm wide, using multibeam laser scribing and multitip mechanical scribing. The submodule interconnect region is discussed in detail elsewhere [4,9]. A perimeter area is used for lead attachment and is subsequently covered by the module frame during packaging operations. For some studies, the 0.4 m² circuit plates are cut into nine "slices" each approximately 10 cm wide (Fig. 1). Each slice is a complete 53 cell string and the nine slices map the performance along the long dimension of the 0.4 m² circuit plate.

MODULE PACKAGING

Submodules are encapsulated to mechanically protect the thin film layers, and the encapsulated submodules are framed to protect and strengthen the module package and provide for mounting. The first step is to solder electrical leads onto the circuit. A cover glass sheet is then laminated to the submodule plate with thermally cured ethylene vinyl acetate (EVA) to form a durable glass/EVA/thin film circuit/glass laminate. The cover glass is low iron, waterwhite glass, which reduces photocurrent

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Fig. 1. Slices cut from a module to enable further studies.

loss due to absorption in the cover glass. The present prototype design uses a 0.3 cm thick thermally tempered cover glass with approximately the same dimensions as the submodule substrate. Finally, reaction injection molding (RIM) is used to form a frame that provides additional mechanical support and mounting points.

OUTDOOR TESTING

Module stability is being evaluated under continuous outdoor exposure at test sites in Colorado and California. The longest term results available (Fig. 2) are for 0.1 m² submodules laminated with EVA between a cover glass and a backing metal. The power after more than 1000 days of continuous outdoor exposure at the SERI PV Outdoor Test Site in Golden, Colorado, has stabilized at approximately 95% of initial power [10].* This minimal loss after 1000 days of outdoor exposure is a demonstration of long term stability for CIS.

Long term stability has also been demonstrated for glass/glass packages. Minimal loss has been demonstrated after 700 days of cumulative outdoor exposure at test sites in Chatsworth and Camarillo, California, for 0.1 m² submodules laminated with EVA in a glass/glass package with a RIM formed frame. Outdoor exposure of 0.4 m² modules in a glass/glass package has been measured for almost 4 months in Camarillo (Fig. 3). Stable performance has been demonstrated although a distribution is observed with power changes ranging from slight gains to losses approaching 10%. Characteristics of the distribution for 0.4 m² modules are similar to characteristics for the 0.1 m² modules with 700 days of cumulative outdoor exposure. Differences in the

*The data in Fig. 2 were obtained at SERI using two different solar simulators. One solar simulator was used for the first 600 days and a second from then on. For comparison of data from the two simulators, data from the second simulator is normalized to the last measurement taken on the first simulator [10].

Fig. 2. Stability of CIS 0.1 m² modules after more than 1000 days of exposure outdoors.

change in power with outdoor exposure are dominated by differences in the changes in fill factor. The fill factor usually increases early in the outdoor exposure but may then drop below the initial value. Based on the 0.1 m² module data, changes in fill factor stabilize after about 400 days of exposure. There is also a current change that appears to consistently stabilize at a 3 to 4 point loss. Open circuit voltage does not change significantly.

ACCELERATED ENVIRONMENTAL TESTING

Accelerated environmental tests were conducted according to the Flat-Plate Module Qualification Test Procedure defined in the Technical Specifications and Scope of Work for the Emerging Technologies - 2 section of the PVUSA project [11], which closely parallels the SERI Interim Qualification Tests and Procedures for Terrestrial Photovoltaic Thin-Film Flat-Plate Modules [12]. The standard prototype package was a RIM framed 0.4 m² module. Delamination of the circuit plate from the cover glass was initially a problem and was resolved by changes in lamination and RIM framing techniques.

Corrosion susceptibility and wet hi-pot tests were performed simultaneously by using test criteria that were more rigorous than those defined by either test: less than 30 microamps at 3000 V while fully

Fig. 3. Stability of CIS 0.4 m² modules after more than 120 days of exposure outdoors.

immersed in a water/wetting agent. Modules passed the more rigorous test both before and after all environmental tests. Measurements were made both immediately after the humidity-freeze cycles and after the additional time required for structural integrity and hail impact tests. While acceptable currents were measured at both times, measurement immediately after humidity-freeze cycles is the more stringent test since the measured currents were significantly higher immediately after removing the modules from the humidity-freeze cycles.

Modules also passed static load, hail-impact, and hot-spot endurance tests. The hot-spot endurance test was performed following as closely as possible a proposed procedure for non-intrusive testing by the International Electrotechnical Commission. No significant change in power was noted after more than five hours of exposure to greater than 900 W/m² with one cell shaded.

As with outdoor testing, temperature cycling and humidity-freeze cycling tests produce a distribution of powers after cycling. Similar distributions result from both humidity-freeze and temperature cycling using procedures defined by either the Jet Propulsion Laboratory Block V test procedure [13] or by the SERI Interim Qualification Tests and Procedures [12].

Figure 4 summarizes results from humidity-freeze tests and a temperature cycling test that was defined to distinguish between temperature effects and temperature combined with humidity effects. For the data presented in Fig. 4, the temperatures and cycle times for temperature cycling were made the same as for the humidity-freeze cycles.

Stability of CIS modules through accelerated environmental testing is demonstrated by groups of modules where all modules pass the humidity-freeze test. Indeed, most modules pass the humidity-freeze test, retaining more than 90% of their initial power. However, some still fail the test. The distribution for the temperature cycling without humidity is not significantly different from the humidity-freeze test, indicating that exposure to humidity is not necessary to cause the observed loss in power.

Fig. 4. Changes in initial power of CIS 0.4 m² after humidity-freeze and temperature cycling tests.

There are similarities and differences between the results obtained from outdoor testing and accelerated environmental testing. In both outdoor testing and accelerated environmental testing, changes in power are dominated by changes in fill factor. Also, the open circuit voltage does not change significantly in either test. However, outdoor testing causes a 3-4% loss in current whereas accelerated environmental testing shows no significant change.

ADDITIONAL STUDIES

Experiments were conducted to determine if there are effects due to the packaging process or contact with EVA during accelerated environmental testing. Complete 53-cell slices, approximately 10 cm wide, cut from 0.4 m² modules were used for the experiments. Module slices with and without the standard lamination process used for 0.4 m² modules were subjected to the temperature cycle of humidity-freeze cycling but without humidity. The module slices with no lamination were sealed using aluminum foil and aluminum foil tape with butyl rubber adhesive to protect the films from residual humidity that might be encountered during temperature cycling. The distributions after temperature cycling for laminated and unlaminated module slices were similar. The packaging process or an interaction with the EVA is not necessary to produce the power loss distributions.

The distributions after temperature cycling for laminated and unlaminated module slices were also similar to the distributions for 0.4 m² modules that were temperature cycled or humidity-freeze cycled. This result is a preliminary indication that there is no systematic variation in the long dimension of a 0.4 m² module. Studies of individual cells in the cell string are under way.

Experiments have begun to determine the mechanisms for changes in fill factor during outdoor testing or accelerated environmental testing. Laminated ZnO on glass structures, mimicking the lamination process for 0.4 m² modules, with copper ribbon voltage probes were subjected to humidity-freeze cycling. Changes in the ZnO sheet resistance were small and could not be responsible for the observed distributions after accelerated environmental testing.

Changes at the interconnects could also cause changes in fill factor and the observed distributions. CIS module slices were patterned [14] to separate the effects of interconnect contact resistance from diode parameters and were then subjected to humidity-freeze cycling. Changes in the interconnect contact resistance were observed but the magnitude of the changes also does not explain the observed distributions. Further studies of this type are under way.

SUMMARY

Stability of large area, 0.4 m², CuInSe₂ solar cell modules has been demonstrated by outdoor

testing for over 1000 days and by accelerated environmental testing. Although stability has been demonstrated, performance variations are observed. Differences between modules are dominated by differences in the change in fill factor from both outdoor testing and accelerated environmental testing. A secondary change in current is observed from outdoor testing but not from accelerated environmental testing. Preliminary studies indicate that the changes in fill factor are not due to interactions with the package, changes in ZnO resistivity or changes in interconnect contact resistance; therefore, nonuniformities in the CIS cell structure are believed to be responsible for variations in results from outdoor testing and accelerated environmental testing. Improvements in process control and processing uniformity are being pursued to complete CIS prototype module development.

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