UCRL-10009 Rev.

UNIVERSITY OF CALIFORNIA

Lawrence Radiation Laboratory
Berkeley, California

Contract No. W-7405-eng-48

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ABSTRACT

Presented herein is a philosophy for designing wideband multistage transistor amplifiers. The amplifier is visualized as an integral unit, the interstage networks constituting the elements of the amplifier unit. By designing the amplifier as a unit and adjusting the overall response (gain and bandwidth) with the interstage time constants, an increase in gain-bandwidth product is realized over the iteratively designed amplifiers. The resulting increase in gain-bandwidth product results from absence of the bandwidth shrinkage factor for multistage amplifiers.

Formulas are derived for both a two- and three-transistor integrally designed wideband amplifier, in which shunt peaking networks are used for coupling. Experimental amplifiers were constructed following these formulas, and the observed performance agreed quite well with the calculations.

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I. INTRODUCTION

A greater overall gain-bandwidth product for multistage amplifiers is realizable through a design procedure that characterizes the total amplifier rather than characterizing each stage separately. The design entails picturing the several stages of the amplifier as an integral unit and adjusting the individual time constants to obtain the desired overall response. The principle of stagger tuning[1] has been applied to transistor amplifiers by Victor H. Grinich[2] and others, and can be considered as an application of the integral-unit philosophy of circuit design. However, the use of this design philosophy as shown in this paper is not yet reported elsewhere in print.

The increase in gain-bandwidth product will be shown to result from the absence of the bandwidth shrinkage factor in the calculation. Here the bandwidth shrinkage factor is the ratio of overall amplifier bandwidth to the interstage bandwidth of an iteratively designed amplifier. If the iteratively designed amplifier has a single-time-constant (one-pole) response, the shrinkage factor is given by $(2^{1/N}-1)^{1/2}$, where N is the number of cascaded stages. Absence of the shrinkage factor is the result of an integral-unit design philosophy, rather than an iterative (i.e., identical-stages-cascaded) design. The convenience of designing one stage and then cascading costs the designer a fraction of the attainable gain-bandwidth product of the multistage amplifier. The integral-unit philosophy is applied here

*Work done under the auspices of the U. S. Atomic Energy Commission.

to the design of both two- and three- transistor amplifiers utilizing shunt-peaked interstage networks. Shunt-peaking interstage networks are selected because of their relative simplicity and conservation of gain-bandwidth product when broad-banded. The gain-bandwidth product of a shunt-peaked interstage is approximately equal to f_t of the transistor.[3]

As shown in Appendix A, the current gain of a typical shunt-peaked interstage is of the form

$$A_i = H \frac{p+z}{p^2+ap+b},$$

where $p = j\omega$ and H is a constant.

It can easily be shown that the shunt-peaked interstage can be designed to yield a single-time-constant (one-pole) form of response.[4] This occurs by factoring the denominator polynomial into two real roots, one of which is set equal to the numerator term (the zero), and the resulting function is of the form (see Appendix A)

$$A_i = \frac{H}{p+c} \cdot \frac{p+z}{p+z} = \frac{H}{p+c}.$$

For two shunt-peaked interstages connected in series the current gain is of the form

$$A_I = H_1 H_2 \frac{p+z_1}{p^2+a_1 p+b_1} \times \frac{p+z_2}{p^2+a_2 p+b_2}.$$

Let one stage (1) be designed for a single-pole response,

$$A_I = H_1 H_2 \frac{p + z_1}{(p + c_1)(p + z_1)} \times \frac{p + z_2}{p^2 + a_2 p + b_2};$$

then for $c_1 = z_2$,

$$A_I = \frac{H_1 H_2}{p^2 + a_2 p + b_2}.$$

This current-gain expression shows that the bandwidth is determined only by the second interstage, and the gain by both interstage networks. The two roots of the denominator polynomial may be varied to obtain the shape of response desired, maximally flat magnitude, linear phase, and other results.

For three stages, the final form of the gain is

$$A_I = \frac{H_1 H_2 H_3}{(p^2 + a_2 p + b_2)(p + c_3)}.$$

To generalize on this scheme, assume a product of n shunt-peaked interstage terms

$$A_I = \prod_{i=1}^{n} \frac{H_i (p + z_i)}{p^2 + a_i p + b_i}.$$

List of symbols

C_c	= depletion-layer capacitance of the collector-base junction
r_b'	= extrinsic base resistance of transistor
r_e	$= \frac{kT}{qI_e} = \frac{0.026 \text{ volt}}{I_e}$, intrinsic emitter resistance (where I_e is the dc emitter current)
R_1	$= (B_0 + 1)(r_e + R_e)$
R_e	= external emitter resistance, unbypassed
R_I	= interstage resistance
L	= interstage inductance
β_0	$= \frac{a_0}{(1 - a_0)}$, or low-frequency current gain of a common emitter stage when the load is a short circuit
ω_β	= frequency at which the common emitter current gain has dropped 3 db from β_0, with a short-circuit load
ω_t	$= \omega_\beta (\beta_0 + 1)$
ω_{3db}	= frequency at which the amplifier response is down 3 db from its low-frequency value
D	$= 1 + \omega_t(C_c + C_{cb})(R_L + r_e + R_e)$, a factor that indicates the degradation of bandwidth because of feedback through C_c and C_{cb} (where C_{cb} is the extrinsic collector-to-base capacitance.)

By proper cancellation of the numerator and denominator factors the overall A_I function can take the form

$$A_I = \left(\prod_{i=1}^{n} H_i\right) \Big/ (p^n + a_n p^{n-1} + b_n p^{n-2} + \cdots + y_n p + z_n),$$

which means that the response function for n stages contains an nth-order polynomial in the denominator.

To determine the relative merit of this design, the resulting bandwidth, as determined by the nth-order denominator polynomial, is multiplied by the low-frequency gain, and this gain-bandwidth product is then compared with that obtained by cascading the same number of transistors in an iterative design. In the iterative design, all stages have the same bandwidth and a single-time-constant form of response.

II. ANALYSIS OF INTEGRAL DESIGN

The band-edge frequency of an nth-order gain function is determined by the shape of the response; for our examples, a maximally flat magnitude response is specified.

A. Two-Stage Amplifier

For the two-stage amplifier, we have

$$A_i = H_1 H_2 / (p^2 + a_2 p + b_2) . \tag{1}$$

For maximally flat magnitude we require

$$a_2^{\,2} = 2b_2 . \tag{2}$$

and the 3-db frequency is

$$\omega_{3\,db} = \sqrt{b_2}\ . \tag{3}$$

The low-frequency gain is expressed by

$$A_i\,(0) = \frac{H_1 H_2}{b_2}\ , \tag{4}$$

and the gain-bandwidth product is

$$A_i\,(0)\,\omega_{3\,db} = H_1 H_2 (b_2)^{1/2}. \tag{5}$$

In terms of the circuit parameters, we have

$$H_1 = \omega_{t(1)}/D_1\ ,$$

$$H_2 = \omega_{t(2)}/D_2\ ,$$

and

$$\omega_{3db} = (b_2)^{1/2} = \left[\frac{\omega_{\beta(2)}}{D_2}\left(\frac{R_{I(2)} + R_1 + r_b'}{L_2}\right)\right]^{1/2}, \tag{6}$$

or

$$A_i(0) = \left(\frac{\omega_{t(1)}}{D_1} \times \frac{1}{\omega_{3db}}\right)\left(\frac{\omega_{t(2)}}{D_2} \times \frac{1}{\omega_{3db}}\right), \tag{7}$$

and

$$A_i(0)\ \omega_{3db} = \left(\frac{\omega_{t(1)}}{D_1} \times \frac{\omega_{t(2)}}{D_2}\right)\ \frac{1}{\omega_{3db}}\ . \tag{8}$$

It will be seen that the gain-bandwidth product for the integrally designed amplifier, Eq. (8), is greater than that of the iteratively designed amplifier with the same bandwidth by the reciprocal of the square of the shrinkage factor, for two stages, approximately a factor of 2.4.

B. Three-Stage Amplifier

In the case of the three-stage amplifier we have

$$A_i = H_1H_2H_3/(p^2+a_2p+b_2)(p+c_3), \tag{9}$$

and

$$p + z_2 = p + c_1 \quad \text{or} \quad z_2 = c_1, \tag{10}$$

and we have

$$(p+z_1)(p+c_1) = p^2 + a_1 p + b_1,$$

and

$$(P+z_3)(P+c_3) = P^2 + a_3P + b_3,$$

or

$$z_1 + c_1 = a_1, \tag{11}$$

$$z_1 \; c_1 = b_1, \tag{12}$$

and

$$z_3 + c_3 = a_3, \tag{13}$$

$$z_3 \; c_3 = b_3. \tag{14}$$

For a maximally flat magnitude, we require

$$a_2 = \sqrt{b_2}, \tag{15}$$

$$c_3 = a_2, \tag{16}$$

and

$$\omega_{3\,db} = (b_2\, c_3)^{1/3}. \tag{17}$$

The low-frequency gain for three stages is then expressed

$$A_i(0) = \frac{H_1 H_2 H_3}{b_2\, c_3}\,, \tag{18}$$

and

$$A_i(0)\,\omega_{3\,\mathrm{db}} = \frac{H_1 H_2 H_3}{(b_2 c_3)^{2/3}}\,. \tag{19}$$

In terms of transistor parameters, we have

$$H_1 = \frac{\omega_{t(1)}}{D_1}\,,$$

$$H_2 = \frac{\omega_{t(2)}}{D_2}\,,$$

and

$$H_3 = \frac{\omega_{t(3)}}{D_3}\,.$$

Also,

$$b_2 = \frac{\omega_{\beta(2)}}{D_2}\left(\frac{R_{I(2)} + R_1 + r_b'}{L_2}\right),$$

$$c_3 = \frac{\omega_{\beta(3)}}{D_3}\left(\frac{R_{I(3)}\, R_1 + r_b'}{R_{I(3)}}\right),$$

and

$$\omega_{3\,\mathrm{db}} = (b_2 c_3)^{1/3}\,;$$

or

$$A_i(0) = \left(\frac{\omega_t(1)}{D_1} \times \frac{1}{\omega_{3\,\mathrm{db}}}\right)\left(\frac{\omega_{t(2)}}{\omega_{3\,\mathrm{db}}} \times \frac{1}{\omega_{3\,\mathrm{db}}}\right)\left(\frac{\omega_{t(3)}}{D_3} \times \frac{1}{\omega_{3\,\mathrm{db}}}\right). \tag{20}$$

and

$$A_1(0)\ \omega_{3\,db} = \left(\frac{\omega_{t(1)}}{D_1}\right)\left(\frac{\omega_{t(2)}}{D_2}\right)\left(\frac{\omega_{t(3)}}{D_3}\right)\left(\frac{1}{\omega^2_{3\,db}}\right). \tag{21}$$

Generalizing, for n stages we apply the formula

$$A_1(0) = \left(\frac{\omega_{t(i)}}{D_i}\ \frac{1}{\omega_{3\,db}}\right)^n. \tag{22}$$

III. ANALYSIS OF ITERATIVE DESIGN

The gain and bandwidth of an iteratively designed amplifier may be derived as follows.

Where the typical interstage gain is

$$a_i = K/(p + p_0). \tag{23}$$

and

$$\omega_{3\,db} = p_0.$$

$$a_i(0)\ \omega_{3\,db} = K, \text{ and } K = \frac{\omega_t}{D}. \tag{24}$$

For n stages cascaded we have

$$a_I = [K/(p + p_0)]^n. \tag{25}$$

and

$$\omega_{3\,db} = p_0 \cdot S. \tag{26}$$

Where we have the shrinkage factor $S = (2^{1/n} - 1)^{1/2}$, (27)

we have

$$a_I(0) = \frac{K}{P_0}^{n} = \left(\frac{\omega_t}{D}\;\frac{1}{\omega_{3\,db}}\right)^{n} S^{n}, \tag{28}$$

and

$$a_I(0)\,\omega_{3\,db} \;\; (\omega_t / D\,\omega_{3\,db})^{n}\;\omega_{3\,db}\,S^{n}. \tag{29}$$

IV. COMPARATIVE THEORETICAL PERFORMANCE

By comparing integral equation (22) and iterative equation (28), we see that the gain of an n-transistor amplifier designed by the integral unit method is S^{-n} times the gain of the iteratively designed one, where both amplifiers have the same overall bandwidth, and where S is the shrinkage factor calculated for n cascaded stages. Table I shows the gain-increase factor S^{-n} for two-, three-, and four-stage integral designed amplifiers, in which

$$\text{Gain bandwidth}_{\text{iterative}} = \text{Gain bandwidth}_{\text{integral}} \times S^{n}$$

for equal bandwidths.

The resulting improvement in gain-bandwidth product indicates that for equal bandwidths the integrally designed amplifier will have a gain that is 2.4 times that of an iteratively designed amplifier using two interstages. For three transistor interstages the gain advantage is a factor of 9.48, and for a four-stage amplifier an impressive factor Of 30.5.

If the compared amplifier designs are simplified to a typical or equivalent interstage of each overall design, the difference between them is the exclusion of the shrinkage factor from the integrally designed amplifier interstage. This indicates an improvement in interstage broadbanding efficiency by the same amount as the gain-bandwidth product of that stage is increased; namely, the shrinkage factor.

V. EXPERIMENTAL VERIFICATION

The procedures for integral designs, developed in detail in Appendices A and B, were used to design the two- and three-stage amplifiers shown in Figs. 1 and 2. Theoretical and experimental performance of the amplifiers are compared in Table II. The agreement between predicted gain and bandwidth, as shown, is as close as experimental accuracy allowed, about ±10%.

Although the design equations yield an exact cancellation between the numerator and denominator terms, the realization of such exactness is not possible because of nonideal elements. The observed behavior of the two amplifiers, Figs. 1 and 2, indicates that considerable error in the cancellation may be tolerated before degradation of the performance results. Inasmuch as the final value of the numerator and denominator terms is determined by adjusting the value of the interstage inductance with a tuning slug while observing either the pulse or frequency response on an oscilloscope, the desired accuracy of cancellation is limited by the method of observation.

The amplifier of Fig. 1 was constructed with a silicon mesa-type transistor, 2N834. To reduce losses in the biasing circuitry a relatively large value of collector supply voltage was selected. However, in designing the second amplifier the selection of voltages was restricted to conform with LRL standards. The use of a lower supply potential necessitated placing the shunt-peaking circuit in the collector supply path rather than in the base. This in turn required the use of appropriate (5.0-kilohm) biasing resistors in the base circuit of the transistors.

The addition of a 39-ohm unbypassed resistance in the emitter lead[5] of the shunt-peak stage desensitizes the circuit performance to transistor parameter changes (series feedback). The use of an unbypassed emitter resistance in no way degrades the attainable performance of the shunt-peaked interstage, and it makes it possible to use arbitrarily selected transistors of the same type without redesign of the amplifier.

The design is most sensitive to changes in r_b' of the transistors, as the value of the canceling term is approximately r_b'/L, and the range of adjustment in L must be sufficient to account for variation in r_b' from one transistor to another. The use of an unbypassed emitter resistance also reduces this sensitivity because the canceling term becomes $(r_b' + R_e)/L$. The available range of output voltage developed into a 50-ohm load for the examples is approximately ± 0.75 v with about 1% linearity.

VI. CONCLUSION

The philosophy of integral design is a useful technique for circumventing the limitation of gain-bandwidth product for multistage amplifiers. A greater gain-bandwidth product results for the integral design of multistage amplifiers because the bandwidth shrinkage factor is eliminated. This factor is defined as the loss in attainable gain-bandwidth product that results from cascading identically (iteratively) designed stages. By eliminating this loss, an appreciable increase in gain can be realized (see Table I), which could result in the use of fewer transistors to realize the same gain-bandwidth product as an iteratively designed amplifier.

Some practical difficulty is encountered with the design because the parameters of the transistors are not accurately known nor uniform from unit to unit. This difficulty can be somewhat reduced by such devices as the external emitter resistance used in amplifier design. The improvement in gain-bandwidth product realized by this design technique more than offsets these difficulties.

ACKNOWLEDGMENTS

I would like to thank D. O. Pederson of the University of California at Berkeley for his help and encouragement in developing this design technique, and the Lawrence Radiation Laboratory Nuclear Instrumentation Development Group, especially Horace G. Jackson, for frequent discussions.

APPENDICES

A. The Integral Design of a Two-Transistor Shunt-Peaked Amplifier

The gain of a typical shunt-peaked interstage may be derived as follows (see Fig. 3):

$$A_i = \frac{i_L}{i_g} = -\frac{\omega_t}{D} \times \frac{p + R_I/L}{p^2 + \left(\frac{R_I + r_b'}{L} + \frac{\omega_\beta}{D}\right) p + \frac{\omega_\beta}{D}\left(\frac{R_I + R_1 + r_b'}{L}\right)} . \tag{A-1}$$

where

$$R_1 = (\beta_0 + 1)\, r_e .$$

$$C_1' = \frac{1}{\omega_t\, r_e} .$$

$$D = 1 + \omega_t (C_c + C_{cb})(R_L + r_e) ,$$

and

$$\omega_t = \omega_\beta(\beta_0 + 1),$$ as stated in Table I.

The condition for cancellation may be determined by dividing the denominator by the numerator to find

$$
\begin{array}{r|l}
 & p + \dfrac{r_b'}{L} + \dfrac{\omega_\beta}{D} \\
\hline
p + \dfrac{R_I}{L} & p^2 + \left(\dfrac{R_I + r_b'}{L} + \dfrac{\omega_\beta}{D}\right) p + \dfrac{\omega_\beta}{D}\left(\dfrac{R_I + R_1 + r_b'}{L}\right) \\
 & \underline{p^2 + (R_I/L)\, p} \\
 & \left(\dfrac{r_b'}{L} + \dfrac{\omega_\beta}{D}\right) p + \dfrac{\omega_\beta}{D}\left(\dfrac{R_I + R_1 + r_b'}{L}\right) \\
 & \underline{\dfrac{\omega_\beta}{D}\left(\dfrac{R_I}{L}\right) + \dfrac{R_1 r_b'}{L^2}} \\
 & \dfrac{\omega_\beta}{D}\left(\dfrac{R_1 + r_b'}{L}\right) - \dfrac{R_I r_b'}{L^2} = 0.
\end{array}
$$

However, the denominator factors into

$$
\left(p + \frac{R_I}{L}\right)\left(p + \frac{r_b'}{L} + \frac{\omega_\beta}{D}\right), \tag{A-2}
$$

provided that

$$
\frac{\omega_\beta}{D}\left[\frac{R_I + r_b'}{L}\right] - \frac{R_I r_b'}{L^2} = 0,
$$

or if

$$
\frac{R_I}{L} = \frac{\omega_\beta}{D}\left[\frac{R_1 + r_b'}{r_b'}\right]. \tag{A-3}
$$

Now consider the case of two integral stages, for which we can derive the gain as follows:

$$A_I = \frac{\omega_{t(1)}}{D_1} \times \frac{\omega_{t(2)}}{D_2} \times \frac{p + R_{I(1)}/L_1}{p^2 + \left(\frac{R_{I(1)} + r_b'}{L_1} + \frac{\omega_{\beta(1)}}{D_1}\right) p + \frac{\omega_{\beta(1)}}{D_1}\left(\frac{R_{I(1)} + R_1 + r_b'}{L_1}\right)}$$

$$\times \frac{p + R_{I(2)}/L_2}{p^2 + \left(\frac{R_{I(2)} + r_b'}{L_2} + \frac{\omega_{\beta(2)}}{D_2}\right) p + \frac{\omega_{\beta(2)}}{D_2}\left[\frac{R_{I(2)} + R_1 + r_b'}{L_2}\right]} . \qquad \text{(A-4)}$$

For cancellation we have

$$\frac{R_{I(1)}}{L_1} = \frac{\omega_{\beta(1)}}{D_1}\left[\frac{R_1 + r_b'}{r_b'}\right] , \qquad \text{(A-5)}$$

and

$$\frac{R_{I(2)}}{L_2} = \frac{r_b'}{L_1} + \frac{\omega_{\beta(1)}}{D_1} . \qquad \text{(A-6)}$$

The condition for maximally flat magnitude is

$$\frac{R_{I(2)} + r_b'}{L_2} + \frac{\omega_{\beta(2)}}{D_2} = \left[\frac{2\omega_{\beta(2)}}{D_2}\left(\frac{R_{I(2)} + R_1 + r_b'}{L_2}\right)\right]^{1/2} . \qquad \text{(A-7)}$$

But we have

$$\omega_{3\,db} = \left[\frac{\omega_{\beta(2)}}{D_2}\left(\frac{R_{I(2)} + R_1 + r_b'}{L_2}\right)\right]^{1/2} ; \qquad \text{(A-8)}$$

Then

$$A_I = \frac{\omega_{t(1)}}{D_1} \times \frac{\omega_{t(2)}}{D_2} \times \frac{1}{p^2 + \left(\frac{R_{I(2)} + r_b'}{L_2} + \frac{\omega_{\beta(2)}}{D_2}\right) p + \frac{\omega_{\beta(2)}}{D_2}\left[\frac{R_{I(2)} + r_b' + R_1}{L_2}\right]},$$

and

$$A_I(0) = \frac{\omega_{t(1)}}{D_1} \times \frac{\omega_{t(2)}}{D_2} \times \frac{1}{\omega_{3\,db}{}^2} \qquad \text{(A-9)}$$

A systematic design technique now appears in which we successively

(a) pick a bandwidth $(\omega_{3\,db})$ for the amplifier, or pick á gain, and then from Eq. (A-9) find the bandwidth;

(b) use the shape-constraint equation (A-7),

$$\frac{R_{I(2)} + r_b'}{L_2} + \frac{\omega_{\beta(2)}}{D_2} = \sqrt{2}\ \omega_{3\,db},$$

and Eq. (A-8), the bandwidth equation, to determine $R_{I(2)}$ and L_2;

(c) use these data in turn to solve Eqs. (A-5) and (A-6) for $R_{I(1)}$ and L_1.

There is an additional degree of freedom in the design that allows some flexibility in selecting components. This freedom results from varying $\beta_0 r_e$, since $r_e = kT/qI_e$, by changing I_e. These equations assume that the transistors, ω_t, ω_β, r_b', C_c, and the optimum biasing conditions, I_e, V_{ce}, have been specified.

If we include an unbypassed emitter resistance R_e, to stabilize the design (see Appendix B), the design equations then become

(a) from (A-9),

$$A_i(0) = \frac{\omega_{t\,1}}{D_1} \times \frac{\omega_{t\,2}}{D_2} \times \frac{1}{\omega_{3db}{}^2};$$

(b) from (A-7) and (A-8),

$$\frac{R_{I_2} + r_{b_2}' + R_e'}{L_2} + \frac{\omega_{\beta_2}}{D_2} = \sqrt{2}\ \omega_{3\,db},$$

$$\frac{\omega_{\beta_2}}{D_2}\left[\frac{R_{I_2} + r_{b_2}' + (\beta_{0_2} + 1)\,R'_E}{L_2}\right] = \omega_{3db}^2 .$$

and (C) from (A-5) and (A-8),

$$\frac{R_{I_1}}{L_1} = \frac{\omega_{\beta_1}}{D_1}\left[\frac{r_{b_1}' + (\beta_{0_1} + 1)\,R_E'}{r_{b_1}' + R_E'}\right]$$

and

$$\frac{R_{I_2}}{L_2} = \frac{r_{b_1}' + R'_E}{L_1} + \frac{\omega_{\beta_1}}{D_1} .$$

Let us assume an amplifier to be constructed from two 2N834 transistors to have a bandwidth of 75 Mc. The transistor parameters are as follows.

	β_0	f_t (Mc)	r_b' (Ω)	$C_c + C_{cb}$ (pf)	I_e (ma)	V_{ce} (volts)
Q_3	54	500	90	4.0	20	5.0
Q_2	46	460	55	4.0	20	5.0

To obtain a D factor assume R_L of Q_2 is r_b' of Q_3, R_L of Q_3 is 50 Ω.

Then $D_3 = 1 + \omega_t(C_c + C_{cb})\,(R_L + R_E + r_e)$

$= 1 + 2\pi\,(500\times 10$ [illegible] $0^{-12})\,(50 + 40)$

$= 1 + 1.1 = 2.1,$

$D_2 = 1 + 2\pi\,(460\times 10^6)\,(4.0\times 10^{-12})\,(90 + 40)$

$= 1 + 1.5 = 2.5.$

then substitute into the design equations

(a) $$A_1(0) = \left(\frac{460}{(2.5)(75)}\right)\left(\frac{500}{(2.1)(75)}\right) = 7.8$$

for $$\omega_{3\,db} = 2\pi \times 75 \times 10^6 = 4.7 \times 10^8;$$

(b) $$\frac{R_{I_2} + r_{b_2}' + R_E'}{L_2} = \sqrt{2}\ \omega_{3\,db} - \frac{\omega_{\beta_2}}{D_2}$$

$$= (1.414)(4.7\times 10^8) - 0.25\times 10^8 = 6.41\times 10^8$$

and $$\frac{R_{I_2} + r_{b_2}' + (\beta_{0_2} + 1) R_E'}{L_2} = \frac{\omega_{3\,db}^2}{\frac{\omega_{\beta_2}}{D_2}} = 88.\times 10^8,$$

or $$\frac{\beta_{0_2} R_E'}{L_2} = 88\times 10^8 - \frac{R_{I_2} + r_{b_2} + R_E'}{L_2} = 81.4$$

$$L_2 = 0.23\,\mu h$$

$$R_{I_2} = (6.62)(23.) - (55+40) = 56.\ \Omega;$$

(c) for cancellation,

$$\frac{R_{I_2}}{L_2} = \frac{r_{b_3}' + R_E'}{L_3} + \frac{\omega_{\beta_3}}{D_3}.$$

$$L_3 = \frac{r_{b_3}' + R_E'}{\frac{R_{I_2}}{L_2} - \frac{\omega_{\beta_3}}{D_3}}$$

$$= \frac{90 + 40}{\frac{56}{0.23} - 27.7} \times 10^{-6} = 0.60\mu h.$$

$$\frac{R_{I_3}}{L_3} = 27.7\times10^6 \left[\frac{90 + (56+1)(40)}{90 + 40}\right].$$

$$R_{I_3} = 300\ \Omega .$$

The measured response showed a gain of 6.3 and a bandwidth of 85 Mc. A schematic of this amplifier, including a common base stage (Q_1) at the input for matching the source impedance, is shown in Fig. 1. The loss in low-frequency gain due to the biasing resistances can be calculated as $(\frac{2.0\times10^3}{2.3\times10^3} \times \frac{2.0\times10^3}{2.06\times10^3} =)\ 0.845$, or a calculated gain of $[(.845)(7.8) =]$ 6.6.

B. The Integral Design of a Three-Transistor Shunt-Peaked Amplifier

In order to operate the transistors at optimum emitter bias current while still maintaining the freedom to vary $\beta_0 r_e$, the input resistance of the transistor, a small unbypassed resistance (R_E) is included in the emitter lead. The equivalent circuit is represented schematically in Fig. 4.

The gain can be derived as follows:

$$A_i = \frac{\omega_t}{D}\ \frac{p + R_I/L}{p^2 + \left[\frac{R_I + R_E' + r_b'}{L} + \frac{\omega_\beta}{D}\right] p + \frac{\omega_\beta}{D}\left[\frac{R_I + r_b' + \frac{(1)}{1-a_0} R_E'}{L}\right]}$$

in which

$$D = 1 + \omega_t (C_c + C_{cb}) (R_L + R_E').$$

We now consider the case of three stages, for which we derive the gain as follows:

$$A_I = \frac{\omega_{t(1)}}{D_1} \times \frac{\omega_{t(2)}}{D_2} \times \frac{\omega_{t(3)}}{D_3}$$

$$\times \frac{p + R_{I(1)}/L_1}{p^2 \left(\frac{R_{I(1)} + R_E' + r_b'}{L_1} + \frac{\omega_{\beta(1)}}{D_1}\right) p + \frac{\omega_{\beta(1)}}{D_1} \left(\frac{R_{I(1)} + r_b' + \left(\frac{1}{1-a_0}\right) R_E'}{L_1}\right)}$$

$$\times \frac{p + R_{I(2)}/L_2}{p^2 + \left(\frac{R_{I(2)} + R_E' + r_b'}{L_2} + \frac{\omega_{\beta(2)}}{D_2}\right) p + \frac{\omega_{\beta(2)}}{D_2} \left(\frac{R_{I(2)} + r_b' + \left(\frac{1}{1-a_0}\right) R_E'}{L_2}\right)}$$

$$\times \frac{p + R_{I(3)}/L_3}{p^2 + \left(\frac{R_{I(3)} + R_E' + r_b'}{L_3} + \frac{\omega_{\beta(3)}}{D_3}\right) p + \frac{\omega_{\beta(3)}}{D_3} \left(\frac{R_{I(3)} + r_b' + \left(\frac{1}{1-a_0}\right) R_E'}{L_3}\right)}$$

For cancellation we have

$$\frac{R_{I(1)}}{L_1} = \frac{\omega_{\beta(1)}}{D_1} \left[\frac{\beta_0 R_E' + r_b'}{R_E' + r_b'}\right], \qquad \text{(B-3)}$$

$$\frac{R_{I(2)}}{L_2} = \frac{\omega_{\beta(2)}}{D_2} \left[\frac{\beta_0 R_E' + r_b'}{R_E' + r_b'}\right], \qquad \text{(B-4)}$$

and

$$\frac{R_{I(3)}}{L_3} = \frac{r_b' + R_E'}{L_2} + \frac{\omega_{\beta(2)}}{D_2}. \qquad \text{(B-5)}$$

Then we can derive

$$A_I = \frac{\left(\omega_{t(1)}/D_1\right)\left(\omega_{t(2)}/D_2\right)\left(\omega_{t(3)}/D_3\right)}{\left[p^2 + \left(\frac{R_{I(3)} + r_b' + R_E'}{L_3} + \frac{\omega_{\beta(3)}}{D_3}\right) p + \frac{\omega_{\beta(3)}}{D_3}\left(\frac{R_{I(3)} + r_b' + R_E'}{L_3}\right)\right]\left[p + \frac{r_b' + R_E'}{L_1} + \frac{\omega_{\beta(1)}}{D_1}\right]} \tag{B-6}$$

For a maximally flat magnitude we have

$$\frac{R_{I(3)} + r_b' + R_E'}{L_3} + \frac{\omega_{\beta(3)}}{D_3} = \left[\frac{\omega_{\beta(3)}}{D_3}\left(\frac{R_{I(3)} + r_b' + R_E'}{L_3}\right)\right]^{1/2} \tag{B-7}$$

$$= \frac{r_b' + R_E'}{L_1} + \frac{\omega_{\beta(1)}}{D_1}, \tag{B-8}$$

and

$$\omega_{3db} = \left[\left\{\frac{\omega_{\beta(3)}}{D_3}\left(\frac{R_{I(3)} + r_b' + R_E'}{L_3}\right)\right\}\left\{\frac{r_b' + R_E'}{L_1} + \frac{\omega_{\beta(1)}}{D_1}\right\}\right]^{1/3} \tag{B-9}$$

There are six unknowns (R_i and L for each stage) and six equations (B-3, B-4, B-5, B-7, B-8, and B-9); therefore a solution is only a question of algebra. As in the two-transistor example, the initial step in the design is to specify the bandwidth, or to calculate the bandwidth from the specified gain and the gain-bandwidth product, which is

$$A_I(0) = \left(\frac{\frac{\omega_{t(1)}}{D_1}}{\omega_{3db}}\right)\left(\frac{\frac{\omega_{t(2)}}{D_2}}{\omega_{3db}}\right)\left(\frac{\frac{\omega_{t(3)}}{D_3}}{\omega_{3db}}\right). \tag{B-10}$$

or

$$A_I(0)\ \omega_{3db} = \left(\frac{\omega_t}{D}\right)^3 \left(\frac{1}{\omega_{3\,db}}\right)^2 .$$

An amplifier was constructed following the above design equations (see Fig. 2), with a specified bandwidth of 50 Mc. The gain calculated from Eq. (B-10) is 76 and the measured gain was 66, the difference resulting from losses in the bias circuitry (i.e., the 5 k base resistor). When the resulting 0.85 loss factor is included, the gains compare quite well.

The bandwidth was determined from a pulse-rise-time method to be

$$f_{3db} = 0.35/t_r = 0.35/(7.2\times 10^{-9}) = 48 \text{ Mc.}$$

The amplifier comprised three 2N834 transistors, and the system was specified to have a bandwidth of 50 Mc. The properties of the transistors were as shown in the table.

	β_0	f_t (Mc)	r_b'	C_c	D	Gain correction from biasing resistors
Q_2	50	420	60	4 pf	2.13	0.96
Q_3	60	480	60	4 pf	2.13	0.90
Q_4	50	450	60	4 pf	2.13	0.985

These properties yield a calculated gain

$$A_i = \left(\frac{450}{2.13\times 50}\right)\left(\frac{450}{2.13\times 50}\right)\left(\frac{420}{2.13\times 50}\right) = 76,$$

which, when the loss from the biasing resistors is included, gives us, for amplifier gain,

$$76\times(0.96)(0.90)(0.985) = 66.$$

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Table I. Gain increase factors for two-, three-, and four-stage amplifiers

Stages (n)	S	S^{-n}
2	0.64	2.4
3	0.49	8.48
4	0.425	30.5

Table II. Comparison of calculated and measured performances of the amplifiers (Figs. 1 and 2).

n	Gain		Bandwidth (Mc)	
	Calculated	Measured	Calculated	Measured
2	6.6	6.3	75	85
3	66	66	50	48

FIGURE LEGENDS

Fig. 1. Schematic diagram of a two-stage integrally designed amplifier.

Fig. 2. Schematic diagram of a three-stage integrally designed amplifier.

Fig. 3. Typical shunt-peaked interstage network.

Fig. 4. Equivalent circuit with unbypassed resistance R_E.

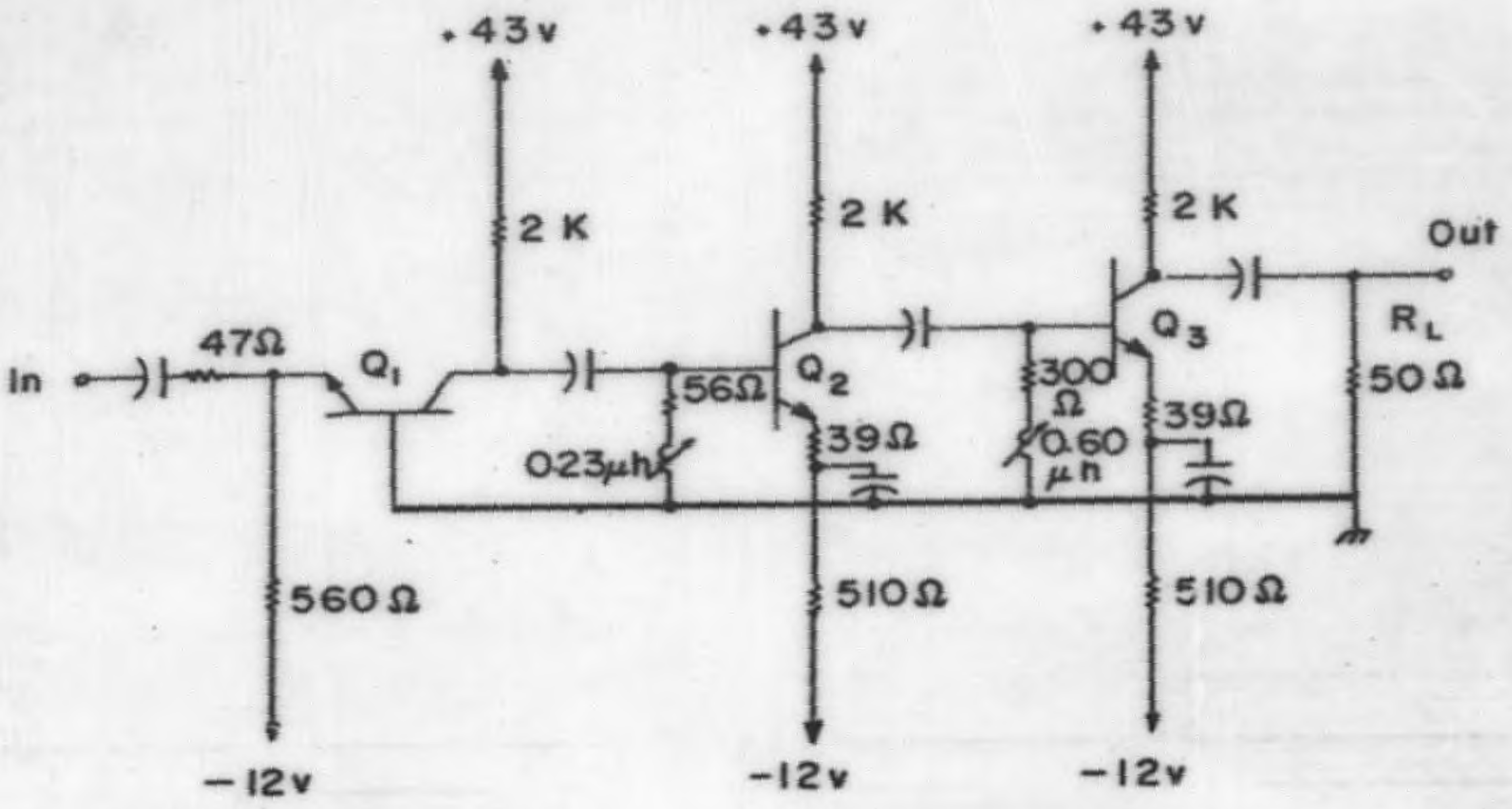

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Fig. 4

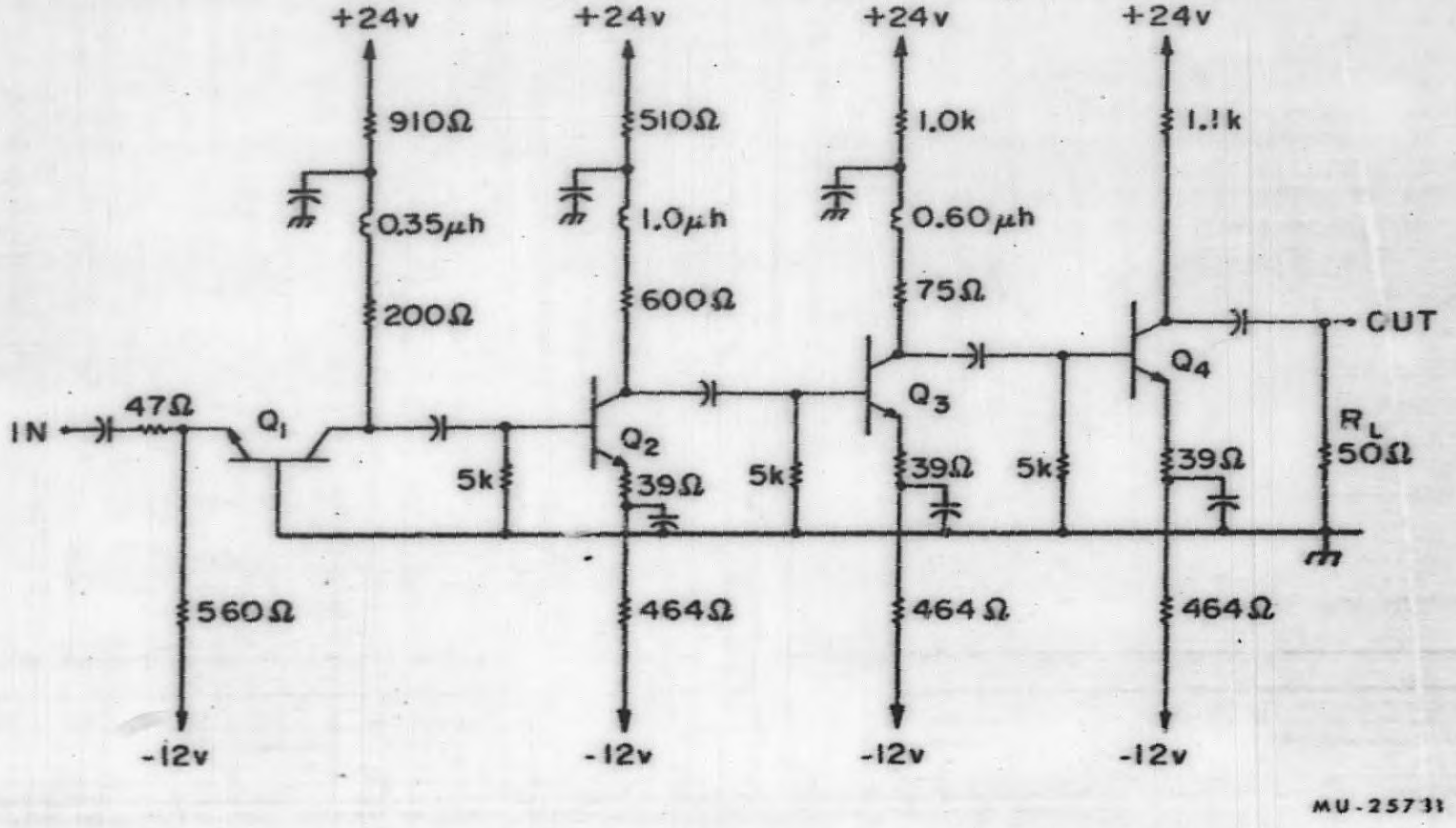
+24v
+24v
+24v
+24v
910Ω
510Ω
1.0k
1.1k
0.35μh
1.0μh
0.60μh
200Ω
600Ω
75Ω
OUT
Q1
Q2
Q3
Q4
IN
47Ω
5k
5k
5k
39Ω
39Ω
39Ω
RL
50Ω
560Ω
464Ω
464Ω
464Ω
-12v
-12v
-12v
-12v
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Fig. 2

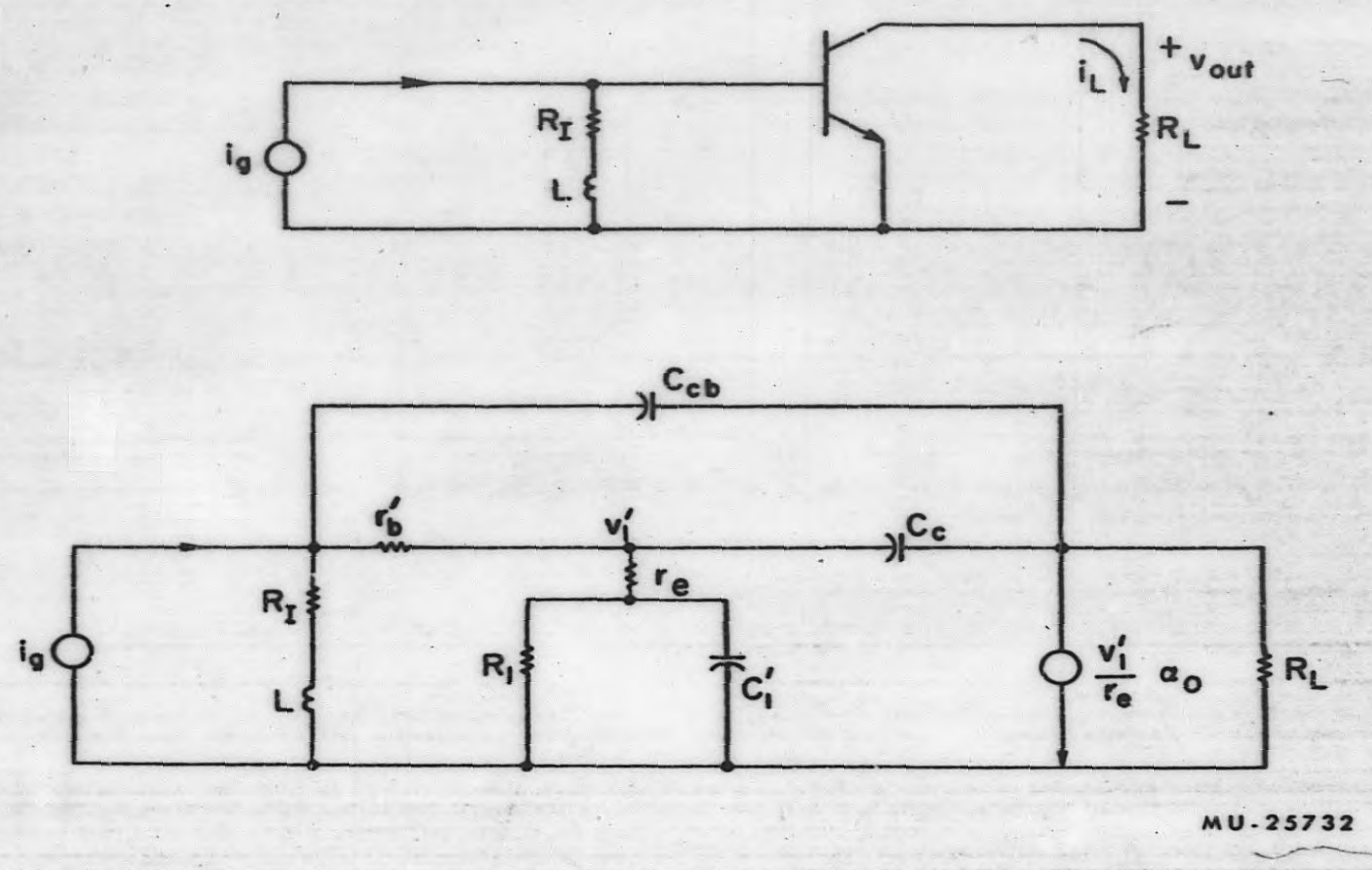

Fig. 3

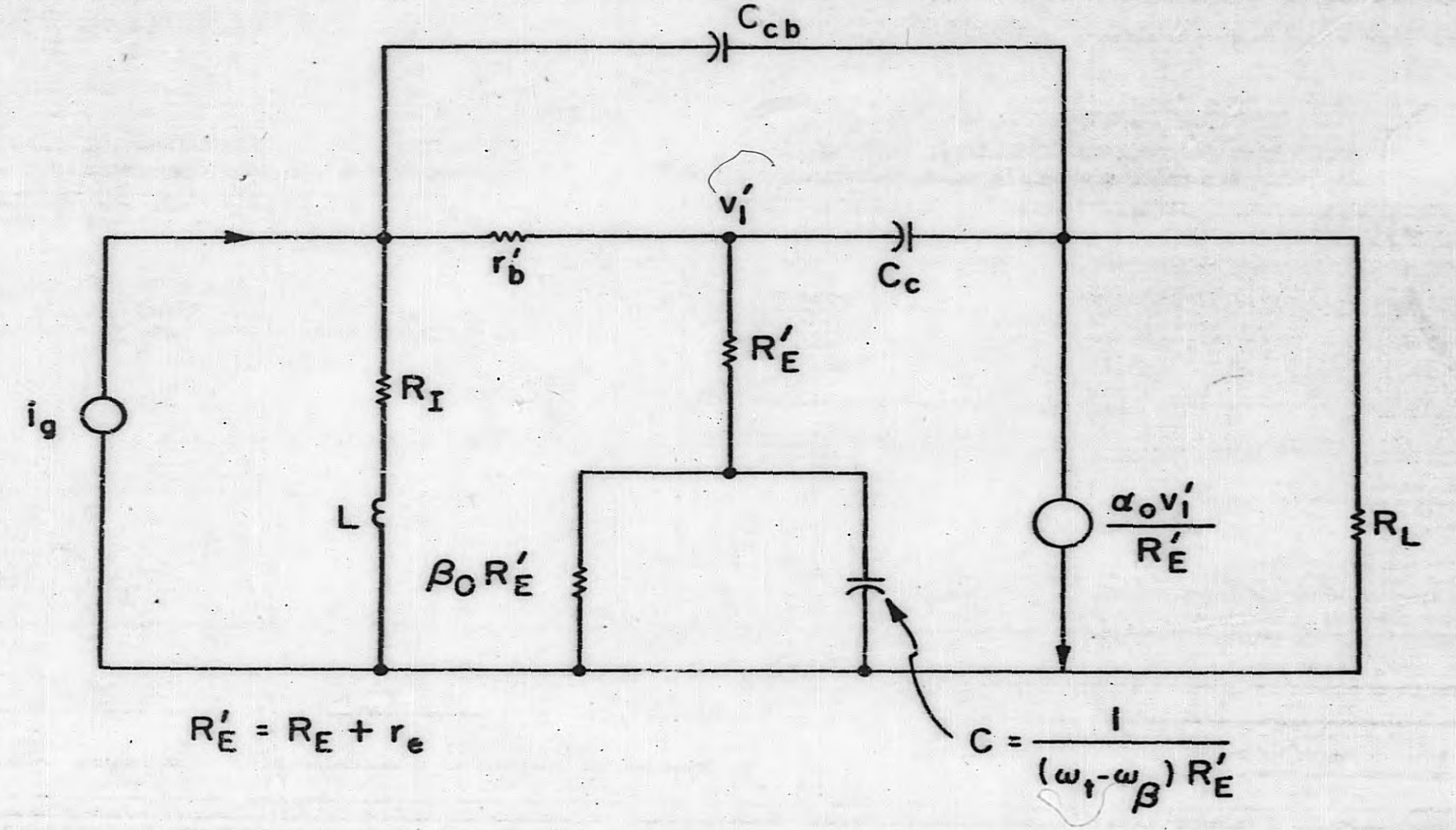

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Fig. 4

END