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DOE/JPL/954865-2

ARRAY AUTOMATED ASSEMBLY TASK, LOW COST SILICON SOLAR
ARRAY PROJECT. PHASE 2

Quarterly Technical Report No. 2, January—March 1978

By
Gregory T. Jones
Sang S. Rhee
Kimberly L. Allison

MASTER

Work Performed Under Contract No. NAS-7-100-954865

Sensor Technology, Incorporated
Chatsworth, California

U.S. Department of Energy

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ARRAY AUTOMATED ASSEMBLY TASK
LOW COST SILICON SOLAR ARRAY PROJECT
PHASE 2

QUARTERLY TECHNICAL REPORT NO. 2

Gregory T. Jones, Sang S. Rhee,
Kimberly L. Allison

January - March, 1978

MASTER

Contract No. NAS-7-100-954865

"The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE".

Sensor Technology, Incorporated
Chatsworth, California

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PREFACE

The information presented in this report, represents the work performed from January 1st, 1978 through March 31st, 1978 by Sensor Technology, Inc., in Chatsworth, California. The program is directed by Sang S. Rhee. Principal contributors include Gregory T. Jones, Kimberly L. Allison, Sanjeev Chitre, Charles Snyder, Louis R. Rosinski, Nelson E. David, and A. PeBenito.

The JPL Technical Program Manager is Paul Alexander.

ABSTRACT

Work on Phase 2 of the Array Automated Assembly Task, a low-cost silicon solar array project, was conducted during this quarter. This project covers the period from January 1st, 1978 through March 31st, 1978.

Data was gathered and analysis continued on thirteen process task groups. Four tasks were completed. A solar cell test data acquisition system was constructed. The data acquisition equipment showed that an automated system for collecting data on solar cell electrical performance is very useful and suitable for large scale production. The application of plasma etching to thick film resist removal was studied and was not found to be a promising process technique. The laser trimming and holing operation was completed. The computer program, flow chart and operations manual was delivered. Wafer surface preparation experiments were completed and a SAMICS study performed. The new texturizing system would add 6.39 cents to the price of a cell which was in excess of the 1986 IPEG goal by about a factor of three. This high cost was primarily due to pretexturizing chemical cleaning solution costs which account for 80% of the total material costs for this process sequence. A preliminary

investigation into three types of scanning procedures has led to the selection of the laser scanning method for the detection of mechanical defects in silicon solar cells. The present technology in thick film printing has been reviewed and some of the anticipated problem areas have been investigated. A company was contacted in order to provide information concerning the low pressure vapor metal deposition techniques; however, their response to our request for a quotation was negative. The current technology in the field of plasma silicon nitride deposition was studied and a preliminary cost estimate was performed for the purpose of identifying the most advantageous method. A new moderately sized system for the sequential plating of silicon wafers has been designed and found to be conducive for our automation requirements. Technical information pertaining to the spray on dopant and drying system was obtained. The solar cell interconnection method which uses a copper clad Kapton sheet without overlay was designed. A preliminary flexible printed circuit sheet for the 2' x 4' module was drawn and the fabrication of a design feasibility model which would demonstrate the viability of the flexible printed circuit sheet is currently underway.

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INTRODUCTION

The automated process sequence is being investigated in seventeen groups. The process groups, which are not in sequential order, each cover a number of process steps. Analysis of each process step will be performed in one of these groups. Each group is discussed in the technical section of this report. A SAMICS report will be made after our analysis of each process group is complete. The SAMICS method used by Sensor Technology is shown as an example for task group number four on wafer surface preparation. Data was gathered and analysis continued on thirteen process groups during this quarter. They are discussed below,

II. TECHNICAL DISCUSSION

A. Process Group Summaries

1. Cell Test Data Acquisition

A solar cell test data acquisition system was constructed during this quarter. This piece of equipment is designed to measure the electrical performance of solar cells for use in evaluation of cell quality and suitability for module assembly. The cell test data acquisition system will sample the Xenon solar simulator at 100 mW/cm^2 , and automatically record the cell short circuit current (I_{sc}), open circuit voltage (V_{oc}), current at a predetermined voltage (I_v), and the cell current (I_{cell}) and voltage (V_{cell}). This equipment has shown that an automated system for collecting data on solar cell performance is very suitable for module assembly. A continuation of this data acquisition for solar cells and an extension to include solar cell modules for large scale automation will be performed in Task 13 and a SAMICS study will be made on that task.

2. Plasma Etching of Resist

Plasma etching is a popular process in semiconductor industries and is reportedly more economical than standard chemical methods. Its applicability extends throughout the following five areas: (1) silicon oxide or silicon nitride etching, (2) photoresist etching

up to 2 um thickness (3) silicon surface cleaning (4) removal of silicon splatter resulting from laser-scribing and (5) making higher resolution opening photolithography.

No manufacturer to date, has made any attempt to apply this method towards the removal of thick film resist. The major reason for this is simply that the process is much too slow to effect the removal of a thick film resist which is approximately 5 mils thick. Consequently, no etching rate data has been made available for thick film resist. If it is assumed that the etching rate of photoresist is identical to that of the thick film resist, this would imply that an 8000 Å thick film can be removed within 15 minutes as claimed by LFE Corporation's (Waltham, Massachusetts) PDS-504-AP(4) Model and thus the required process time for a 5 mil thick resist which is used in the photovoltaic industry will be approximately 40 hours.

In view of this result, the application of plasma etching to thick film resist removal does not look promising in the near future and no further study will be performed for this task.

3. Laser Trimming and Holing Operation

The laser trimming and holing operation was defined through a quotation sent to us by Quantronix Corporation. The negotiation for procurement of a Laserscribe Computer program for sequentially trimming a hexagon and cutting a central hole from a round silicon wafer has been successfully completed. Programming of Quantronix Corporation's Model 603 Laserscribe with a logic board and study of a Laserscribe system for higher throughput will be made. A software flow chart and operating procedures outline for a combined hexagon and central hole program is now available. The hexagon/circle computer program consists of three main features. A special servo program permits motion of the table in straight line segments at arbitrary angles thereby generating hexagonal and circular patterns with respect to the X-Y axes. A special monitor program produces the appropriate position coordinates and velocity data. Special hardware enables the above patterns to be produced with accuracy at high speeds. The holing operation may occur through either of two options. In one, only the hole is generated. In the other, a scribed hexagon is produced along with a central hole. In order to fabricate central holes of 0.1 to 0.5 inches

in diameter, a chuck with a circular moat will be required. A logic board for storing the hexagon and central hole program will be fabricated. This action has been necessitated due to the limited logic board space on our present logic board which stores only a hexagon scribing program.

4. Wafer Surface Preparation

The present wafer surface preparation process equipment was modified to process a sample volume of silicon wafers. Jigs, carrier baskets and rinse/spin dryer buckets were procured. Experiments were completed this month. A summary of the wafer surface preparation process is presented below:

The wafer surface preparation process consists of five steps. They are (1) wafer surface cleaning, (2) surface macrostructure etching, (3) four stage cascade rinse, (4) surface macrostructure final cleaning, and (5) final rinse/spin dry.

Ninety millimeter diameter, Czochralski (100) as cut, round silicon wafers were procured and sample inspected for experimentation. They were manually placed into cassettes which hold twenty-five wafers. Four cassettes or one hundred silicon wafers were manually loaded into a carrier basket ready for the first process step.

The first step in the wafer surface preparation process consists of a two stage wafer surface cleaning procedure. The silicon wafers are placed into a hot trichlorethylene for five minutes (preferably in an ultra-sonic tank) followed by a 5 minute methanol dip. This process step cleans any organic contaminants off the wafer surfaces which might otherwise impede surface macro-structure etching step.

The second step is the wafer surface preparation process is surface macrostructure etching. The carrier basket containing the silicon wafers is introduced into an ultrasonic stainless steel tank which has been filled with a 10% solution by weight of NaOH to deionized water at $85^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Suspended in the tank is a nitrogen bubbler system which is designed to agitate the solution in addition to the ultrasonics. Approximately 10 liters per minute of nitrogen gas is required for the bubbler designed by Sensor Technology, Inc. It is to be noted that the design and the placement of the bubbler with respect to the silicon wafers determines the consistency of the surface macrostructure etching process. A large amount of nitrogen bubbles which are small in diameter contribute to uniform surface macrostructures. The process time is approximately five minutes which will vary according to the amount of silicon particles and contaminants in the NaOH solution.

The carrier baskets are manually removed from

the surface macrostructure etching tank and placed into the first ultrasonic stage of a four stage cascade rinse system which make up the third step in wafer surface preparation process. The carrier baskets remain for five minutes in each of the four stages. Hot deionized water flows at a rate of 3.8 liters per minute from the fourth stage where the D.I. water input temperature is $80^{\circ}\text{C} \pm 5^{\circ}\text{C}$ to the first ultrasonic stage where the D.I. water output temperature is $72^{\circ}\text{C} \pm 5^{\circ}\text{C}$. The silicon wafers get progressively cleaner as they move from the first stage to the fourth stage of the cascade rinse system.

The fourth step in the wafer surface preparation process is surface macrostructure final cleaning. The wafer cassettes are manually removed from the cascade rinse and introduced into a 6 HCL: $6\text{H}_2\text{O}_2:50\text{H}_2\text{O}$ mixture at $70^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for five minutes. This solution removes any remaining deposits of sodium hydroxide that might be trapped in the wafer surface macrostructure. The wafers are rinsed off in running D.I. water for five minutes and are now ready for the final step in this process sequence.

The fifth step in the wafer surface preparation process is the final rinse/spin dry. The last remaining wafer surface contaminants in this five minute cycle are removed. The wafers are now ready for the junction formation process.

The wafer surface preparation process demonstration equipment was used to process 100 ninety millimeter diameter silicon wafers for each carrier basket or four cassettes carrying 25 wafers each. The system capability is 200 wafers per process step assuming two layers of 100 wafers each. Therefore, the wafer surface preparation process can manually process 2400 wafers in one hour.

The texturized wafers produced by this process technique have a black antireflective surface; they are uniformly etched and are batch to batch reproducible. The wafer surface preparation process procedure is used to estimate the parameters and costs required by SAMICS for an automated system to meet the 1986 goals. The cost analysis on this process sequence is shown in a separate section on SAMICS.

5. Laser Scanning Inspection

An investigation into three types of scanning procedures was initiated for the purpose of selecting an optimum method for the detection of mechanical failures in photovoltaic cells at test stations.

The first method under consideration was the X-ray scanning method which has a demonstrated capability of detecting mechanical failures. There is however a serious draw-back in this system with regard to its data acquisition method which is required to effect the transition of the system to production line applications. This problem can eventually be overcome but only as the result of extensive study.

The second method is the IR-Micro-Inspection Method developed by Electrophysics in New Jersey. It appears that with this method, the detection of soldering faults is an extremely difficult feat and will consequently be unsuitable for our requirements.

The final method is the laser scanning method. This system is presently employed at the JPL facility, and is used in the detection of hairline cracks in solar cells. This system appears to have favorable prospects, however, its potential optimization and

practicality for production line applications will require further investigation.

After reviewing the above three methods, it has been concluded that only the laser scanning method is within the realm of present day technology, and consequently it will warrant further investigation in order to accurately assess its feasibility for use in production line applications.

6. Wafer Printing

During this quarter, the present technology in thick film printing has been reviewed and some of the anticipated problem areas have been investigated.

The current high-speed automatic thick printing equipment is completely adequate for standard catalog-sold devices such as resistor networks or the panel display industry. A large size silicon solar cell application would however, require a special design in order to achieve any degree of automation.

In order to provide an illustrative example of a typical problem area which would be encountered during the wafer printing process, a discussion concerning the problem of floor space will be presented along with the suggested modifications.

a) Floor Space

The wafer printing process entails the following sequential steps: (1) loading (2) printing (3) leveling

time (4) drying process and (5) unloading.

The printing machine can operate at a potential rate of 7200 wafers/hr. with the restriction that small-sized wafers be used. With the double head feature, it can operate at the potential rate of 7200 wafers/hr., independent of the wafer size. By using the former option, it is found that the required furnaces and dryers will be prohibitively expensive and large. For example, let us assume that a 3.5" wafer is printed at the rate of 7200 wafers/hr., and that the leveling time and IR drying time requires up to five and fifteen minutes respectively. Also it will be assumed that the belt width of the furnace is 3 feet so that ten wafers can be loaded into a row. If this is the case, the required speed of the furnace belt will be 4 feet/min. and the total length of the belt will extend 80 feet. Furthermore the unloading device usually requires a minimum length of 2 feet. By taking into consideration the dimensional aspects of the above components, it is clear that the printing speed is often limited by the required floor space.

This problem will be resolved if the trayoven or overhead proofer which is used extensively in the bakery industry can be applied. This method can be used in conjunction with a multilayer conveyor even

though the packing efficiency is poor in comparison with the belt conveyor. For example, if a 4 layer tray conveyor is used, the overall length will be within the 25 foot range with a total oven height of 5 feet. This arrangement has the beneficial feature of allowing the installation of the drying chamber overhead, thus eliminating the need for excessive bottom floor space which could serve alternate functions. The only difficulty foreseen with this method is the loading and unloading process which will require a special design in order to prevent breakage of the silicon wafers.

b) Wafer Loading and Unloading

There are several varieties of loading devices which are available in today's market such as vibratory bowl feeding, stack-type magazine and shelf-type magazine. The only suitable method found applicable to silicon wafers is the shelf-type magazine. This is the only method which incurs the prevention of contamination or damage to the wafer surface and also protects the cell from breakage due to mishandling. The problem encountered by this method is that the magazine is unable to hold many wafers.

If the printer operates at the rate of 7200 wafers/hr., one magazine will be cured in only 1.5 minutes. Consequently, multiple magazines should be used in either a multiposition shuttle arrangement or in a multiple magazine carousel. Similar problems exist at the unloading station where the printed wafers are to be loaded into carriers which are used in the wafer plating process.

c) Screenware

The typical stainless steel mesh screen with emulsion is capable of enduring between 10,000 and 20,000 printings. Therefore, at the rate of 7200 wafers/hr., the screen will be rendered ineffectual every two hours. Recently a new type of screen has been developed with the capability of performing up to 50,000 printings. As a consequence of this development the problem of screen abrasion is not considered to be a significant deterrent toward the attainment of 1986 production goals.

As discussed above, most of the technology required for high speed printing is already within present-day capabilities. The automation rate of 7200 wafers/hr., will be an easily accessible production standard by 1986. At the present time, the best devices in the market will be selectively chosen to fabricate a high speed printing system and a subsequent cost analysis based on this

system will be performed.

7. Low Pressure Vapor Metal Deposition

A local company was contacted to discuss the low pressure vapor metal deposition technique. A representative from that company came to talk with us and a quotation was requested. The response to the quotation was negative and at this point, no other action has been taken.

8. Silicon Nitride AR Coating

This process will play an integral role in the development of a reduced-cost photovoltaic cell. The current method of silicon monoxide A.R. coating by evaporation is an extremely costly process step due to its low throughput and exorbitant electric power consumption rate. In order to meet future pricing goals, it would therefore be desirable to formulate a new and more efficient A.R.coating method.

One of the most technologically advanced AR coating methods now in existence is silicon nitride coating by means of the plasma deposition method. During this quarter considerable effort has been channeled into the investigation of current technology in the field of plasma silicon nitride deposition, and a preliminary cost estimate has been made in order to identify the most advan-

tageous method.

Four companies are currently involved in the plasma coating area and these include Texas Instruments (T.I.), Advanced Material Technology (AMT), Tegel Corp., and LFE Corp. Among these four representative systems, the T.I. and AMT systems are almost identical, so that only AMT will need to be considered.

Even though numerous parameters are used in the evaluation of the systems, only the most crucial parameters will be discussed below.

a) Comparative Operation and Installation Information

The key process information pertaining to three companies is given in Table 1. It is clear that LFE Corp., maintains a minimal power and gas consumption rate in relation to the other companies. The concentration of silane gas used by the Company A and B systems approaches the 6-8% range as opposed to the LFE system which consumes merely 1.5%.

b) Wafer Throughput

The wafer throughput of each system is a parameter of far-reaching significance. The throughput comparison of the three companies is given in Table 2. This table displays two throughputs; one is indicative of the recharacterizing process, and the other is not. Both the A and B company systems require recharacterizing processes

TABLE 1. Comparative Operation and Information of Silicon Nitride antireflective coating manufacturers.

	<u>LFE</u>	<u>A</u>	<u>B</u>
Power Consumption (Deposition Mode)	4.5 KVA	25.0 KVA	10.5 KVA
Water	Not required	6 GPM	1 GPM
Exhaust	1"	2"	1"
Compressed Air	0.05 ft ³ /hr.	0.2 ft ³ /hr.	0.2 ft ³ /hr.
Deposition Gases	1½% Silane / Ar, House N ₂	Silane, N ₂ ⁽¹⁾ . Ammonia	Silane, N ₂ ⁽¹⁾ , Ammonia
Cleaning	(CF ₄ + O ₂) ⁽²⁾ (3)	CF ₄ ⁽³⁾	CF ₄ + O ₂ + N ₂ ⁽³⁾
Vacuum Pump (main)	1100 l/M	990/6600 l/M	720 l/M

(1) Requires special storage area and safety precautions.

(2) LFE Patented Process U.S. Patent # 3,795,557.

(3) LFE - recommended (minimum) cleaning every 4 hours.

Note: Process must be recharacterized after cleaning. This frequent cleaning is suggested due to significant particulate contamination problems; however, it is only marginally effective.

TABLE 2. Wafer throughput table for silicon nitride antireflective coating manufacturers.

	Max Wafers Per Batch		Batch Cycle (time in min).		Throughput W/O Recharacterizing		Throughput W/Recharacterizing	
	3" dia. 100mm dia.		Without Recharacterizing	With Recharacterizing after Plasma Clean	Wafers/hr. 3"dia.- 100mm dia.		Wafers/hr. 3" dia.-100mm dia.	
LFE	N.A.	N.A.	N.A.	N.A.	40	40	40	40
A	28	28	49	68	34 *	22 *	25 **	16 **
B	35	20	43	62	49 **	28 *	34 **	19 **

Typical throughput
based on customer
feedback

N.A. - Not Applicable

* - Throughput computed without recharacterizing

** - Throughput computed with recharacterizing

due to the severe particulate "sandstorm" caused by the batch system design. Often this recharacterizing process is required for MOS applications.

Even without taking into account the re-characterizing process, the LFE system demonstrates a maximum throughput.

c) Process Costs

The important direct process costs for each process have been estimated and a comparison is shown in Table 3. These estimates do not take into consideration such factors as overhead, floor space, and equipment costs. However, the above estimates can be used to elicit a relative comparison among the different systems. The results indicate that the process costs of the LFE system will be eight times less than that of Company A and three times less than that of Company B. Even though these estimations yield only approximate results, it is apparent that the LFE system will provide comparatively greater cost effectiveness relative to the other systems.

After reviewing the available systems in the current market, the LFE 8000 system has been found to provide the greatest efficiency both in terms of technical ability and operating costs.

TABLE 3. Direct wafer process cost for silicon nitride antireflective coating manufacturers.

	<u>A</u>	<u>B</u>	<u>LFE</u>
GASES	\$.238	\$.063	\$.036
ELECTRICAL POWER	\$.06	\$.02	\$.006
LABOR	\$.06	\$.05	\$.003
	<hr/>	<hr/>	<hr/>
COST PER WAFER	\$.358	\$.133	\$.045
	<hr/>	<hr/>	<hr/>
EQUIPMENT COST *	\$75,000	\$47,000	\$75,000

* Domestic price

Size of wafer is 3 in. ~ 4 in.

The LFE system will now be compared to the present evaporation system. The process costs for both systems have been computed in accordance with the SAMIC's method which makes the underlying assumption that the wafer diameter is 90 mm and the peak watt output is .653 watts. The monetary values are deflated back to 1975 dollars. The results are specified in Table 4. These results appear to indicate that the present evaporation method is twice as expensive as the LFE plasma coating method. It also shows that the evaporation process will require considerable developmental improvements in order to achieve automation goals and reductions in power consumption while the LFE system will need to reduce the equipment cost or else increase the wafer throughput.

Next quarter, effort will be directed towards the investigation of the possibilities for improvement of the LFE system with the specific objective of obtaining a high wafer throughput. In addition, a cell sample will be tested using the LFE 8000 system in order to obtain verification of the quality of the A.R.Coating.

TABLE 4. A.R. Coating cost in 1975 dollars per
Peak Watt for 3.5 inch wafers at
0.653 watts per cell

	Kinney's Evaporation (SiO ₂ Coating)	LFE System 8000 (Silicon Nitride Coating)
MATERIAL	0.0975	0.0596
LABOR	0.2318	0.008
UTILITY	0.1738	0.0010
EQUIPMENT	0.0229	0.1413
FL. SPACE	0.0254	0.0146
BY PRODUCT EXPENSE	0.0110	--
<hr/>		
TOTAL	0.5624	0.2334

9. Wafer Plating

The sequential procedure followed by the wafer plating process is as follows: (1) Removal of silicon dioxide with hydrogen fluoride (2) Prime metal deposition on the wafer (3) Nickel plating (4) D.I. water rinse. It has been determined that although the present wafer plating method is fully compatible with current production standards, it is not amenable for large scale mass production. The present process is inadequately synchronized due to differences in tank size and process times, thereby making an uninterrupted production line difficult to achieve. The heating system of the nickel bath is a direct immersion heater which consumes the nickel solution due to deposition of nickel on the heating element. Since the throughput of the system is about 200 wafers/hr., this figure is clearly unsuitable in terms of the projected 1986 production rate of 7200 wafers/hr. An additional disadvantage lies in the fact that the current method is not a cost-efficient process.

In order to circumvent the disadvantages outlined above, a new moderately sized system capable of automation has been designed which can process 1500 wafers/hr., for a 3.0 to 4.0 inch size wafer and 2500 wafers/hr., for a 2.0 to 2.5 inch wafer size.

The schematic layout of the system is shown in Figure 1. Each tank size has been determined for the specific purpose of allowing standard carriers of all sizes to be used. The first two tanks are small because their process times are faster than the others. Two nickel plating tanks (Tanks 4-12 and Tanks 4-13) are used because the solution consumption rate is large for the nickel solution bath and because heating the solution up to 85°C takes approximately 30 minutes. Therefore, by utilizing two tanks, no interruption in production will occur as the result of solution preparation since at least one tank will always be in an operable condition while the other tank is being replenished.

Initial operation of the process begins when the wafers are placed into a hydrogen fluoride tank (Tank 1) for 30 seconds and then moved to the primer metal bath (Tank 2) for 25 seconds. Next, the wafers are stored in the overflow rinse tank (Tank 3). After repetition of three cycles of this process, a total of six wafer carriers are collected at the overflow rinse tank. These six carriers are then placed on a platform which will travel to the plating tanks

Figure 1. Layout of Nickel Plating System
1500-2500 wafers per hour capacity

DESIGN SPECIFICATIONS

- (1) Depth of Tank = 10" + (3" Exhaust Outlet).
- (2) Material: Polypropylene & Corning Glass.
- (3) All tanks have drain holes connected to sewer except Tank 2 which is connected to reservoir tank (Reservoir Tank = 14" x 16" x 12").
- (4) Exhaust Outlets are needed for Tank 1, 2 & 4. Use air knife or air curtain if possible.
- (5) D.I. Water line should be installed as specified.
- (6) Tank 4 requires indirect dual wall heating system which can heat 30 gallons of water up to 85°C within 20 min. and maintain 85°C $\pm$ 5°.
- (7) Both rinse tanks 3 and 5 require flow meters and control valve for water flow.

where they are processed for five minutes. For the next step, the wafers are moved into a two stage cascade rinse tank (Tank 5) where they will remain for ten minutes.

The standard wafer carriers can hold 25 wafers each and batch quantities of 3.5" wafers will be in units of 150 wafers (250 for 2"-2.5" wafers) with a batch cycle time given in terms of minutes.

The typical features of the system will be:

- 1) An indirect heating system used for the nickel plating tank so that there will be no metal losses in this tank.
- 2) The proper gauges will be installed so that the proper data can be obtained.
- 3) Tank sizes are determined by considering the standard wafer carrier sizes available in the current market.

10. Solder Coating and Flux Removal

Work on this task is scheduled to begin in April. No work has started at this time in the program.

11. Cell Handling for Module Construction

Only preliminary ideas are being discussed at this time in the program. Among these ideas are a wafer flip over technique for the spray on dopant system, automatic wafer handling for the printers, and automatic cell loading and unloading from conveyors to cassettes and from cassettes to conveyors. Pneumatic movers, robots and direct hopper dispensers are being investigated.

12. Laser Trimming and Holing Automation

The study of the application of the laser-scribing process to large scale automation is one of the essential components of this contract. It is necessary that a high level of effort be expended on this process study. Next quarter, a design study will begin for a high throughput system based on 1986 capabilities and a throughput of 7200 cells per hour including equipment and operating cost estimates.

13. Cell and Module Test and Data Storage

This task follows the completion of Task 1 and will begin in April. A minicomputer will be utilized to store and automatically evaluate the solar cell electrical performance data. Sensor Technology under this contract, will use the data developed on the individual cell test and show its application to the test of the full module. This work will involve the interfacing of both the cell and module to the minicomputer.

14. Module Construction Study

The solar cell interconnection method which uses a copper clad Kapton sheet without overlay was designed and is sketched in Figure 2. The P.C. sheet allows one to connect the bottom of one cell through the center hole to the top of the adjacent cell. Fabrication of a design feasibility model which would demonstrate the viability of the flexible printed circuit sheet is currently underway. The model's dimensions are scaled down by a factor of 1/6 relative to that of the actual production size. A model of this size has been determined to be fully adequate for study and demonstration purposes and is also compatible with local manufacturing capabilities. The model will establish

Figure 2. Inter-Connection Method Between Cells
(Copper Claded Kapton Sheet without Overlay)

the following important facts: (1) The configuration of the cell string assembly on a P.C. sheet, (2) Sheet material design verification, and (3) Construction concepts that will evolve.

The model incorporates a hex cell string which utilizes a flexible printed circuit (P.C.). A cell stringing configuration with a notched-out cell-to-cell interconnect tab is being developed. A one mil thick Kapton base material with 2 oz., copper clad on one side was selected over other potential materials for use in the P.C. due to the acceptable soldering temperature characteristics exhibited by Kapton.

A large sector of the current mechanical engineering effort devoted to the module model fabrication task is concentrated on the interconnect tab design application. A basic experiment has been conducted for the purpose of observing (1) the compliance characteristic of the notched-out tab when made to bend upright from a flat position, and (2) under simulated production conditions, the practical feasibility of tab to thread, through an individually dropped cell from an overhead dispenser.

This experiment yielded encouraging results, and further experimentation in this area will be directed towards the simulation of the actual dispensing technique of batched cells from a hopper which will dispense individual cells to their corresponding tabs in the P.C. string matrix.

An X-Y table is currently being designed which will be manually operated in order to demonstrate and evaluate the dispensing approach.

15. Spray on Dopants

The Model 100SC precision spray coating and drying system which is manufactured by Advanced Concepts Equipment, Inc., has been specifically designed for the purpose of spraying thin films of dopants onto silicon wafers. An illustration of this system can be found in Figure 3 . It is capable of processing approximately one sq. ft. per minute, allowing 65% utilization of the conveyor area. In order to provide a more economical system which maintains all the essential controls of sophisticated spray equipment, the support frame has been reconstructed as a bench type model with open access. This system has the capability of providing a high degree of uniformity between successive coating batches due to a

manually selected flush system which cleans the internal passages, filter, and nozzle orifice of the spray gun after the coating cycle. Good thickness and leveling control can be attained as a result of the many overlapping passes of the spray gun. Important parameters such as conveyor speed, coating material flow rate, air or nitrogen flow rate (atomization) and I.R. emitter temperature are fully adjustable. All functions are controlled by conveniently located switches and regulators.

The coating and drying system consists of six components, each of which performs a specific function. The loading station is 12" long and accessible from three sides. The conveyor system will transport manually loaded pellets containing six wafers each, through the spraying operation, drying tunnel and finally onto the unloading station. It is driven by an explosion-proof motor and adjustable speed reducer which will provide conveyor speeds of .3 to 3 feet per minute. The spray chamber houses the air atomization spray gun which can dispense both the coating material and the cleaning solvent as the result of a special

valving arrangement which has the additional advantage of facilitating selective control of the spray/flush sequence. The spray chamber has a rectangular cross-sectional area of 24" by 27" and a height of 16". The conveyor entry and exit openings extend 2" in height. An exhaust plenum located in the lower portion of the spray chamber serves to maintain the cleanliness of the chamber through the use of overspray pans and an exhaust filter. The air dry station located between the spray chamber and the IR/convection drying tunnel, is fabricated from type 304 stainless steel. The special environment maintained in the "air dry" station hinders the formation of "pin holes" on the substrates during the subsequent elevated temperature drying cycle by evaporating the more volatile solvents from the coating. The drying tunnel, is constructed of stainless steel and utilizes both convection and IR radiation to cure the thin-film coating. The infra-red radiation output of the heater panel is independently regulated by a solid state temperature controller which provides a maximum variation of plus or minus 2% of full scale. The heater panel is covered with fiberglass insulation to minimize

thermal radiation leakage to the outside enclosure. Unlike many conventional IR heat sources, this panel heater has been specifically designed for explosion-proof operation in an environment of concentrated organic solvent vapors such as that encountered in the drying tunnel. To minimize the concentration of solvent vapors within the oven tunnel, an air flow of approximately 50 linear feet per minute has been recommended. The spray booth exhaust will be used to facilitate this requirement. The unloading station, like the loading station, is 12" long and accessible from three sides.

A preliminary SAMICS calculation will be performed next quarter in order to determine the cost effectiveness of the spray on dopant and drying system in terms of the projected 1986 pricing goals.

Figure 3. Sketch of spray on dopant system model

16. Conveyorized Dopant Diffusion

Work on this task was scheduled to begin in May. An initial contact was made with a company and a quotation was discussed, but then rejected. Other sources are now being sought.

17. Module Model Fabrication and Materials

Discussions on module model fabrication led to the fact that a solar cell interconnection design was needed prior to any fabrication or automation equipment study. This interconnection design, shown in Figure 2 of task 14 led to a cell string flex circuit model configuration shown in Figure 4 which will be used to study the concept used in the overall cell string flex circuit for the 2' x 4' module shown in Figure 5. The cell string flex circuit model configuration will be sent out next quarter for fabrication.

FIGURE 4. Cell string flex circuit model configuration

Figure 5. Cell string flex circuit
for the 2' x 4' module

△ 2.125 DIA. CUT OUT.

△ TAB CUTOUT.

△ USE 3 MILES KAPTON (OR MYLAR) SHEET CLADDED
BY 2 OZ. PER SQUARE FT. OF COPPER.

NOTE: UNLESS OTHERWISE SPECIFIED

3	JPL4-14-204	END BUS BAR	
2	JPL4-14-203	TERMINAL BUS BAR	
1	JPL4-14-202	INTER-CONNECTION	
ITEM	PART NO.	DESCRIPTION	REQ.
TOLERANCES (UNLESS OTHERWISE SPECIFIED)		SENSOR TECHNOLOGY, Inc. CHATSWORTH • CA. 91311	
DECIMALS .001 ± .010		DRP <i>La...</i> 3-13-77 CHK <i>...</i> 3-15-77 APP <i>...</i> USED ON	
FRACTIONS ± 1/64			
HOLES + .003 - .00			
BREAK ALL SHARP EDGES			
FINISH		TITLE	
		JPL SOLAR MODULE (FLEX CIRCUIT SHEET)	
MATERIAL		SCALE	SIZE
		-	C
		DWG. NO.	SHEET
		JPL4-14-201	1 OF 1

B. SAMICS STUDY

1. Study Plan

a) Preliminary Process Cost Estimate

The primary objective of this project resides in the selection of a cost efficient process which will eventually lead to the 1986 price goal of \$500/kw. It will therefore be necessary to perform the process cost estimation at each process study.

The Solar Array Manufacturing Industry Cost Standard (SAMICS) is intended to be applicable to a cell or module price based on a company level. A particular process is analyzed by assuming that the wafer price is zero and also that the production yield is 100%. This method will provide the net added value of the cell as a consequence of the process under consideration. The process cost estimate that has just been described will be presentable as soon as the process verification test has reached completion.

The equipment to be considered will be in the form of a prototype system which will be operational by 1986. The basic design of the prototype system will depend upon model test results or else it will

be chosen directly from the market if it is currently available there.

b) Final Overall Cost Estimation

After the completion of each process cost estimation, the best cost effective processes will be selected and then used to set up process lines within the company. A standard SAMICS study will subsequently be performed in order to obtain a comparison between the projected product cost in 1986 and the LSA goal prices. In addition, the more cost processes can be identified and then set aside for further study and revision.

2. Definition of Industries

The cost estimation of each process requires the definition of the industry structure and production plan. The 1986 standard industry as specified by SAMICS will be applied towards this cost estimation. As set forth by the 1986 standard industry, the following basic assumptions are made:

(1) CELLCO, which produces the cells from wafers, will share 40% of the total market. MODULECO, which produces the modules from cells, will purchase 100% of CELLCO's product.

(2) CELLCO and MODULCO will maintain a production yield of 96% and 99% respectively.

(3) The industry's product will be the module which has the following specifications:

MODULE SIZE: 2' x 4'

NUMBER OF CELLS: 119 full hexagonal cells

CELL EFFICIENCY: 14.7% after encapsulation

PACKING RATIO: 0.87%

USABLE SILICON PER WAFER: 81%

CELL SIZE: 51.32 cm.² (wafer diameter is 90mm)

MODULE OUTPUT: 90 watts (0.76 watt/cell)

using the above specifications, the output from the company will be:

CELLCO: $\left\{ \begin{array}{l} 278 \times 10^6 \text{ wafers/year} \\ \text{or } 211 \times 10^6 \text{ watts/year} \end{array} \right.$

MODULCO $\left\{ \begin{array}{l} 2.244 \times 10^6 \text{ modules/year} \\ 202 \times 10^6 \text{ watts/year} \end{array} \right.$

This output will apply to each process cost estimation (The definition of the industry is also presented in Format C of SAMICS).

3. Definitions of Process Steps in CELLCO

The CELLCO company will use the ten process steps that are presented in Format B of SAMICS.

Each step is defined as follows:

1) Wafer Surface Preparation (WFSURPR)

This process includes:

- (a) Wafer surface pre-cleaning
- (b) Surface texturization
- (c) Final cleaning and drying

2) Junction Formation (JUNCF)

Two methods will be considered in this process:

- (a) Spray on N^+ and P^+ , dopant drive-in, and removal of any excess dopants.
- (b) $POCl_3$ diffusion and dopant drive-in followed by low pressure vapor metal deposition for back contact.

3) Front surface pattern printing (FSPP)

An automatic printing machine with dry oven will be considered.

4) Electroless Nickel Plating (ELNIPL)

This process will result in plating and cleaning of wafers.

5) Resist Removal (RESMOV)

Two methods will be studied

- (a) Wet chemical resist removal
- (b) Plasma etching

6) Hexagonal laser scribing (HEXLS)

An automated laserscribing system will be considered.

7) Solder flow on grid line (SDFLW)

Solder flow and flux cleaning occur during this process.

8) AR Coating (ARCT)

Two methods will be studied

(A) Chemical vapor deposition

(B) Plasma deposition

9) Cell Testing (CELTEST)

Both electrical and mechanical tests are to be performed during this process. In addition a data acquisition system will store the relevant data and also formulate individual groups based on this data.

10) Packing the cell (PKCELL)

The grouped cells are packed and then loaded into a cartridge for shipping.

4. Wafer Surface Preparation

a) Prototype Design

The schematic diagram of the prototype system is shown in Figure 6. Its design has been based upon model test results.

Figure 6. Automatic texturizing system, 6000 wafers per hour.

The automated system will consist of twelve identical tanks which are all equally spaced and capable of holding twelve wafer carriers that are situated on a platform lift. Each wafer carrier can hold up to 50 wafers so that the amount of wafers which constitute a batch will be 600.

Each batch of 600 wafers will remain in a tank for five minutes and then simultaneously be transferred to the next station during a one minute period. The transfer mechanism utilized in this process step consists of a lifter at each station and an over-hung track conveyor. The conveyor will transfer each platform to its corresponding station and the lifters will move the platforms up and down within the tank. The function of each tank is specified in Figure 6 which serves to approximate the test model. The only deviation of this figure from the actual test model lies in the replacement of the spindryer system, which is an extremely slow process, by a cascade rinse and dryer tunnel. The tunnel drier is composed of two chambers; the first chamber contains a series of nozzles which serve to blow clean air over the wafers and the second chamber slowly cools the wafers in order to relieve wafer surface stresses.

b) SAMICS Calculations

During the preparation of Format A of SAMICS, the following cost estimates have been calculated for the prototype system.

(1) Equipment Costs

TEXTURIZING SYSTEM

Frame and tanks	\$24,000
Supporting tanks	\$4,000
Ultrasonic and Other Accessories	\$12,000
Moving hoist lifter and conveyor	\$14,000
Main drive system	\$6,000
Control system including gauges	\$10,000
Engineering and design	\$10,000
Burden (50%)	\$40,000

TOTAL COST	\$120,000
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DRIER SYSTEM

Tunnel chambers and conveyor	\$10,000
Nozzle, heater and fan control	\$11,000
Burden (50%)	\$10,000

TOTAL COST	\$31,000
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LOADER AND UNLOADER

Two loaders and one conveyor unloader	\$20,000
--	----------

TOTAL SYSTEM COST	\$171,000
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(2) Floor Space

The layout of the prototype system is given in Figure 6 which also specifies the required floor space which amounts to 448.82ft.

(3) Labor

One operator is needed to operate the machine. Four shifts are required in order to operate the plant for a 24 hour period. Two maintenance men who maintain the entire plant, are assumed to be required during each shift. In addition, one production planner per shift will be used.

(4) Utilities and Commodities

The consumption rates of all required chemicals and other materials are obtained from the model test. It has been concluded from a detailed design analysis of the proposed system that the electric power consumption rate from the utility will be extremely large.

All of the relevant data pertaining to the system can be found in Format A of SAMICS. All figures are computed by using the standard process work sheet and the company work sheet. The temporary catalog used in the computations can be found in Table 5. The resulting process costs per wafer in 1986 dollars are presented in Table 6.

C. SAMICS Conclusions for Wafer Surface Preparation

According to IPEG (Interim Price Estimation Guide), the costs incurred during cell fabrication will increase by a factor of 22.4¢/cell. Since ten process steps are required for the fabrication of a cell, the average cost per process step will be 2.4¢. The new texturizing system, which will add 6.39¢ to the price of a cell, is in excess of approximately three times the pricing goal set by IPEG.

From Table 6 it is evident that the predominant cost factor incurred during cell fabrication is overwhelmingly related to material costs which account for almost 60% of the total processing costs. It can therefore be concluded that future breakthroughs in automation alone, will not significantly reduce process costs.

The major reason for the exorbitant material costs seem to lie with the use of trichlorethylene and methanol. These two chemicals, which are used to clean the wafer, contribute to 80% of the total material costs and add 2.3¢ in terms of 1975 dollars to the process cost. The unit prices for these chemicals are obtained from small lot purchases.

In view of the above results, the next plan for this task will be geared towards the identification and evaluation of possible methods for reducing the chemical consumption rate and also a modification in unit prices will be sought.

TABLE 5. SAMICS temporary catalog on wafer
surface preparation Table 1.

	Unit	Price	Inf. Class	Yr.	Type Class
G 1001 D Trichlorethylene	Liter	2.03	C	77	E
G 1002 D Methanol	Liter	1.13	C	77	E
C 2032 D C.L.Compressed Air	Cu.Ft.	0.00634	C	77	C
D 1064 D Rejected Wafer	Wafer	0.0116	F	86	D
D 1176 D Rejected Cell	Cell	0.01158	F	86	D

TABLE 6. Process costs of wafer preparation process

	1986 cents	1975 cents
Equip.	0.32	0.167
Fl. Space	0.1	0.052
T. Lab	0.5	0.260
Mat.	5.44	2.836
Util.	2.91	1.517
<hr/>		
TOTAL	9.27	4.833

The process cost per unit peak watt turns
out to be:

12.257¢/watt in 1986 dollars

6.39 ¢/watt in 1975 dollars

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

A1 Process Referent WFSURPR

A2 Description (Optional) Wafer Surface Preparation

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent SURPRWF

A4 Name or Description Texturized and Surface Clean Wafer

A5 Units Of Measure Wafer

PART 2 – PROCESS CHARACTERISTICS

A6 Output Rate 100 Units (given on line A5) Per Operating Minute

A7 Average Time at Station 98 Calendar Minutes

A8 Process Usage Time Fraction 0.875 Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

	Process Tank	Drier Tunnel	WF HANDL M/C
A9 Component Referent			
A10 Base Price Year For Purchase Price	<u>1978</u>	<u>1978</u>	<u>1978</u>
A11 Purchase Price (\$ Per Component)	<u>\$120,000</u>	<u>\$31,000</u>	<u>\$20,000</u>
A12 Anticipated Useful Life (Years)	<u>7</u>	<u>7</u>	<u>7</u>
A13 Salvage Value (\$ Per Component)	<u>\$10,000</u>	<u>\$3,000</u>	<u>\$1,000</u>
A14 Cost of Removal & Installation (\$/Component)	<u>\$4,000</u>	<u>\$2,000</u>	<u>\$500</u>

Format A: Process Description (Continued)

A14 Process Referent (From Page 1) WFSURPR**PART 4 – DIRECT REQUIREMENTS PER MACHINE**

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
A 2064 D	Factory Space (Type A)	448	Sq.ft.
B 3672 D	Chemical Operator II.	4	Prsn.a yr.
B 3720 D	Inspector (Q.C.)	0.4	"
B 3736 D	Maintenance Mech. II	0.2	"
B 3688 D	Electronics Maint.	0.2	"
B 3256 B	Production Planner	0.057	"

PART 5 – DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Batch	A23 Units
G 1001 D	Trichloroethylene	0.450	Liter
G 1002 D	Methanol	0.450	Liter
E 1600 D	Sodium Hydro Oxide	0.0882	Lbs.
E 1336 D	Hydrogen Peroxide	0.0938	Lbs.
E 1320 D	Hydrochloric Acid (37%)	0.10153	Lbs.
E 1416 D	Nitrogen Gas	0.0783	Cu. Ft.
C 1144	D.I.Water	0.03531	Cu. Ft.
C 2032 D	Clean Compressed Air	100	Cu. Ft.
C 1064 B	Natural Gas	0.01	Cu. Ft.
C 1032 B	Electric Power	0.289	Kw.-Hr.
D 1048 B	Poluted Water	1.676	Gal.
D 1064 D	Rejected Wafer	0.05	Wafer

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED

A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
PWAFER	Wafer from Wafer Co.	0.9995	Wafer/Wafer

Prepared by Sang. S. Rhee Date 3/15/78

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT B

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

COMPANY DESCRIPTION

B1 Company Referent CELLCO

B2 Description (Optional) Standard 1986, Wafer-to-cell company

B3 Product Produced PVCELL

B4		Process	<u>PKCEL</u>
B5	Intermediate Product		<u>TESTC</u>
		Process	<u>CELTEST</u>
	Intermediate Product		<u>ARCC</u>
		Process	<u>ARCT</u>
	Intermediate Product		<u>SDC</u>
		Process	<u>SDFLW</u>
	Intermediate Product		<u>HEXC</u>
		Process	<u>HEXLS</u>
	Intermediate Product		<u>CLNC</u>
		Process	<u>RESREM</u>
	Intermediate Product		<u>NIPLC</u>
		Process	<u>ELNIPL</u>
	Intermediate Product		<u>FSPPW</u>
		Process	<u>FSP</u>
	Intermediate Product		<u>JUNFW</u>
		Process	<u>JUNCF</u>
	Intermediate Product		<u>SURPRWF</u>
		Process	<u>WFSURPR</u>
	Intermediate Product		
		Process	
	Intermediate Product		
		Process	

B6 Purchased Product PWAFER

B7 Supplier Company Reference WAFERCO Percent Supplied 100%

Supplier Company Reference _____ Percent Supplied _____

Prepared by S. S. Rhee Date 3/15/78

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT C

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

INDUSTRY DESCRIPTION

C1 Industry Referent SAMICS - 86

C2 Description (Optional) 1986 STANDARD INDUSTRY

INDUSTRY OBJECTIVE

C3 Industry Result New Photovoltaic Power Capability

C4 Quantity Produced 500 x 10⁶ Peak-Watts/yr.

DESCRIPTION OF THE FINAL PRODUCT OF THE INDUSTRY

C5 Reference PSM Name Packed Solar Module

C6 Production is Measured in (5.56 x 10⁶) Module/yr.

C7 Hardware Performance 90 peak watt/module (C4 per C6)

C8 Product Design Description (Optional) Module with 2' x 4' dimensions
contains 119 solar cells and produces .90 watts at 28°C
and at 100 mW/cm².

MAKERS OF THE FINAL PRODUCT OF THE INDUSTRY

C9 Company Reference MODULCO Market Share 40%

Company Reference _____ Market Share _____

Company Reference _____ Market Share _____

*The remaining companies are smaller than
MODULCO, and are not listed

Prepared by SANG S. RHEE Date 3/15/78

CONCLUSIONS & RECOMMENDATIONS

The work performed on Phase 2 of the Array Automated Assembly Program during this quarter has led to a number of conclusions and recommendations:

The data acquisition equipment has shown that an automated system for collecting data on solar cell electrical performance is very useful and suitable for large scale production. A more indepth study of this data collection technique and data storage is planned for next quarter.

The application of plasma etching to thick film resist removal does not look promising due to the great length of time required to perform this operation. It is thus a highly inefficient technique and should not be pursued for the removal of thick film resist.

Wafer surface preparation process demonstration equipment was used to process 100 ninety millimeter diameter silicon wafers at one time. The texturized wafer produced by this process technique have a black antireflective surface; they are uniformly etched and are batch to batch reproducible. The wafer surface preparation process procedure was used to estimate the parameters and costs required by SAMICS for an automated system

to meet the 1986 goals. The new texturizing system which will add 6.39 cents to the price of a cell, is in excess of the goal by about a factor of three. The high cost is due primarily to material costs and is specifically due to the pretexturizing chemical cleaning solution costs which account for 80% of the total material costs for this process sequence. It is recommended that future efforts be directed toward reducing the chemical cleaning material costs in the wafer surface preparation process.

The laser scanning method is within the capability of present day technology. It appears that this method of determining mechanical defects in silicon solar cells is suitable for large scale production, and it will be studied further to determine its' potential for automation.

Most of the technology required for high speed printing is already within present day capabilities. The automation rate of 7200 wafers per hour will be an easily accessible production standard by the year 1986 and is a highly recommended process.

NEW TECHNOLOGY

A solar cell test data acquisition system has been constructed and its feasibility in terms of production line applications has been evaluated. This equipment has demonstrated that an automated system for collective data on solar cell performance is extremely conducive for module assembly.

A wafer surface preparation process which can manually process 2400 wafers per hour was developed. The new low-cost texturizing system produces silicon wafers that have a black antireflective surface; they are uniformly etched and are batch to batch reproducible. This process sequence is very suitable for large scale automation.

PROGRESS SUMMARY AND PROGRAM PLAN

The progress summary and program plan for Phase 2 of the Array Automated Assembly Task is shown in Figure 7.

Figure 7. Phase 2 Array Automated Assembly Task
Progress Summary and Program Plan

△ planned goals
▲ completed goals