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High-Efficiency Large-Area CdTe Panels

Final Subcontract Report June 1987 - July 1990

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SUMMARY

OBJECTIVES

This is the final technical progress report required under a three year subcontract through the Solar Energy Research Institute, #ZL-7-06031-3.

The objective of this three year effort has been to develop an improved materials technology and fabrication process for limited volume production of 1 ft² and 4 ft² CdS/CdTe photovoltaic modules.

The module stability objective by the end of this three year subcontract was to develop techniques to provide ten year life extrapolation with no greater than 10% degradation.

In order to achieve these efficiency and stability objectives, the research program has been separated into tasks including:

1. Analysis and Characterization of CdS/CdTe Devices
2. Performance Optimization on Small Cells
3. Encapsulation and Stability Testing
4. Module Efficiency Optimization

The major results for each of these tasks are reviewed.

RESULTS AND DISCUSSION

Analysis and Characterization of Devices

Electrical and optical measurements have been performed in order to characterize the effect of process variations on the cell behavior and to better understand the mechanism of current flow at the junction. The highlights of these studies are discussed.

Interface states and/or deep recombination centers affect not only the diode reverse saturation current (J_0) but also the junction collection efficiency and hence the light-generated current (J_L). A preliminary model describing the junction current flow in terms of tunneling and interface recombination has been developed and the highlights will be reviewed.

Studies of the current voltage characteristics have indicated that the series resistance contribution in a high efficiency device is already acceptably low, at 1.0 ohm-cm². The diode quality factor, however, can be inordinately high indicating an unpassivated recombination mechanism. Thus, it is concluded that the major potential for reaching higher efficiencies lies mostly in the reduction of this diode quality factor and not in the ohmic contact to the CdTe.

Device and Module Efficiency Improvement

The structure of a CdS/CdTe polycrystalline thin-film photovoltaic device produced at Photon Energy, Inc. is presented, along with its potential for efficiency improvement. Results on larger area modules having areas of 929 cm² and 3716 cm² are summarized. Module design is described, and projections for future expected module outputs are presented.

Small area devices ($.313 \text{ cm}^2$) cut from $30.5 \text{ cm} \times 30.5 \text{ cm}$ substrates have achieved active area efficiencies of up to 12.3% (25.0 mA/cm^2 short-circuit current, $.783 \text{ V}$ open circuit voltage, 63% fill factor) as measured at SERI. Fill factors as high as 72% have been achieved on other devices at PEI (19.1 mA/cm^2 short circuit current, $.785 \text{ V}$ open circuit voltage, 72% fill factor). It is expected that 14% efficiency will be exceeded on small devices by improving the fill factors on the higher current devices in the reasonably near future. Efficiencies in the 16%-18% are expected to be achieved in the longer term.

Currently, Photon Energy is making cadmium-sulfide/cadmium-telluride modules approximately 929 cm^2 in area which have shown an average efficiency in the active area of over 8% (7.3% aperture area efficiency, 838 cm^2 aperture area). Modules with this efficiency, producing over 6 watts peak power output have been fabricated using the low-volume prototype production line at Photon Energy. The largest known single-substrate CdTe-based photovoltaic module (3716 cm^2) has been produced at Photon Energy, Inc. and was delivered to SERI in 1989. A demonstration project for these 4 ft^2 substrates is a 20 KW photovoltaic system to be installed in Davis, CA for the Photovoltaic for Utility Scale Applications (PVUSA) project.

Encapsulation and Life Testing

Early in the subcontract, PEI abandoned an electrode based on Te due to stability problems. A much more stable, doped-graphite electrode has resulted in good long-term stability when properly encapsulated.

The structural integrity of the encapsulation design and methodology appears in order. Thermal cycling on 1 ft^2 and 4 ft^2 modules from -40°C to 90°C for over 200 cycles has shown no delamination modes. Encapsulated submodules have been life tested for over 270 days with no observable degradation by the SERI Outdoor Reliability and Life Testing Laboratory.

CONCLUSIONS AND FUTURE OBJECTIVES

The efficiency and stability objectives at PEI on CdS/CdTe modules are being addressed. The feasibility of producing 4 ft^2 modules of CdS/CdTe has been shown and requires further effort in order to realize the overall potentials.

In the near future, the greatest potential for efficiency improvement beyond the above results will be realized through further optimization of the window layer and the improvement of the fill factor. In addition, optimization of the absorber material using methods including alloying and doping will likely result in the minimization of the recombination losses and the enhancement of the collection efficiency. In the long term, it is believed that efficiencies in the 16% to 18% range will be achieved.

Future directions in encapsulation will pursue the development of a low-cost hermetic seal, study of barrier coatings applied directly to the film before encapsulation of the backcap, and address corrosion and other long-term reliability issues.

Module output will be increased by uniformity improvement in the deposition process, and by minimizing the loss of active area due to cell division interconnects. Module output is expected to attain 135 watts per square meter in the mid 1990s and over 150 watts per square meter in the long term.

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SECTION 1.0

INTRODUCTION

Since 1984 the developmental effort at Photon Energy, Inc. has been directed toward production of high efficiency, large area, low cost photovoltaic modules based on the CdS/CdTe heterojunction. Beginning in June 1987, Photon Energy, Inc. became involved with a subcontract through the Solar Energy Research Institute. Under this three year subcontract, #ZL-7-06031-3, PEI has undertaken research and development projects to improve our existing technologies and processes to meet both the general DOE objectives and the more specific PEI objectives.

The objective of this three year research effort has been to develop an improved materials technology and fabrication process for limited volume production of 1 ft² and 4 ft² CdS/CdTe photovoltaic modules. The encapsulation objective by the end of this three year subcontract has been to develop techniques to provide 10 year projected field life with no greater than 10% degradation.

In order to achieve these efficiency and stability objectives, the research program was separated into tasks including:

1. Analysis and Characterization of CdS/CdTe Devices
2. Performance Optimization on Small Cells
3. Encapsulation and Stability Testing
4. Module Efficiency Optimization

The major results for each of these tasks are reviewed.

SECTION 2.0

DEVICE STRUCTURE

2.1 History of Structure

During this three-year subcontract Photon Energy has worked with basically two types of device structures. The significant difference between the two is in the thickness of the CdS window layer. The device structure for the earlier type structure (Type I) is given first and a schematic cross section for the structure is shown in Fig. 2-1.

On commercial 3 mm float glass is deposited a 0.6-0.9 μm film of tin oxide by spray pyrolysis, at a deposition temperature of approximately 480°C. A typical resistivity for the tin oxide film is $4\text{-}5.5 \times 10^{-4}$ ohm-cm, and typical extinction coefficients are 900-1200 cm^{-1} . The tin oxide films generally measure 5-9 ohms per square in sheet resistance and 90%-95% transmission relative to the glass substrate over the wavelength range from 520 nm to 850 nm, with a variation of 10%-50% in sheet resistance across a 1 ft^2 substrate.

In the case of a Type I structure, a 6 μm film of CdS is then deposited on top of the tin oxide. Voltage-biased capacitance measurements, using Schottky diodes deposited on this CdS, indicates a carrier concentration on the order of $1 \times 10^{18}/\text{cm}^3$.

Approximately 6 μm of CdTe is then deposited on top of the CdS; the measured hole concentration of the CdTe is on the order of $1 \times 10^{15}/\text{cm}^3$.

To complete the device a graphite electrode is deposited on top of the CdTe to a thickness of approximately 10 μm . The top electrode is completed by the evaporation of a more conductive tin-based metal contact of approximately 1 μm thickness.

The basic difference between the Type I and the Type II structures is in the CdS film. The thickness of the CdS layer is significantly less in this approach in order to pass a larger percentage of the solar spectrum.

Fig. 2-2 shows the cross-sectional scanning electron microscope view of the Type I structure. The improvement of the Type II structure over the Type I structure is shown succinctly in Fig. 2-3. The improved spectral response at wavelengths less than 520 nm allows a significant improvement in device I_{sc} . Approximately 29 mA/cm^2 is possible with a well optimized device structure. Over 25 mA/cm^2 has already been achieved.

2.2 History of Electrode

The "art" of CdTe photovoltaic devices has long been concerned with achieving a satisfactory ohmic contact to the CdTe by a practical electroding method. Two electrodes in particular have been well utilized both before and during this three year subcontract.

Tellurium Electrode

Early in the subcontract, PEI abandoned an electrode based on tellurium due to stability problems. It was found, in life testing such cells, that their primary mode of degradation was a loss of open circuit voltage. This voltage loss occurs at a decreasing rate, but the rate is strongly dependent on temperature. The loss of voltage was not found to be substantially reversible.

Figure 2-4 shows the V_{oc} of such a cell, life tested first for 1500 hours at one temperature, then subsequently at a higher temperature. Note the decreasing rate of V_{oc} loss with time, and the strongly increasing rate with temperature. Note also, that the rate of V_{oc} loss does not appear to be asymptotic to zero.

On this type of cell, a dependency on O_2 exposure was observed. Most cells utilizing this tellurium electrode, when exposed to room air or dry air, increased in V_{oc} , while cells exposed only to N_2 decreased in V_{oc} as above. The increase in V_{oc} was, however, accompanied by an increase in R_{sh} .

We attributed the voltage degradation to a diffusion process, in which Te from the electrode diffuses toward the junction, presumably along grain boundaries. The effect of O_2 is attributed to an oxide passivation of a surface recombination center.[1]

Similar behavior has also been observed at PEI when utilizing gold or nickel electrodes. These were abandoned for the same type of V_{oc} instability at elevated temperatures.

Graphite Electrode

A doped graphite electrode utilized at PEI is much more stable than the tellurium electrode. The principal mode of degradation for this type of cell is an increase in R_{sh} due to exposure to humidity. No degradation modes have been found to exist directly related either to temperature (as found with Te, Au, or Ni) or to light exposure. This electrode has exhibited excellent field stability when suitably encapsulated in order to protect it from moisture. Further discussion of stability issues will be found in Section 5.0.

2.3 Film Analysis

Considerable analysis of the CdTe film has been done during this subcontract. Two important areas of analysis have resulted from doping of the CdTe and from analyzing the surface of the CdTe. Standard analytical techniques such as ESCA, SIMS, and EDAX have been explored. Reflectivity studies through the glass substrate have also been completed. Transmission electron microscopy has also been found to be an important tool with a great deal of potential. Analyses such as these are invaluable in order to be able to confidently focus on the materials issues in which the most potential can be gained. Morphology issues relating to minority carrier lifetimes are yet to be properly addressed and will likely be the major issue when improving from the 14% efficiency level up to the 16-18% efficiency level.

Doping

Conceivably, CdTe should be significantly improved through improved doping. CdTe can indeed be made quite conductive with suitable doping; however, this higher conductivity has not yet been converted into higher efficiencies at PEI.

Heating phosphorus (or copper) and CdTe in a closed quartz container at temperatures above 750°C results in reproducible resistivities below 100 ohm-cm. Neither arsenic nor antimony have provided similar results using these procedures. It has been previously reported [1] that phosphorus-doped CdTe can result in devices having measured hole concentrations as high as $2.8 \times 10^{16}/\text{cm}^3$. Using copper-doped CdTe, measured hole concentrations are actually lower than undoped CdTe. CdTe which is not intentionally doped generally measures $0.9\text{--}2.0 \times 10^{15}/\text{cm}^3$.

The best device which has yet been produced at PEI using the phosphorus-doped CdTe measured 7.3% in efficiency, had a short-circuit current of $17.5\text{mA}/\text{cm}^2$, an open-circuit voltage of 734mV, a fill factor of 57%, and a hole concentration of $2.3 \times 10^{15}/\text{cm}^3$. Another device similarly produced with a measured hole concentration of $2.8 \times 10^{16}/\text{cm}^3$ had low J_{sc} ($12.9\text{mA}/\text{cm}^2$), low V_{oc} (692mV), and a poor fill factor (46%). A statistical comparison of six phosphorus doped and six undoped samples indicate that an increase in measured hole concentration from $2.5 \pm 0.4 \times 10^{15}/\text{cm}^3$ to only $5.1 \pm 0.7 \times 10^{15}/\text{cm}^3$ already results in lower I_{sc} (15.0 to $13.0\text{mA}/\text{cm}^2$), V_{oc} (694 to 684mV), and efficiency (6.3 to 5.9%). For polycrystalline devices doped in this manner, there appears to be a hole concentration threshold above which cell parameters suffer, especially J_{sc} and V_{oc} . According to recent work [2], the phosphorus reduces the minority carrier diffusion length in CdTe so that the threshold observed here is not likely due to an inherent correlation of performance decrease with a carrier concentration increase, but rather due to the use of phosphorus itself by these methods.

The results on devices produced by copper-doped CdTe indicates an even greater adverse affect on device performance. Very low open-circuit voltages (593mV best) were observed. It appears that during deposition and processing, the copper in the doped CdTe has a tendency to diffuse into the CdS and also to self-compensate the CdTe, thereby resulting in a much larger than optimum depletion region width, poorer fields, and a lower V_{oc} .

Contact Chemistry

The condition of the CdTe surface affects the resulting device efficiency due to its contribution to contact resistance. Therefore, treatment of the surface using various chemical rinses and etches is of major importance for good device efficiency and stability. Understanding the growth and removal steps of the oxide at the surface is both a performance and stability issue.

ESCA analyses have been done [3] on CdTe surfaces treated by our laboratory. The ESCA results on material after various steps of a bromine etch are given in Table 1. The bromine solution, 0.5 vol% in methanol, is followed by a 6 molar sodium hydroxide soak. The raw data showing the Te peak positions are also indicated.

By the method used, one cannot distinguish between Cd^0 , Cd in CdTe, or Cd in $\text{Cd}(\text{OH})_2$. Nor can this method distinguish between Te^0 and Te in CdTe. However, some valid comments can be made.

It is observed that the measured composition of the surface growth is vastly different between the 530°C (Cd/Te=.95) air heated sample and the 200°C air heat treatment (Cd/Te=1.7).

Table 2-1. ESCA Data at various stages of a Br₂ Etch

	Corrected Peak Ratios		*	Peak Positions		
	Cd/Te	Te ⁰ /Te ⁺⁺		Te	Cd	Te ⁺⁺
			Cd/Te after sputter			
#1: 200°C, air	1.7	~1.9	1.1(10min.)	572.6ev	405.3ev	576.4ev
#2: 200°C, air+Br ₂	.04	<.02	.03(5min.)	---	405.6	576.6
#3: 200°C, air+Br ₂ +NaOH	2.6	>100	1.3(5min.)	572.2	404.9	very small
#4: 200°C, air+NaOH only	1.9	>100	1.0(5min.)	572.4-.5	404.9	---
#5: 530°C, air	.95	~.02	1.3(5min.)	572.2	405.7	576.4

After the 200°C air anneal, measurements indicate an excess of Cd⁰ or a Cd compound on the surfaces likely made up of an oxide mixture of CdO, TeO₂ and CdTeO₃. However, no CdO peak near the published 404.0eV mark was observed on any sample except for a very small side peak on the 530°C, air heat treated sample. The high Cd/Te ratio on CdTe after an air anneal has been claimed to be due to Cd out-diffusion by Danaher *et al* [4] and Bryant *et al* [5].

After a subsequent Br₂/MeOH etch which removes ~0.5µm of CdTe, measurements indicate no lattice Cd or Te. The only peak observed is the Te⁺⁺ peak. It is not certain from this work whether this Te⁺⁺ peak is due to residual insoluble TeBr₄ or to TeO₂ (or CdTeO₃).

However, in either case, a subsequent soak in the NaOH solution removes the Te⁺⁺ peak entirely. Both TeO₂ and TeBr₄ are soluble in NaOH solution. The Cd/Te ratio after the NaOH soak is higher than expected for a stoichiometric CdTe. In addition, the shift of the Cd peak by 0.4-0.7eV away from the supposed CdO peak which occurred during the NaOH soak, may indicate that some residual Cd⁰ did exist at the point prior to the NaOH treatment even though no CdO peak was observed directly. Further work should include direct measurement of the CdO peak.

Similar results are seen for the NaOH soak alone after the 200°C air anneal, but the final Cd/Te ratio is higher if the Br₂ etch is done first. Residual Na was found after the NaOH soak in both cases.

It is qualitatively apparent that the oxide can be controllably removed and that the CdTe stoichiometry can be adjusted by this and similar etches. The effect on contact is pronounced. ESCA is an extremely powerful method for these types of analyses.[6]

Transmission Electron Microscopy

Recent work at SERI [7] has resulted in transmission electron micrographs of discrete grains of CdTe. Electron diffraction images indicate that these discrete grains are each a single lattice having a zincblende structure. Fig. 2-5 shows the high magnification phase images of one of these grains. A number of defect images are visible. Further work is necessary to further define the role of these defects resulting from this type of deposition. This area of analysis may become extremely important once alloying studies in CdTe are further along.

Compositional Analysis

In addition to the work done by ESCA described above, analysis of the composition of the CdTe films has been done utilizing Auger Spectroscopy and Secondary Ion Mass Spectroscopy (SIMS). [8] One of the more interesting pieces of information resulting from these analyses is that a significant amount of sulfur was found at the surface of the CdTe.

It appears unlikely that an accurate determination of the exact interface chemistry will be achieved via SIMS or any ion milling technique due to some extreme morphological results caused by the ion milling. Fig. 2-6 shows an SEM micrograph indicating the results of ion milling of CdTe on CdS films [9]. Fig. 2-7 and 2-8 show compositional vs. depth results from this type of milling-dependent morphology. Notice the broad compositional overlap caused by these morphology problems.

Reflectivity

In June - July 1989, reflectivity results on a number of different "brands" of CdTe devices were compared [10]. The results from these analyses are shown in Fig. 2-9. The specular reflections of all the "brands" were within approximately 10% of the average value of 4.7%. Ametek had the least reflection whether considering specular or total diffuse. A considerable variation in the diffuse reflectance is noted for the two different PEI samples. The earlier film (dated 1987) had a large diffuse reflectivity of 7.7%, whereas the more recent film dated 1989 had a considerably improved value of 1.7%. This value is still somewhat high compared to the Ametek result of 0.5%. However, the gain in efficiency by achieving the lower reflection value is estimated at only approximately 0.5%.

Collaborations with the SERI laboratories and with other SERI subcontractors have helped provide considerable insight into the material issues related to CdTe/CdS heterojunctions. Access to the expertise at SERI in material analysis has helped to begin to allow these issues to be properly addressed.

SECTION 3.0

DEVICE CHARACTERIZATION AND MODELING

A number of electrical and optical measurements of the CdS/CdTe devices have been performed in order to characterize the effect of process variations on the cell behavior and to better understand the mechanism of current flow at the junction. The characterizations include voltage-biased capacitance measurements (at various frequencies), electron beam induced currents (EBIC), current-voltage diode curve analyses, and optical characterizations including biased and unbiased spectral response, perturbed spectral response, and quantum efficiency measurement.

3.1 Electron Beam Induced Currents (EBIC)

Fig. 3-1 shows the results of EBIC analysis on an early device exhibiting ~7% efficiency.[11] It is clear from this figure that the peak of the photovoltaic response does not always fall at the CdS-CdTe metallurgical junction, but lies at a distance of 0.7-0.8 μm on the CdTe side of the junction. The corresponding diffusion lengths were calculated to be 0.7 μm for the p-CdTe and 1.3 μm and 1.19 μm for the n-CdTe and CdS respectively.[12]

EBIC measurements (performed at the University of Texas) on several cells showed a response which did not follow the relation, $J = J_0 \exp(-x/L)$, where x is the distance from the junction and L is the diffusion length [12]. Non-exponential behavior of an EBIC response can be attributed to, (i) non-uniform doping of CdS and CdTe resulting in spatially varying diffusion lengths, (ii) non-zero surface recombination velocity, (iii) a condition of high injection from electron beam excitation, or a combination of these three factors.

Work was done to derive the EBIC equations taking into account the high injection, the finite generation volume and the finite surface recombination velocity. Numerical solutions were obtained from the Texas Center for High Performance Computing. The details were given previously [13].

The cause of non-exponential EBIC response in these devices is not yet completely understood. However, we have noted that a number of the curves become nearly linear at distances far away from the junction. Since this is unlike the experimentally observed EBIC response the suggestion is that high surface recombination velocity is not the primary cause of non-exponential behavior of EBIC. Furthermore, it was ascertained that non-exponential EBIC is observed even at low injections.

This leads to the premise that non-uniform doping across the junction may be responsible for non-exponential EBIC response in these devices. Further analyses involving the grain boundaries and the depletion layer are necessary before this can be confirmed.

3.2 Capacitance Measurements

A zero bias value in the dark for the junction capacitance is typically 2.4 nF on a device with an area of 0.302 cm^2 , which corresponds to a depletion layer width of approximately 2.4 μm . When a cell is illuminated with a white light

intensity of as little as 16 mW/cm² its capacitance generally increases to approximately 2.9 nF (corresponding to a depletion layer width of 0.95 μm). Carrier concentration (N_A) in CdTe was determined to be 1.8×10^{15} cm⁻³ from plots of junction capacitance vs. reverse bias voltage. This calculation assumed an n⁺-p junction. Earlier measurements on Schottky diodes on CdS have typically yielded CdS carrier concentration values in the range of 10^{18} cm⁻³, nearly three orders of magnitude higher than typical CdTe carrier concentration.

Fig. 3-2 plots the junction capacitance as a function of reverse bias at 1 KHz, 10 KHz, 100 KHz and 1 MHz on a typical device. [14] There is a large difference in measured capacitance at various frequencies, and the 100 KHz curve approaches the 1 MHz curve at greater than 0.5V reverse bias. This indicates that the dispersion effects due to interface states and/or the midgap recombination states in the depletion layer persist at frequencies as high as 100KHz.

3.3 Optical Characterization

In earlier reports the results of voltage and/or current perturbations of spectral response measurements were reported. [15,16] Spectral variations were measured with and without white light bias (5.3 mW/cm²) and with a variable voltage bias (-1.0 to +0.5 V). The circuits for short-circuit current perturbation ΔJ_{sc} and open-circuit voltage perturbation ΔV_{oc} measurements were presented earlier [15].

A reduction in the magnitude of ΔJ_{sc} under forward bias in the dark as well as under white light bias was observed. On the other hand, ΔJ_{sc} appears to be much less sensitive to the intensity of white light bias in the low range of zero to 5.3 mW/cm².

Regarding the difference between 8% efficient devices and 10% devices, we concluded from these results that the increase in reverse saturation current with illumination and/or forward bias is much more important in altering the cell characteristics than is the reduction in ΔJ_{sc} .

In a somewhat different area of optical study, some recent time-resolved photoluminescence has been carried out on CdTe films [17]. The carrier lifetimes in the larger grains of CdTe were found to be approximately three times that of the smaller grains. Typical values for the minority carrier lifetime near the metallurgical interface were found to be 1.5 to 1.7 nanoseconds.

In a third area, transparent electrodes have been deposited on PEI CdTe/CdS devices for optical analyses, in addition to a number of electronic characterizations. [18] These analyses involved illuminating the resulting structure from either side (i.e. through the glass vs. through the CdTe electrode) in order to better understand the optical and electrical mechanisms involved. Fill factor problems were the norm; however, large improvements were achieved via a treatment developed at IEC, a bromine etch and a subsequent heat treatment at 150 Celsius. The major conclusions drawn from these studies were that: 1) high-performance devices can be made utilizing transparent CdTe electrodes, and 2) post electrode treatments can have significant effects on the performance of Cu-Au electrodes.

3.4 Diode Curve Discussion

As previously reported [16], many cells have exhibited a cross-over in the dark and light current-voltage characteristics in the positive voltage - positive current quadrant. This cross-over can be caused by a reduction in junction potential barrier and an effective increase in diode reverse saturation current (J_0) with illumination. A likely mechanism is the photoexcitation of interface states which changes the charge distribution at the junction and lowers the potential barrier.

The reduction of ΔJ_{sc} with forward bias appears to be relatively insensitive to the wavelength of monochromatic radiation. This insensitivity suggests that the loss mechanism is likely to be a reduced electric field at the junction causing an increased trapping of the light-generated electrons by midgap recombination centers and/or interface states. A generally weaker spectral response at longer wavelengths may indicate that the short-circuit current of these devices could be improved by increasing the diffusion lengths in the CdTe, by reducing the CdTe thickness and using a reflective electrode, and/or by achieving more heterojunction character, thereby increasing the field at the metallurgical interface.

Variation of V_{oc} with J_{sc} is normally expressed as $V_{oc} = (AKT/q) \log (J_{sc}/J_0)$. This yields a linear relation between V_{oc} and $\log J_{sc}$ when J_0 is a constant and J_{sc} is independent of bias voltage. In thin-film heterojunction devices like these, however, effective J_0 increases with light intensity and J_{sc} decreases with forward bias.

3.5 Characterization Summary

It was found previously [15], that interface states affect not only the diode reverse saturation current (J_0) but also the junction collection efficiency and hence the light generated current (J_L). A preliminary model describing the junction current flow in terms of tunneling and interface recombination was developed and presented earlier [16].

As discussed earlier, cells analyzed by EBIC showed the existence of a shallow homojunction with a peak response 0.7-0.8 μm into the CdTe. The diffusion lengths were measured as 0.7 μm for the p-CdTe, 1.3 μm for the n-CdTe, and 1.2 μm for the CdS.

Time resolved photoluminescence studies done at SERI have resulted in measured minority carrier lifetimes of 1.6 - 1.8 nanoseconds.

It was also found [15] that under a white light intensity of 16 mW/cm^2 a typical cell (0.302 cm^2 in area) capacitance is 2.9 nF, corresponding to a depletion layer width of 0.95 μm . Results from capacitance measurements at various frequencies have indicated that the dispersion effects due to interface states and/or the midgap states in the depletion layer persist at frequencies as high as 100KHz.

Quantum efficiency measurements suggest that a major loss mechanism is likely to be a reduced electric field at the junction causing an increased trapping of the light-generated electrons by midgap recombination centers and/or interface states. Absolute measurements of quantum efficiency corrected for all absorptions and reflections remains to be done.

A study of the current voltage curve for a 12.3% efficiency cell indicated that the series resistance contribution in this device is already acceptably low, at 1.0 ohm-cm². The diode quality factor measured for this cell, however, was a rather high 3.6. [19] Thus it is concluded that the potential for reaching significantly greater than 63% fill factor on the improved current devices lies primarily in the reduction of this diode quality factor and not in the ohmic contact to the CdTe.

In a recent report [20], a comparison of several "brands" of CdTe/CdS devices was made. It was shown that the major loss mechanism presently limiting device efficiencies to 12.3% are basically due to recombination effects which limit the maximum power point voltage.

Diffusion length and electric field improvements at the metallurgical interface are to be achieved through further optimization of the alloying, doping, and surface passivation of the CdTe and through further improvement of the morphology of the crystals near the junction.

3.6 Modeling of Junction Transport

The general equation to be modelled can be written as

$$J = j_{D \cdot interface} + j_{D \cdot tunnel} - J_L(V)$$

where,

J = Cell current under illumination,

J_D = Diode Current (Separated into Interface and Tunneling Currents),

J_L = Light Generated Current

A preliminary model for the current transport across the junction was developed. [15,16] As shown in Fig. 3-3, a good match between the calculated diode characteristics and the experimental curve was obtained using the following parameters:

Carrier Concentration in CdTe (N_A)	= $1 \times 10^{15}/\text{cm}^3$,
Carrier Concentration in CdS (N_D)	= $5 \times 10^{16}/\text{cm}^3$,
$\sigma_n V_{th}$	= $10^{-7} \text{ cm}^3/\text{sec}$,
$\sigma_p V_{th}$	= $2 \times 10^{-6} \text{ cm}^3/\text{sec}$,
m_p^*	= $0.4m_0$,
m_n^*	= $0.1m_0$,

where,

σ_n is the electron capture cross section,

σ_p is the hole capture cross section,

V_{th} is the electron thermal velocity,

m_p^* is the effective mass of a hole,

m_n^* is the effective mass of an electron,

Interface state density	= $0.54 \times 10^{11} \text{ cm}^{-2}$,
Interface Mobility (μ_i)	= $4 \text{ cm}^2/\text{V-sec}$,

The individual tunnelling and interface recombination components of the diode current are also plotted in Fig. 3-3 for comparison. We note that the relative contribution of $J_{D \cdot interface}$ is negligibly small (for the particular

values of σ and V_{en} used in these calculations). σ_p was chosen to be higher than σ_n because we assumed the interface states to be neutral when empty and negatively charged when filled. Further refining of this model continues.

SECTION 4.0

DEVICE AND LARGE-AREA MODULE RESULTS AND PROJECTIONS

4.1 Small Device Results and Efficiency Projections

Laboratory cells made as described in Section 2.1 of the Type I structure have shown efficiencies as high as 10.8%, with fill factors as high as 72% (19.1 mA/cm² short circuit current, .785 V open circuit voltage, 72% fill factor). Early developmental work to deposit a Type II device utilizing a thinner CdS layer, thus allowing more light to reach the junction, increased the efficiency to 12.3% (25.0 mA/cm² short-circuit current, .783 V open circuit voltage, 63% fill factor). Figure 4-1 shows the current-voltage performance for this cell as measured at SERI [21]. The dramatic increase in the blue response has resulted in an increase in current from 19.1 to 25.0 mA/cm² when comparing a Type I and a Type II structure. Using these already obtained values for current, voltage, and fill factor, 14% efficiencies are expected to be realized in the reasonably near future.

Analysis of the current-voltage characteristics on this 12.3% cell was done in order to obtain accurate values of the diode quality factor (diode ideality factor) for thin-film cells. As previously discussed, this study indicated that the series resistance contribution in this device is already acceptably low, at 1.0 ohm-cm². The diode quality factor measured for this device, however, was a rather high 3.6. Thus it is concluded that the potential for reaching significantly greater than 63% fill factor on the improved current devices lies primarily in the reduction of this diode quality factor and not in the ohmic contact to the CdTe.

Table 4-1 indicates a conservative estimate for the efficiency potential of this technology. Using already obtained values for current, voltage, and fill factor, 14% efficiencies are expected to be realized in the reasonably near future. Greater than 17% efficiencies are expected in the longer term.

Table 4-1. Device Efficiency Projections

	<u>Present Cell</u>	<u>Ideal Device</u>	<u>Best Observed Single Parameter</u>	<u>Optimized Device</u>
V _{oc}	0.78 V	0.95	0.83	0.85
J _{sc}	25 mA/cm ²	29	25	27
FF	0.627	0.80	0.72	0.75
Eff	12.3%	22.0%	12.3% 14.9% if all together	17.2%

4.2 Progress on 1 ft² Modules

A 1 ft² module is prepared with the layers as described above. An interconnection step such as was shown in Fig. 2-1 allows one to optimally match the maximum power point of a single module to a 12 volt storage battery. Figure 4-2 shows an unencapsulated module with such an interconnection.

Table 4-2. Performance of Modules Delivered to SERI

Date	Output	Active Area	Active Area Eff	Aperture Area Eff
June '87	4.0W	660cm ²	6.1%	5.4%
Nov. '87	4.4W	660cm ²	6.6%	5.8%
March '88	4.7W	686cm ²	6.8%	6.1%
June '88	5.3W	760cm ²	7.0%	6.3%
Oct. '88	6.1W	754cm ²	8.1%	7.3%

Significant progress has been made since 1987. As seen in Table 4-2, an increase of over 35% in aperture area efficiency was attained in only 16 months. An active-area efficiency of 8.1% average over the entire area has been attained. An aperture area of 838 cm² for the same module results in a 7.3% aperture area efficiency. The current-voltage performance curve for a 6.1 watt module is shown in Figure 4-3.[22]

4.3 Progress on 4 ft² Modules and Efficiency Projections

The Department of Energy (DOE) objectives for photovoltaic development call for PV modules larger in area than 1 ft² in order to properly address the future of large-capacity terrestrial photovoltaic installations. With this in mind, a 4 ft² module was produced and delivered to SERI in 1988.

Both 1 ft² and 4 ft² modules may be produced with equipment currently in place at PEI. Performance optimization is ongoing on both sizes of module.

A demonstration project for the 4 ft² substrates is a 20 KW installation to be installed in Davis, CA for the Photovoltaics for Utility Scale Application (PVUSA) project. The 4 ft² module to be produced at PEI will be 2' x 2' and will yield 23 to 28 watts in the early stages.

Further improvement of the percentage of active area on a given module can be realized. The portion of the active area lost at the division (interconnection) can practically be reduced from approximately 12% to less than 6%. Increasing the size of the module to 4 ft² allows an aperture area of 3413cm² with a 1/2" border. At 7% aperture area efficiency nearly 24 Watts can be expected on the 4 ft² modules. Considerable work remains in order to optimize the output of these larger modules.

A midterm goal for modules is an overall module active area efficiency of 12% corresponding to an output of approximately 9 watts per ft^2 or 36 watts on a 4 ft^2 module. This increase is to be accomplished by further optimization of the fill factor, the window layer, and the active area to total area ratio. After full optimization of device structure, materials, and processing, a 14% efficiency over the active area is expected to be achieved and will be able to produce approximately 50 watts output from a 4 ft^2 module at 1000 watts/m^2 insolation. This corresponds to 135 watts per m^2 and is expected to be achieved in the mid 1990's. In the longer term over 150 Watts per square meter is the ultimate goal.

SECTION 5.0

STABILITY, ENCAPSULATION AND LIFE TESTING

5.1 Stability Issues

Considerable work has been done at PEI regarding encapsulation and lifetesting cells and modules. There are a number of issues involved in providing a photovoltaic product exhibiting long term reliability.

Early on in the contract, a number of discussions and reviews with the Reliability and Testing Laboratory at JPL [23,24] were quite helpful in order to help us understand the complete issue of encapsulation. The foundation that JPL laid helped us to avoid a number of problematic design issues.

It was realized that not only are moisture resistance and structural integrity of the module important, but also such issues as long-term corrosion, adhesive or plastic degradation in ultraviolet light, and chemical incompatibilities. Most or all of these issues can be avoided by the proper choice of design or materials.

Through studies of water ingress into modules and studies of sensitivity of the active materials to water, we have been able to achieve extrapolated lifetime values as discussed below.

5.2 Results From Early Encapsulation Methodology

As discussed in Section 2.2, PEI had abandoned development on an electrode based on tellurium due to stability problems. It was found, in lifetesting such cells, that their primary mode of degradation was a loss of open circuit voltage dependent on temperature. Similar life testing results were observed with gold or nickel electrodes.

A graphite electrode was developed which indicates good stability when adequately encapsulated. The principal mode of degradation which an unencapsulated cell using this improved electrode can exhibit is an increase in R_{sh} due to an overexposure to humidity as previously discussed. The major focus of the reliability turned to the encapsulation itself.

An early encapsulation method explored was a lamination of a foil to the active substrate using a vacuum bag laminator of known design [25]. Foils were utilized due primarily to their cost advantages. The thermoplastic and thermoset adhesives explored by this method have generally been EVA-based.

It was considered a possibility that the use of a foil-to-glass encapsulation would lead to failures due to differential thermal expansion of the foil and glass. Therefore, modules were cycled from -30°C to +60°C on a 3-hour cycle for several weeks. In these conditions were placed modules sealed with foil-to-glass and glass-to-glass systems, and with an edge-only system. We found no evidence of thermal expansion stress problems on any of the samples.

Long-term life test results on cells encapsulated with EVA and a cover glass only showed good stability for some time followed by a significant increase in R_{eq} , indicating that humidity eventually reached the cell from the exposed edges of the EVA. This result shows the need for an edge seal with improved design so as to protect against oxidation and water vapor effects better than EVA alone.

Further evidence that EVA alone was not an adequate encapsulant is data collected for PEI at the Jet Propulsion Lab [24], in which humidity sensors encapsulated by various methods were tested in 85%RH 85°C for 300 hours. Many schemes failed, including EVA glass-to-glass, but the two which passed the full 300 hours were both epoxy edge seals.

In a second generation encapsulation method, the EVA application was followed by an edge seal with high-performance epoxy. Even though this method was quite satisfactory from a manufacturing standpoint, the stability of this type of early encapsulation was not acceptable. Fig. 5-1 shows the improvements in stability over early life testing, and that good stability can be realized when modules are sealed utilizing the methodology described in the next subsection.

5.3 Present Status of Life Testing on Modules

Long-term outdoor and accelerated life testing at PEI has shown the CdS/CdTe device structure to be inherently stable, if adequately encapsulated. Outdoor lifetesting at the SERI Outdoor Measurement and Reliability Testing Laboratory have shown no measurable degradation after 270 days so far. The data from this life testing is shown in Fig. 5-2.[26] In addition, accelerated lifetesting of laboratory cell samples, at elevated temperatures, is an ongoing part of process parameter studies, and substantiates the inherent stability of the device structure.

Proper encapsulation does play a very important role in the stability of these devices. A novel and secure encapsulation method has been developed. Backcaps formed out of sheet metal, containing two hermetic electrical feedthroughs, are edge sealed to the float glass border surrounding the module's active material. A dessicant is placed inside the backcap during this process.

Any polymer adhesive will exhibit a certain bulk permeability to water vapor, and probably to a greater degree, will exhibit permeability along the bond line interface due to the polar nature of the water molecule.

The design of such an encapsulation system involves first quantifying the rate of moisture ingress into the package. Such work has [24] shown less than 10mg of water entering a suitably structured polymer edge seal around the periphery of a 4" x 6" test module in 2232 hours at 85°C and 85%RH. The corresponding ingress value of water was therefore less than 0.02g per year per linear foot of edge (at elevated temperature and humidity).

A dessicant with appropriate properties must be selected; primarily it must hold the vapor pressure of water low even at the elevated temperatures seen during outdoor exposure of the modules. Finally, enough dessicant is included that an acceptable lifetime may be extrapolated. Failures of the adhesive in rigorous desert lifetesting conditions can occur with some backcap-adhesive combinations. Resistance to differential thermal expansion, weathering, and UV exposure are also required.

It has been shown by the SERI Reliability and Testing Laboratory that the structural integrity of a sufficiently compatible set of materials is adequate regarding expansion coefficient issues. A 4 ft² module was thermally cycled from -40 °C to 90 °C for over 200 cycles with no indications of any type of delamination.[27]

SECTION 6.0

FUTURE PLANS

The efficiency and stability objectives at PEI on CdS/CdTe modules are being addressed. The feasibility of producing 4 ft² modules of CdS/CdTe has been shown and requires further effort in order to realize the true potential for this technology.

In the near future, the greatest potential for efficiency improvement beyond the results discussed will be realized through further optimization of the window layer and the improvement of the fill factor. In addition, optimization of the absorber material using methods including alloying and doping will result in the minimization of the recombination losses and the enhancement of the collection efficiency. In the long term, it is believed that device efficiencies will exceed 17%.

Module output will also be increased by uniformity improvement in the deposition process, and by minimizing the loss of active area due to interconnects. Module output is expected to attain 135 watts per square meter in the mid 1990s and over 150 watts per square meter in the longer term.

Future directions in encapsulation will pursue the development of a low-cost hermetic seal, study of barrier coatings applied directly to the film before encapsulation of the backcap, and address corrosion and other long-term reliability issues.

A three-year contract, through SERI, to accomplish a number of these issues begins in July 1990.

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ABSTRACT

This is the final technical progress report required under a three year subcontract through the Solar Energy Research Institute, #ZL-7-06031-3.

The efficiency and stability goals under this subcontract are being addressed.

Efficiencies of up to 12.3% have been achieved on small devices. It is expected that 14% efficiency will be exceeded on small devices by improving the fill factors on the present devices in the reasonably near future. Efficiencies in the 16-18% are expected to be achieved in the longer term.

Modules approximately 929 cm² in area with an active area efficiency of over 8% (aperture efficiency of 7.3%) are producing over 6 watts peak power output.

The feasibility of producing 4 ft² modules of CdS/CdTe has been shown and requires further effort in order to realize the overall potentials.

The structural integrity of the encapsulation design and methodology appears satisfactory. Encapsulated submodules have been life tested for over 270 days with no observable degradation by the SERI Outdoor Reliability and Life Testing Laboratory.

In addition to further optimization of materials and device structure, module output will be increased by uniformity improvement in the deposition process, and by minimizing the loss of active area due to cell division inter-connects. Module output is expected to attain 135 watts per square meter in the mid 1990s and over 150 watts per square meter in the long term.

Schematic Cross-Section of the Type I Device, Showing Division Interconnections

Figure 2-1

Scanning Electron Micrograph Showing an Edge View of the Tin Oxide, CdS, and CdTe Films

Figure 2-2

Quantum Efficiency

Comparison of Quantum Efficiency of a PEI 12.3% Efficiency Device
With an IEC-Made Device Using Conventional Window Layers

Figure 2-3

V_{oc} DEGRADATION AT TWO TEMPERATURES USING NOW-ABANDONED Te ELECTRODE

Open Circuit Voltage vs. Time For Now-Abandoned Tellurium
Electrode

Figure 2-4

**Transmission Electron Micrograph of a Single Grain of CdTe
Showing Pure Crystallinity and Line Defects**

Figure 2-5

Scanning Electron Micrograph of Ion-Milled CdTe Films

Figure 2-6

SERI DEPTH-PROFILE

#1 Cs+/-

SIMS Results on CdTe/Cds Film Using O⁺ Ions For Milling
Figure 2-8

Angular Reflectivities on CdS/CdTe Devices

Figure 2-9

Reflection From CdTe Photovoltaic Cells

EBIC Analysis on a 7% Efficient CdTe/CdS Device

Figure 3-1

GRAPH OF VOLTAGE-BIASED CAPACITANCE AS A FUNCTION OF FREQUENCY

Graph of Capacitance at Various Frequencies

Figure 3-2

GRAPH OF CURRENT VS. VOLTAGE

For Experimental vs Modelled Data

Experimental and Calculated Diode Characteristics Under Illumination

Figure 3-3

Light I-V

Current-Voltage Performance Curve of a 12.3% Device Measured at SERI

Figure 4-1

Photograph of an Unencapsulated 1 ft² CdS/CdTe Module

Figure 4-2

Sun=100.0mW/cm²

Pmax=6.11W

Voc=20.485V

Isc=0.519A

FF=57%

Aperture Area

Efficiency=6.51%

Active Area

Efficiency=7.3%

Figure 4-3

Current-Voltage Response for a One-Square-Foot Module Delivered to SERI, as Measured on the Spire Simulator at SERI

Progress on Stability of Modules

Figure 5-1

OUTDOOR LIFE TESTING DATA MEASURED AT SERI

Outdoor Life-Testing Results on PEI Submodules

Figure 5-2

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16. Abstract (Limit: 200 words) This report describes a three-year project to develop an improved materials technology and fabrication process to produce 1-ft ² and 4-ft ² CdS/CdTe photovoltaic modules. The stability objective for the project was to develop techniques to provide a ten-year life extrapolation with an efficiency degradation of not more than 10%. First, CdS/CdTe devices were analyzed; electrical and optical measurements were taken to characterize the effect that process variations had on cell behavior and to better understand current flow at the junction. Second, device and module efficiency improvements were quantified. Photovoltaic devices of various sizes were analyzed. Small-area devices achieved active-area efficiencies of up to 12.3%, and other, lower-current devices exhibited fill factors as high as 72%. Efficiencies in excess of 14% are expected by improving the fill factor on higher-current devices. Finally, encapsulation and life testing studies were carried out on devices made with a doped-graphite electrode (which proved to be more stable than the Te-based electrodes). Thermal cycling on 1-ft ² and 4-ft ² modules revealed no delamination modes. Encapsulated submodules were life-tested outdoors for more than 270 days and showed no observable degradation. Detailed conclusions and a recommended future direction are also presented.			
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