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Fundamentals of Polycrystalline Thin Film Materials and Devices

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SUMMARY

Objectives:

The principal objective of the research described in this report has been to gain a deeper understanding of the materials, processing, and device issues needed to improve the performance, reliability, and cost of polycrystalline thin film solar cells. A further objective of this research has been to support the efforts of the SERI polycrystalline thin film task through collaboration with other research groups, especially the thin film PV industry.

Discussion:

In order to achieve these objectives, the Institute of Energy Conversion (IEC) has carried out a program of investigation and analysis of polycrystalline thin-film CuInSe_2 and CdTe processing, materials and devices. The research was organized into six integrated tasks encompassing: (1) CuInSe_2 thin film deposition; (2) band gap modified CuInSe_2 solar cells; (3) window layers; (4) innovative cell design; (5) CdTe solar cell processing; and (6) device analysis.

CuInSe_2 films were deposited by elemental vacuum evaporation from Cu, In and Se effusion sources where the incident fluxes are controlled by precisely controlling source temperature. The system was highly reliable and reproducible and was used to provide samples for the other tasks and to other research groups needing device-quality CuInSe_2 . Formation of CuInSe_2 by selenization of Cu/In layers was also investigated. Cu and In layers were deposited by electron beam evaporation. A system for reacting Cu/In layers in flowing H_2Se was designed, built and tested, including an effective H_2Se effluent gas treatment unit. Two major problems, the effect of substrate holder material and control of the Cu/In ratio, were identified and corrected. Single phase CuInSe_2 films were grown at different growth temperatures, gas flows/concentrations and reaction times. The Cu/In layers are converted to CuInSe_2 films in less than 20 minutes and little effect of H_2Se gas concentration on the film composition was observed. CuInSe_2 devices with efficiency over 7% were fabricated.

Previous analysis of high efficiency CuInSe_2 cells indicated that the V_{oc} is limited by Shockley-Read-Hall recombination in the CuInSe_2 . This suggests that V_{oc} can be increased by increasing the bandgap of the absorber region near the heterojunction interface. The approach taken to forming CuInSe_2 layers with an increased bandgap region near the surface has been to form thin Cu(InGa)Se_2 layers. Initially, uniform Cu(InGa)Se_2 films were deposited to establish the capability to deposit device quality Cu(InGa)Se_2 by elemental evaporation. Uniform $\text{CuIn}_y\text{Ga}_y\text{Se}_2$ devices

with $y=0.4$ and $E_g=1.25$ eV were fabricated with $V_{oc}>550$ mV. Then $CuInSe_2/Cu(InGa)Se_2$ layer devices with the $Cu(InGa)Se_2$ layers ranging in thickness from 0.1 to 0.5 μm were fabricated and characterized. The $Cu(InGa)Se_2$ device behavior demonstrated that V_{oc} can be increased while still generating carriers at wavelengths out to the $CuInSe_2$ band edge.

The goal of research on window layers for $CuInSe_2$ solar cells was to increase J_{sc} while maintaining V_{oc} and FF. A solution growth technique for depositing thin ($<500\text{\AA}$) layers of CdS from aqueous solutions of cadmium salts, thiourea and complexing agents was adopted. When ZnO was used as a transparent conductor instead of ITO, problems with pinholes in the thin CdS were managed and cells with $J_{sc} = 40$ mA/cm² and efficiency over 10% were achieved.

Conventional high efficiency $CuInSe_2/CdS$ solar cells have been developed in the so-called substrate configuration in which the $CuInSe_2$ is deposited first onto Mo coated glass. Superstrate devices in the configuration glass-transparent oxide-CdS- $CuInSe_2$ are of interest for future development of monolithically integrated thin-film modules. Glass/ITO/CdS/ $CuInSe_2$ solar cells in the superstrate device configuration were fabricated using CdS films with thicknesses from 0.1 to 1.0 μm that were evaporated on glass sputter coated with ITO with a sheet resistance of 10 $\Omega/\square$. Both In-doped and undoped CdS films were used with the resistivity of the films varying from 10 to 10^{-3} $\Omega\cdot cm$. The $CuInSe_2$ films were deposited by three source evaporation in a single step at substrate temperatures from 300°C to 400°C. Electron beam evaporated Pt served as an ohmic contact to the $CuInSe_2$. The best superstrate device was characterized by $V_{oc} = 0.33$ V, $J_{sc} = 35$ mA/cm², FF = 55% and Eff. = 6%.

Collaborations with SERI PV industry subcontractors (AMETEK Applied Materials and Photon Energy) showed that high efficiency CdS/CdTe solar cells could be fabricated using a variety of techniques for forming the CdS and CdTe layers, including physical vapor deposition methods developed at IEC. Post-deposition processing - heat treatments and chemical treatments - and contacts were found to be the critical steps in CdS/CdTe cell fabrication. The post-deposition processing consisted of coating as-grown CdTe with a thin layer of $CdCl_2$, heat treating in air at 400°C, application of a Cu/Au contact, heat treating at 150°C, and chemical treatment in Br_2 -MeOH or hydrazine. The effects of each processing step on material and device properties were investigated. Heat treating CdTe with a $CdCl_2$ coating restructures the CdTe by increasing grain size and interdiffusing Te and S. Without the $CdCl_2$ coating, higher temperatures ($T>500^\circ C$) are needed to produce these changes. Bi-facial I-V and spectral response analyses show that the as-deposited CdTe/CdS devices operate in a p-i-n mode. After a mild heat treatment, which it is believed causes Cu to diffuse from the contact into the CdTe, the CdTe layer becomes more p-type, resulting in a p-n

heterojunction device. Immersion of the devices in $\text{Br}_2\text{-CH}_3\text{OH}$ or $\text{N}_2\text{H}_4\text{-H}_2\text{O}$ for a few minutes results in V_{oc} increasing from 650 mV to >720 mV. The relatively rapid effect of the chemical treatment suggests action at grain boundaries. AES and SIMS analysis indicate a sharp reduction in Cd at the near-surface region of the CdTe which makes conditions favorable for formation of Cu and Au tellurides, both of which form ohmic contact to p-type CdTe, hence the improved contact. Using the post-deposition processing procedures, a small area CdS/CdTe cell with 9.6% efficiency was verified by SERI.

The primary limitation on the efficiency of thin film CuInSe_2 polycrystalline solar cells is low open circuit voltage (V_{oc}). By analyzing the current-voltage (I-V) behavior and spectral response of thin film $\text{CuInSe}_2/(\text{CdZn})\text{S}$ solar cells, it has been possible to determine and quantify the mechanisms controlling device behavior under illumination and suggest possible improvements to enhance V_{oc} . Previous measurements and analysis indicated that the open circuit voltage is limited by Shockley-Read-Hall recombination. Recent device analysis has focussed on quantifying this behavior with emphasis on optimization heat treatments and as accurate determinations of diffusion lengths and optical absorption coefficients.

A method has been developed to determine the minority carrier diffusion length in operating $\text{CuInSe}_2/(\text{CdZn})\text{S}$ polycrystalline thin film solar cells. The technique involves measuring the spectral responses through both the (CdZn)S front side of the device and a semi-transparent molybdenum-glass back. From analysis of bi-facial spectral response on operational high efficiency CuInSe_2 devices, a diffusion length > 1 μm and the CuInSe_2 optical absorption coefficient from 1 to 1.4 eV were determined.

Heat treating CuInSe_2 devices in hydrogen was found to primarily affect the resistivity of the CuInSe_2 layer and the dark resistivity was found to increase by around 2 orders of magnitude depending on the duration of the reducing heat treatment. The CuInSe_2 Fermi level E_{fp} shifts towards the middle of the bandgap. The position of the CuInSe_2 Fermi level is expected to affect both the $\text{CuInSe}_2/\text{CdS}$ heterojunction and the Mo/ CuInSe_2 back contact.

Spectral response and temperature dependent current-voltage (I-V vs. T) measurements on $\text{CuInSe}_2/\text{CdS}$ devices were carried out as a function of hydrogen heat treatments. The behavior of $\text{CuInSe}_2/\text{CdS}$ heterojunction solar cells during heat treatments was quantitatively modelled by considering the change in resistivity of the CuInSe_2 and its effect on the collection widths at both the $\text{CuInSe}_2/\text{CdS}$ heterojunction and the Mo/ CuInSe_2 back diode. It was found that the $\text{CuInSe}_2/\text{CdS}$ heterojunction is governed by Shockley-Read-Hall recombination in the CuInSe_2 with $\phi \sim 1.0$ eV and

A₂. The Mo/CuInSe₂ back diode, which is in series with the heterojunction, is characterized by $\phi' \approx 0.2$ eV and $A' = 1$, but only has a photovoltaic contribution (i.e., $J_L' \neq 0$) when the device has been heat treated in hydrogen. Furthermore, the back diode has no effect on efficiency of cells that have been heat treated in air and tested under normal operating conditions.

Conclusions

- ▶ An apparatus for formation of device quality CuInSe₂ films by selenization of Cu and In has been constructed and is being used to conduct fundamental studies of selenization kinetics.
- ▶ Open circuit voltage of 0.55 volts has been achieved by alloying CuInSe₂ with Ga to increase the band gap and band gap modified Cu(InGa)Se₂/CuInSe₂ shows promise for achieving increased open circuit voltage without loss in short circuit current.
- ▶ A CuInSe₂/CdS solar cell with short circuit current of 40 mA/cm² was fabricated using a thin CdS window layer deposited from aqueous solution and sputtered ZnO transparent conductor.
- ▶ A CuInSe₂/CdS solar cell in a superstrate configuration - glass/ITO/CdS/CuInSe₂/Pt - with >5% efficiency has been fabricated.
- ▶ Post-deposition heat treatments and chemical processing steps have been developed and used to fabricate a CdS/CdTe cell with efficiency of 9.6% using physical vapor deposition to deposit CdS and CdTe.
- ▶ A bi-facial spectral response technique for determining the diffusion length and optical absorption coefficient of CuInSe₂ in an operational CuInSe₂ solar cell has been developed.
- ▶ The effects on current-voltage behavior of heating CuInSe₂ solar cells in air and in hydrogen have been quantitatively modelled on the basis of reversible changes in Fermi level position in CuInSe₂.

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SECTION 1.0

INTRODUCTION

1.1 BACKGROUND

Polycrystalline thin film solar cells based on CdTe and CuInSe₂ have the potential to become flat-plate solar electricity generating sources on a widespread basis throughout much of the world. Research has led to the development of active-area cell efficiencies of 10%-14%. Improved stability of prototype thin film CdTe and CuInSe₂ modules has also been demonstrated. However, studies carried out by U.S. DOE and EPRI indicate that efficiencies greater than 15% will be of great value for flat plate modules. Therefore, further fundamental research is needed to achieve these higher efficiencies. In order to systematically improve the performance of polycrystalline thin film devices and to establish achievable efficiencies, improved understanding at both the material and device level is necessary. Understanding the growth kinetics of films during the actual deposition process will help develop device quality films for fabricating high performance devices. Modeling studies will help identify the various loss mechanisms and point out the directions for improvement in solar cell fabrication. Characterization and analysis of the chemical, electronic, optical, and structural properties of thin films will assist in improving performance of devices. Novel methods for depositing low-cost, high performance materials will also assist in developing low-cost approaches to help meet the U.S. DOE long-term goals.

Accordingly, an objective of the research described in this report has been to gain the deeper understanding of the materials, processing, and device issues needed to improve the performance, reliability, and cost of polycrystalline thin film solar cells. A further objective of this research has been to support the efforts of the SERI polycrystalline thin film task through collaboration with other research groups, especially the thin film PV industry.

1.2 TECHNICAL APPROACH

In order to achieve these objectives, the Institute of Energy Conversion (IEC) carried out a program of investigation and analysis of polycrystalline thin-film CuInSe₂ and CdTe processing, materials and devices. The research was organized into six integrated tasks which are summarized in Table 1.1.

Table 1-1 Research Tasks and Primary Emphasis

Task 1. CuInSe₂ Thin-Film Deposition

- develop a well-characterized and reproducible process for fabricating device quality CuInSe₂ thin-films by selenization of Cu and In layers

Task 2. Band Gap Modified CuInSe₂ Devices

- fabricate and characterize photovoltaic devices with band gap modified CuInSe₂ by alloying with Ga in order to reduce space charge recombination and increase open circuit voltage.

Task 3. Window Layers for CuInSe₂ Devices

- fabricate and characterize CuInSe₂ devices with high transparency window layers to determine maximum short circuit current.

Task 4. Innovative CuInSe₂ Solar Cell Configuration

- fabricate and characterize CuInSe₂ solar cells in a glass/TCO/window layer/CuInSe₂/back contact superstrate configuration

Task 5. Thin-Film CdTe Devices

- fabricate and characterize high efficiency CdTe solar and determine effects of post-deposition processing on device behavior

Task 6. Device Modelling and Analysis

- determine optical absorption coefficient and minority carrier transport in CuInSe₂ in operational high efficiency devices from bifacial spectral response measurements.
- determine limits to efficiency of state-of-art polycrystalline thin-film CuInSe₂ and CdTe solar cells and develop approaches for increasing efficiency

1.3 OUTLINE OF REPORT

In this report we describe significant results obtained under each of the Tasks delineated in Table 1-1. In Section 2.0 the design of IEC's selenization and effluent treatment system are described along with materials characterization and device results obtained with CuInSe_2 that was fabricated by reactive annealing of Cu and In layers in hydrogen selenide. In Section 3.0 development of $\text{CuIn}_{1-y}\text{Ga}_y\text{Se}_2$ films and fabrication and analysis of band gap profiled devices are presented. High short circuit current ($>40 \text{ mA/cm}^2$) CuInSe_2 cells with thin CdS window layers and ZnO transparent contacts are reported in Section 4.0. An alternative device configuration in which glass/ITO/CdS/ CuInSe_2 /Pt devices were fabricated in the superstrate configuration is described. Progress towards achieving high efficiency CdTe cells using physical vapor deposition techniques to deposit the CdTe and post-deposition annealing and chemical treatments is reported in Section 6.0. Finally, in Section 7.0 quantitative determination of the optical absorption coefficient, electron diffusion length and space charge width of the CuInSe_2 in an operational high efficiency device are reported along with the quantitative analysis of the effects of reducing heat treatments on the current-voltage behavior of CuInSe_2 devices.

SECTION 2.0

CuInSe₂ THIN FILM DEPOSITION

CuInSe₂ films were deposited by two techniques- elemental evaporation and selenization of Cu and In layers deposited by e-beam evaporation. The films were deposited on Corning 7059 and soda lime glass sputtered coated with Mo. The composition of the films were determined by EDS and structural properties examined by XRD. The most sensitive measure of film properties was obtained from analysis of devices.

2.1 TWO-STEP ELEMENTAL EVAPORATION

CuInSe₂ films were deposited by elemental vacuum evaporation from Cu, In and Se effusion sources where the incident fluxes are controlled by precisely controlling source temperature. The system was highly reliable and reproducible and was used to provide samples for Tasks 2, 3, 4 and 6.

The CuInSe₂ films are deposited by a two step process where both substrate temperature and the incident flux ratio of Cu/In is increased during the deposition as described previously (1). Eight 2.5 x 2.5 cm substrates are coated with CuInSe₂ during each deposition. The substrates are typically a combination of 7059 or soda lime glass coated with from 400 nm to 1.0 microns of Mo. One sample from each deposition is processed into devices to verify the quality of the CuInSe₂ films. A fourth source was installed in the system to deposit Cu(InGa)Se₂ films as described in Section 3.0.

2.2 SELENIZATION OF Cu/In LAYERS

CuInSe₂ films grown by selenization have been used for solar cells with efficiencies over 10% (2) and designs for commercial scale systems have been reported (3,4). The selenization process consists of simultaneous or sequential deposition of Cu and In films on a glass/Mo substrate with a Cu/In molar ratio of about 0.9. The Cu-In films are reactively annealed at 400°C in an H₂Se/Ar gas mixture at atmospheric pressure for about 1 hour. A number of variations on this basic approach have been reported, including annealing of a trilayer copper/indium/selenium structure (5), annealing of multiple trilayers (6), sequential selenizations to produce a copper-rich/indium-rich bilayer structure (7), reactive sputtering with a selenium source (8), and annealing in the presence of elemental selenium vapor (9). In this report, the selenization of single Cu-In bi-layers using a H₂Se/Ar gas mixture in a flowing reaction system is described. The major problems encountered in developing this alternate CuInSe₂ film process were controlling of the Cu/In ratio and the effect of the substrate holder on the film growth.

2.2.1 Selenization of Cu-In in Closed Ampoules

Preliminary experiments on selenization of Cu-In layers with elemental Se were performed using a sealed ampoule approach. Electron-beam deposited Cu and In layers (on 7059/Mo substrates) with a Cu/In molar ratio of 1.0 were vacuum sealed in a quartz ampoule containing Se. Using this configuration, the Cu-In layers were converted to CuInSe_2 in a saturated Se atmosphere in which the total selenium pressure was determined by the sum of the equilibrium partial pressures of the Se species (Se to Se_8) over liquid Se at the reaction temperature. A series of eight experiments were performed where the reaction temperature was varied from 300 to 500°C and reaction time was varied from 10 minutes to 16 hours. Results of these experiments are summarized below:

1. At a reaction temperature of 500°C, the entire Mo/Cu/In/Se film flaked off the glass substrate.
2. The composition of all films determined by EDS was nominally 24% Cu, 25% In and 51% Se independent of reaction temperature and time.
3. All films were single phase CuInSe_2 from XRD measurements. This result, along with the composition measurements, indicates that for films formed in a saturated Se atmosphere the entire Cu-In film is converted to CuInSe_2 in less than 10 minutes.
4. XRD analysis of all films showed the presence of MoSe_2 .

2.2.2 Design of Reaction System and Effluent Treatment

An atmospheric pressure tubular flow reactor to selenize Cu-In layers using flowing $\text{H}_2\text{Se}/\text{Ar}$ gas mixture was designed and built. The system (Figure 2-1) consisted of a quartz tube with a 35 cm long, 2.5 x 5.0 cm, rectangular cross section, a gas handling system to control the flow rate and $\text{H}_2\text{Se}/\text{Ar}$ ratio and a tube furnace with a 10 cm flat temperature zone to heat and control the reaction temperature.

In conjunction with the selenization reactor, a waste treatment system (Figure 2-2) to dispose of the H_2Se effluent was designed and built. The waste treatment system consisted of a packed countercurrent gas-liquid absorption column, which utilizes a 1 molar solution of sodium hydroxide for the liquid phase; in series with a caustic soda impregnated carbon absorption column. Together, the two units were designed to reduce the hydrogen selenide concentration to below 10 ppb from an initial concentration of 5% by weight for a flow of 1 liter per minute (STP) - a flow rate that is over a factor of 10 higher than normal operating conditions. The concentration of effluent is

Figure 2-1. Schematic of laminar flow quartz reactor system for selenization of Cu/In films.

Figure 2-2 H_2Se waste treatment system

further reduced before it is released to the atmosphere due to dilution by the bulk airflow through the fume hood (1300 cfm) under which the waste treatment system is placed. The resultant stack effluent concentration is 0.12 ppb. This is below the allowable continuous average stack concentration for hydrogen selenide of 2 ppb.

2.2.3 Cu-In Layers

Cu/In bilayer films were deposited by electron beam evaporation from 99.999% pure Cu and In sources. Nine one square inch $2\text{ }\mu\text{m}$ Mo-coated glass substrates in a 3" x 3" array, or eighteen $1/2$ " x 1" substrates were placed into the deposition system at one time. Cu was deposited first, followed by a top layer of In. Films selenized from Cu over In layers did not adhere to either Mo-coated 7059 or soda lime substrates. The Cu:In ratio was chosen to be between 0.85 and 1.0. In order to achieve a final film thickness of about $2\text{ }\mu\text{m}$, Cu and In thicknesses of approximately 2300 and 5600Å respectively were required. The individual film thicknesses were monitored by a quartz crystal monitor.

Initial experiments on selenization of Cu/In layers with the same molar ratio (determined from the quartz crystal monitor) showed poor correlation of the Cu:In ratio with CuInSe_2 film composition. As a result, the reproducibility and control of the Cu/In layers deposited in electron beam evaporator was evaluated by atomic absorption spectroscopy (AA), optical interferometry, surface profilometry, and EDS. The results indicated:

1. The e-gun process had been producing both Cu and In layers which were thinner than the target thicknesses of 2100Å for Cu and 5300Å for In. Thicknesses determined by AA were about 1800Å for Cu and 3400Å for In, which resulted in Cu rich starting materials. The quartz crystal monitor was recalibrated and Cu-In layers are now deposited with an accuracy of $\pm 100\text{Å}$. Based on this degree of reproducibility, a Cu-In layer with a target molar ratio of 0.90 will be 0.90 ± 0.05 . Based on results of selenization of Cu-In layers with known molar ratios, the resultant Cu content of the CuInSe_2 film should be controllable to within a range of 0.21 to 0.25.
2. The uniformity of the Cu and In film thicknesses over the 4" by 4" substrate holder was about 25%, but there was no measurable spatial variation in the Cu/In ratio.

Based on these results, a sample from every Cu/In deposition is analyzed by AA prior to selenization.

The structure of the Cu, In and Cu/In films was examined. For single layer films, the Cu layer was observed by SEM and optical

microscopy to be smooth and specular. On the other hand, the In layers usually appeared rough, with droplets or connected pools of indium approximately 10 μm across. Figure 2-3 is an SEM micrograph of a Cu/In bilayer. XRD of as-deposited Cu/In bilayers showed the presence of intermetallic Cu-In phases in addition to the pure metals.

The condition of the Cu/In layers at elevated temperatures prior to reaction was also examined. From the Cu-In phase diagram, at 400°C the film may contain a solid phase consisting of approximately 40% In and 60% Cu in equilibrium with a liquid phase consisting of approximately 90% In. From hot stage optical microscopy, the formation of liquid and solid phases at temperatures between 150°C and 450°C was observed. Heat treatments of the Cu/In bilayers on glass and Mo-coated glass substrates were also performed in 200 sccm of flowing argon at temperatures between 300°C and 450°C. The irregular, connected structure of the In layer was preserved during heat treatments of up to two hours at 400°C. XRD patterns of films heat treated for 15 minutes at 400°C showed no pure Cu and In metal phases. For most of the heat treated films, the XRD patterns could be related to one or more of the established Cu-In intermetallic phases (e.g., Cu_9In_4 , Cu_4In). After about one hour at 400°C, the XRD patterns of the films stabilized. The results of heat treatments at lower (300°C) and higher (450°C) temperatures were qualitatively similar to those at 400°C. At 300°C, XRD results after 120 minutes showed little change, while the same was true after 15 minutes at 450°C. AA analyses of heat treated Cu/In bilayers showed no measurable loss of In due to the heating process.

2.2.4 CuInSe₂ Film Growth and Device Results

Substrates with Cu/In molar ratios of 0.92 and 0.95 were selenized at 400 and 450°C using a $\text{H}_2\text{Se}/\text{Ar}$ gas mixture of 0.7% at a flow rate of 72.5 sccm for 2 hr. The heat-up time was 45 minutes and the samples were left at temperature in flowing Ar for 1 hour after the H_2Se gas was turned off. The cool down time was 4-5 hours. The composition of the films was determined using EDS and the structure of the films characterized using X-ray diffraction. $\text{CuInSe}_2/\text{CdS}$ cells (area = 0.09 cm^2) were made on selected substrates.

Table 2-1 summarizes the composition and best I-V parameters (8 to 12 cells were made on each substrate). The composition of all samples was nearly the same and, from XRD measurements, all films were single phase indicating complete reaction. The best device results were made on films grown at 400°C and the performance was independent of the Cu:In ratio. The best cell had an efficiency of 6.8% with $V_{oc}=0.36\text{V}$, $J_{sc}=32\text{ mA/cm}^2$, and $\text{FF}=56\%$.

Figure 2-3. SEM micrograph of a Cu/In bilayer.

Table 2-1

Composition and Device Results Using Selenized CuInSe₂ Films

Temp °C	Cu/In %	Cu %	In %	Se %	V _{oc} * V	Jsc mA/cm ²	FF %
400	0.92	26	26	48	0.36	32	56
400	0.95	25	26	49	0.35	33	55
450	0.92	26	26	48	0.28	32	45
450	0.95	25	26	49	0.31	32	49

In a series of kinetic studies, Cu/In layers with molar ratio of 0.92 were selenized at 400°C in a 3.43% by weight H₂Se/Ar gas mixture flowing at 35 sccm for reaction times from 0.33 to 7 hours. All films were nominally 2 microns thick and had similar compositions as determined by EDS measurements. Further, XRD analysis indicated that the films were single phase CuInSe₂. Thus, the reaction time to convert the Cu/In layers to CuInSe₂ is less than 20 minutes, consistent with the closed ampoule results.

Cu/In layers with a molar ratio of 0.92 were selenized for 60 minutes at 400°C using a range of H₂Se concentrations from 2.9 to 8% by weight (Ar balance) at a total flow rate of 35 sccm. The substrates were placed on the bottom of the quartz tube or on a graphite or ceramic holder. No significant change in film composition was seen over this range of H₂Se concentration. Within a selenization run, the surface features of the sample closest to the gas outlet exhibited a greater degree of surface texture (structures of the order of 5 to 12 microns) than the sample at the gas inlet (structures of the order of 2 to 5 microns). The more textured samples had slightly higher Cu content. Further, the overall uniformity of the films depended to some extent on the substrate holder as discussed below. Devices made on selected samples from these depositions had efficiencies less than 5%. Non-uniformity in selenized films was found to be, in part, associated with the ceramic or graphite block used as a substrate holder. Se species were being absorbed in the substrate holder and released from the substrate support during subsequent runs, causing selenization reactions to begin before the intended introduction of the selenium species. Further, the H₂Se gas may be preferentially dissociating when in contact with the substrate holder creating a higher localized concentration of Se near the edge of the substrate. CuInSe₂ films grown without the substrate holder sitting on the bottom of the quartz reactor, were significantly more uniform in appearance. In order to prevent the absorption of the selenium into the substrate holder, sealed graphite was tested. When a new sealed graphite holder was used for each run, the uniformity of the CuInSe₂ films improved.

2.2.5 Discussion and Future Work

A system for growing CuInSe_2 films by selenizing Cu/In layers has been designed, built and tested. Two major problems, the effect of substrate holder material and control of the Cu:In ratio, were identified and corrected. Single phase CuInSe_2 films were grown at different growth temperatures, gas flows/ concentrations and reaction times. The Cu/In layers are converted to CuInSe_2 films in less than 20 minutes and little effect of H_2Se gas concentration on the film composition was observed. CuInSe_2 devices with efficiencies of 7% were made.

Future work will be directed to improving the reproducibility, optimizing the Cu/In ratio and relative thicknesses, and studying the film growth mechanisms.

SECTION 3.0

BANDGAP MODIFIED CuInSe₂ SOLAR CELLS

3.1 INTRODUCTION

Analysis of high efficiency CuInSe₂ cells indicates that the V_{oc} is limited by Shockley-Read-Hall recombination in the CuInSe₂ absorber layer (10). This suggests that V_{oc} can be increased by increasing the bandgap of the CuInSe₂ near the heterojunction interface. A proposed band diagram where the band gap is modified by alloying with Ga is shown in Figure 3-1. If the higher bandgap region is sufficiently thin compared to the depletion width, a barrier to photogenerated electron transport can be prevented and there should be no loss in J_{sc} . This method of enhancing solar cell efficiency has been demonstrated for Schottky barrier GaAs cells employing a thin AlGaAs layer (11).

The approach taken to forming CuInSe₂ layers with an increased bandgap region near the surface has been to form thin Cu(InGa)Se₂ layers over CuInSe₂. Initially, uniform Cu(InGa)Se₂ films were deposited to establish the capability to deposit device quality Cu(InGa)Se₂ by four source evaporation in a two-step process. Then CuInSe₂/Cu(InGa)Se₂ layers were deposited by several deposition sequences and devices were made.

3.2 UNIFORM Cu(InGa)Se₂

Cu(In_{1-y}Ga_y)Se₂ films were deposited on glass/Mo substrates with $0 < y < 0.40$. Cu(InGa)Se₂/(CdZn)S cells were made with evaporated In-doped (CdZn)S and completed with sputtered ITO and Ni bus bars. The most reliable way to determine the bandgap was found to be extrapolation of the long wavelength spectral response edge. The composition, y , was then determined using the results of Dimmler, et al. (12). The composition was also determined by XRD which gave reasonable agreement. Finally, the bandgap and composition were also determined from the measured optical properties of witness slides deposited on glass. This gave smaller values for the bandgap, probably due to a difference in temperature of the uncoated glass witness slides during the deposition since the temperature is controlled by a thermocouple imbedded in a 7059/Mo substrate. The Cu(InGa)Se₂ depositions were done in two steps at a substrate temperature of 350°C and at 450°C. However, the temperature of the glass witness slides were estimated to have been ~50°C cooler. This may have inhibited Ga incorporation. Furthermore, it has been reported that higher substrate temperatures (>500°C) are needed for Cu(InGa)Se₂ to produce good film morphology and cell results (13,14).

Figure 3-1. Proposed band diagram for CuInSe₂/Cu(InGa)Se₂/(CdZn)S:In solar cell.

Table 3-1 shows the bandgap determined from the spectral response, composition, and best cell results for the uniform Cu(InGa)Se₂/(CdZn)S cells. The V_{oc} increases with the Ga content as expected although the increase is not as much as expected for the shift in bandgap. The highest V_{oc} was obtained at y=0.41. The FF, and therefore efficiency, decreased as the Ga content increased. The spectral response curves show a strongly voltage dependent loss in collection at longer wavelengths which suggests that the collection length may be small. While no additional effort was made to improve the efficiency of homogeneous Cu(InGa)Se₂ devices, these cells served to evaluate the four source thermal evaporation and establish the capability to deposit Cu(InGa)Se₂.

Table 3-1. CuIn_{1-y}Ga_ySe₂ Cell Results*

#	E _g (eV)	y	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff (%)
32072	1.10	0.17	0.51	28	58	7.8
32073	1.11	0.19	0.50	28	58	7.5
32075	1.26	0.41	0.56	16	51	4.3
32076	1.06	0.10	0.45	31	62	8.3

* Measured at 32°C.

3.3 CuInSe₂/Cu(InGa)Se₂ CELLS

3.3.1 Approaches and Fabrication

Three approaches were used to modify the bandgap in the space charge region of CuInSe₂ films: 1) Cu, In, and Ga layers were deposited on CuInSe₂ films with no substrate heating and then Se deposited with the sample at 400°C to form a thin Cu(InGa)Se₂ layer; 2) a graded Cu(InGa)Se₂ layer was produced by increasing the Ga source temperature during the Cu deficient step; and 3) a thin Cu(InGa)Se₂ layer was deposited on completed CuInSe₂ films which were re-inserted in the evaporator. The CuInSe₂/Cu(InGa)Se₂ layers were deposited on glass/Mo substrates and on glass for optical measurements. Evaporated In-doped (CdZn)S films with thickness $\approx 1.5 \mu\text{m}$, 10-15% Zn, and sheet resistance $\approx 50\Omega/\square$ were deposited on CuInSe₂/Cu(InGa)Se₂. Devices were completed with sputtered ITO and Ni contacts.

Cu and In layers were deposited by electron-beam evaporation on the surface of CuInSe_2 films. The samples then had a Ga layer deposited by open boat evaporation. Finally Se was deposited while the substrate was held at 400°C . The thicknesses of the Cu/In/Ga/Se layers were selected to give Cu(InGa)Se_2 layers 150 to $1000\text{\AA}$ thick. Devices made with these samples did not show any enhancement in V_{oc} over standard CuInSe_2 devices and the I-V characteristics with the thicker Cu(InGa)Se_2 layers indicated formation of a blocking diode.

Graded Cu(InGa)Se_2 films were also deposited by the two step evaporation process with the Ga source temperature ramped up during the second step, with the substrate at 450°C , to form a graded bandgap film. The Ga source temperature range was determined to give a film with 25% Ga at the surface based on the uniform Cu(InGa)Se_2 films deposited previously. Thus the film bandgap would be graded from 1.0-1.2 eV. Optical transmission and reflection of the composite $\text{CuInSe}_2/\text{Cu(InGa)Se}_2$ films, measured on witness films deposited on glass, show a shift in the bandgap without a broadening of the absorption edge. This indicates that the Ga diffused through the CuInSe_2 resulting in bulk Cu(InGa)Se_2 films. The best I-V results from cells made from layers in which all or half of the second deposition step was graded are given in Table 3-2. These results are similar to those obtained with uniform Cu(InGa)Se_2 with an increased V_{oc} , but lower J_{sc} and FF.

Table 3-2. Best Cell Results with Graded Cu(InGa)Se_2 Layers

Sample #	V_{oc}^* (V)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)	Grading
32078.23	0.50	26	58	6.9	2nd layer
32079.23	0.45	30	50	6.3	1/2 2nd layer

* Measured at 32°C .

The third approach to $\text{CuInSe}_2/\text{Cu(InGa)Se}_2/(\text{CdZn})\text{S}$ cells used thin Cu(InGa)Se_2 layers deposited onto previously deposited CuInSe_2 films at $300\text{--}450^\circ\text{C}$ with a 1.2eV bandgap, ~25% Ga, and thicknesses ranging from $0.1\text{--}0.4\mu\text{m}$. In addition, glass, $\text{CuInSe}_2/\text{glass}$, and Mo/glass substrates were included for characterization. Optical measurements on $\text{Cu(InGa)Se}_2/\text{CuInSe}_2/\text{glass}$ samples showed no shift in the bandgap from the CuInSe_2 film indicating that the Ga did not diffuse throughout the film during the deposition. The thicknesses of the Cu(InGa)Se_2 films on glass were determined by Dektak profilometer. Compositional measurement by optical or XRD characterization was difficult because of the thinness of the

Cu(InGa)Se₂ films. However, the bandgap, and therefore the Ga content, was determined for Cu(InGa)Se₂ layers deposited directly on glass/Mo substrates during the same deposition in which the CuInSe₂/Cu(InGa)Se₂ layers were formed. Cu(InGa)Se₂/(CdZn)S cells were then made. While these cells generally had very poor diode characteristics, spectral response measurements were made and the long wavelength response used to determine E_g.

3.3.2 CuInSe₂/Cu(InGa)Se₂ Cell Results

CuInSe₂/Cu(InGa)Se₂/(CdZn)S:In cells were made using the third approach above with different thicknesses and composition of the Cu(InGa)Se₂ layers. The best cell results with a 1.15eV bandgap Cu(InGa)Se₂ layer are listed in Table 3-3 along with the results for a high efficiency CuInSe₂/(CdZn)S cell for comparison. With the 0.4μm thick Cu(InGa)Se₂ layer, V_{oc} was close to that with the uniform Cu(InGa)Se₂ absorber reported above, but J_{sc} was much smaller. As the Cu(InGa)Se₂ thickness was reduced, V_{oc} decreased and J_{sc} increased.

I-V and spectral response curves for a cell with a 0.1μm, 1.2eV bandgap, Cu(InGa)Se₂ layer are shown in Figures 3-2 and 3-3. The spectral response, particularly at reverse voltage bias, shows collection out to 1.0eV, the CuInSe₂ bandgap. However, the collection is strongly voltage dependant, particularly at long wavelengths, resulting in the low J_{sc} and FF. In addition, the I-V and spectral response curves are shown before V_{oc} was maximized by heat treatment in air at 200°C. The lower V_{oc} indicates that CuInSe₂ is more resistive and, therefore, space charge width of the CuInSe₂ is greater (15). As a result, there is improved field collection and J_{sc} and FF are increased, particularly in the long wavelength spectral response. Similar behavior was reported by Klenk, et al. (16) for Cu(InGa)Se₂ cells in which the resistivity was increased by hydrazine treatment and by Tuttle, et al. (17) for CuInSe₂/Cu(InGa)Se₂ cells. These results suggest that there may be a smaller diffusion length when Ga is present. In addition, there may be a barrier in the conduction band to the collection of photogenerated carriers (11) which increases as the Cu(InGa)Se₂ thickness increases. Such a barrier would have less effect on the collection as the space charge width is increased.

Table 3-3. CuInSe₂/Cu(InGa)Se₂ Cell Results

Cu(InGa)Se ₂ Thickness (μm)	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	eff (%)
0.4	0.49	22	48	5.0
0.2	0.47	24	38	4.4
0.1	0.45	31	33	4.5
0	0.42	37	69	10.5

Figure 3-2. I-V characteristics of $\text{CuInSe}_2/\text{Cu(InGa)Se}_2$ cell;
 1) after 14 hours heat treatment in air at 200°C to optimize V_{oc} ;
 2) after only 2 hours heat treatment.

Figure 3-3. Spectral response of $\text{CuInSe}_2 / \text{Cu}(\text{InGa})\text{Se}_2$ cell; 1) after 14 hour heat treatment, measured at J_{sc} ; 2) after heat treatment, at -1V bias; 3) after only 2 hours heat treatment, at J_{sc} .

The spectral response curves in Figure 3-3 were measured without light bias. When the $\text{CuInSe}_2/\text{Cu(InGa)Se}_2$ cells are measured with light bias, a large peak occurs at the $(\text{CdZn})\text{S}$ band edge which indicates that the $(\text{CdZn})\text{S}:\text{In}$ is strongly photoconductive (18). This may be due to interdiffusion of species during the $(\text{CdZn})\text{S}$ evaporation and subsequent heat treatments. This photoconductivity makes further quantitative analysis of these cells difficult. The described behavior of these cells has been observed despite several variations in deposition conditions. This has included changes in the substrate temperature during the Cu(InGa)Se_2 depositing from 300-450°C and changes in the composition of the CuInSe_2 , Cu(InGa)Se_2 , and $(\text{CdZn})\text{S}:\text{In}$ films.

3.4 DISCUSSION - FURTHER WORK

The cell results presented above have demonstrated that V_{oc} can be increased while generating carriers out to the CuInSe_2 band edge and suggest that this configuration can be used to enhance CuInSe_2 cell performance. However, several problems remain. The $(\text{CdZn})\text{S}$ needs to be made less photoconductive by modifying the deposition conditions further or by depositing very thin CdS layers by the solution growth method. Also the collection in the $\text{CuInSe}_2/\text{Cu(InGa)Se}_2$ absorber needs to be improved to increase J_{sc} and FF. The selenization process will allow other alternatives for deposition of bandgap modified CuInSe_2 layers using either Ga or S and these will be explored. Finally, the effect of the addition of Ga on the diffusion length can be studied using the bifacial spectral response method discussed in Section 7.1 below.

SECTION 4.0

WINDOW LAYERS

The primary goal of research on window layers was to increase J_{sc} while maintaining high V_{oc} and FF. Cells with high J_{sc} were reported in the previous contract (19) using thin solution grown CdS although these cells had low V_{oc} and FF. High efficiency cells with thin CdS/ZnO have been reported elsewhere (20,21). In this report results for cells with solution grown CdS deposited from different baths will be reported. Cells have been fabricated with ZnO and ITO as transparent conducting layers.

4.1 WINDOW LAYER DEPOSITION

4.1.1 Solution Growth of CdS

The CdS films were deposited on glass and glass/Mo/CuInSe₂ substrates from the following formation reaction:

where A is a complexing agent. Thiourea was used as the source of sulfide in all baths. Either triethanolamine (TEA) or ammonia was employed as the complexing agent and cadmium chloride or cadmium acetate was used as the source of cadmium.

The experimental set-up consisted of a one liter glass reaction vessel immersed in a controlled temperature bath and equipped with a mechanical stirrer and pH monitor. Up to six substrates were held in a vertical position in the reaction vessel.

Three solution grown CdS bath chemistries were evaluated: 1) a TEA-based solution consisting of 0.05M cadmium acetate, 0.10M thiourea, 1.3M ammonia and 0.37M TEA (22); 2) an ammonia-based solution consisting of 0.10M cadmium acetate, 0.20M thiourea and 0.80M ammonia (23); and 3) a solution of 0.02M cadmium chloride (hydrate), 0.065M ammonium chloride, 0.15M thiourea and 0.4M ammonia (24). Reaction temperatures ranged from 30°C to 85°C. The bath pH was set by adjusting the amount of ammonia in the solutions. Finally, the effects of stir rate and various bath additives, including a wetting agent, TRITON-X-100, and a crystal habit modifier, d-sorbitol, were studied.

4.1.2 ZnO Deposition

Al-doped ZnO was deposited by rf magnetron sputtering from pressed ZnO targets doped with 0.2% or 1.0% Al₂O₃ by weight. The best films from the target with 1.0% Al₂O₃ were 0.8-1.0μm thick and had a sheet resistance of 15-20Ω/□. The lowest sheet resistance from the 0.2% Al₂O₃ was comparable but the films were less uniform over the 3"x3" substrate array. In addition, the

sheet resistance with the higher Al content are more stable in heat treatments. After an 8 hour treatment in air at 200°C, the sheet resistance of one piece increased from 22 to 45 $\Omega/\square$. Films from the old target with the lower Al concentration would increase by 1-2 orders of magnitude. Finally, there is greater free carrier absorption above 1000nm with the higher Al content as shown in Figure 4-1.

Sputtered ITO films with 20 $\Omega/\square$ and 0.2 μm thickness have also been used. Devices were fabricated with ZnO, ITO, and ZnO/ITO layers on the solution grown CdS films.

4.2 SOLUTION GROWN CdS-CELL RESULTS

CuInSe₂/CdS cells were fabricated from the three different solution grown CdS baths. Typically, twelve cells were fabricated on each CuInSe₂/CdS substrate; 6 cells with ITO as the contact to the CdS, and six with ZnO. The best cell results are listed in Table 4-1. The highest efficiencies were achieved with the bath using cadmium chloride as the source of cadmium. The pH was 10.2 for this CdS bath and comparable results were attained at 40°C and 50°C. CdS films deposited on glass using the same conditions, at 50°C for 8 minutes, were ~100nm thick. Films deposited at higher pH, 10.9, and higher temperature, 70°C, resulted in cells with lower V_{oc} and J_{sc} , and shunting I-V behavior. V_{oc} , J_{sc} , and FF were all lower on cells with CdS films deposited from the baths using cadmium acetate as the cadmium source. Addition of a wetting agent or a crystal habit modifier did not produce any apparent change in the films or improvement in cell results.

The cells with CdS/ZnO generally have higher V_{oc} and FF than those with CdS/ITO. The difference is shown by the two cells listed for the cadmium chloride bath in Table I which are on the same substrate. The change in V_{oc} may result from pin-holes in the CdS where the ZnO or ITO comes in direct contact with the CuInSe₂. This provides a second diode in parallel to the CuInSe₂/CdS diode with a different dark diode current, J_0 . Results of CuInSe₂/ZnO and CuInSe₂/ITO cells (25), show that with ZnO the V_{oc} is larger than with ITO indicating a smaller J_0 . Cells with thin, <0.8 μm , evaporated (CdZn)S, where pin holes are clearly present, also have higher V_{oc} with ZnO than with ITO.

Cells fabricated with the solution grown CdS have reached their highest efficiency with no heat treatment or, at most 1/2 hour at 200°C in air. This is in contrast to cells fabricated with evaporated CdS or (CdZn)S on identical CuInSe₂ layers which need 8-24 hours heat treatment to be optimized. The I-V characteristic and spectral response of the best CuInSe₂ cell with solution grown CdS are compared in Figures 4-2 and 4-3 with those of a typical cell with an evaporated (CdZn)S:In/ITO window.

Figure 4-1. Optical transmission of ZnO:Al films showing increased free carrier absorption with 1% Al. An ITO film is also shown.

Table 4-1. Cell Results* with Solution Grown CdS.

Bath Constituents	Contact	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)	Eff (%)
Cd chloride/thiourea/ammonia	ZnO	0.398	39.8	63.3	10.0
	ITO	0.381	40.5	55	8.5
Cd acetate/thiourea/ammonia	ITO	0.358	31.9	49	5.6
Cd acetate/thiourea/TEA	ZnO	0.372	38.6	48	6.9

* Measured at 32°C, J_{sc} normalized to 100 mW/cm² AM1.5 global spectrum.

Figure 4-2. I-V characteristic of a $\text{CuInSe}_2/\text{CdS}/\text{ZnO}$ cell with solution grown CdS compared to a $\text{CuInSe}_2/(\text{CdZn})\text{S}:\text{In}/\text{ITO}$ cell with evaporated $(\text{CdZn})\text{S}$.

Figure 4-3. Spectral response of CuInSe_2 cells with solution grown CdS and evaporated $(\text{CdZn})\text{S}$.

The (CdZn)S:In is 1.5 μm thick with 15% Zn and a 2.6 eV bandgap. The cell with evaporated (CdZn)S had higher V_{oc} , 0.425V, and FF, >68%, which gave 9.4% efficiency. The long wavelength quantum efficiency is similar for both cells while the cell with solution grown CdS had enhanced quantum efficiency below 500nm.

The most promising approach to higher efficiency is with solution grown CdS since higher J_{sc} has been achieved and comparable FF and V_{oc} should be achievable. Future work will focus on optimizing the CdS deposition for thinner layers and more reproducible cell results and on controlling the ZnO resistivity to possibly improve V_{oc} . In addition, alternative window materials will be investigated.

SECTION 5.0

INNOVATIVE CELL DESIGN

All high efficiency $\text{CuInSe}_2/\text{CdS}$ solar cells have been made using a substrate device configuration where the CuInSe_2 is grown on a Glass/Mo substrate. In a previous report (19), we assessed CuInSe_2 cells in a superstrate configuration where the CuInSe_2 is deposited onto glass/ITO/CdS. This device configuration could be advantageous for fabricating monolithic integrated modules, since generic manufacturing technology could be transferable to CuInSe_2 modules. Additionally, the superstrate device structure offers new options for monolithic cascade cells using CuInSe_2 .

Figure 5-1 shows a schematic of a $\text{CuInSe}_2/\text{CdS}$ solar cell in the superstrate device configuration. CdS films with thicknesses from 0.1 to 1.0 μm , were evaporated on glass sputter coated with ITO with a sheet resistance of 10 $\Omega/\square$. Both In-doped and undoped CdS films were used with the resistivity of the films varying from 10 to 10⁻³ $\Omega\text{-cm}$. The CuInSe_2 films were deposited by three source thermal evaporation in a single step, in contrast to the two step procedure used for high efficiency substrate CuInSe_2 cells (26), at substrate temperatures from 300°C to 400°C. The CuInSe_2 films were highly oriented along the (112) axis and were specular with smaller grain structure than films used for high efficiency devices. The devices were completed by depositing a 0.07 cm^2 Pt dot to provide the back contact to the CuInSe_2 .

Figure 5-2 shows the I-V curve (at 32°C) for the best cell using the superstrate device configuration (glass/ITO/CdS/ CuInSe_2 /Pt) which had an efficiency=5.9% with V_{oc} =0.33V, J_{sc} =35 mA/cm^2 , and FF=53%. The J_{sc} , when corrected for reflection losses, is comparable to currents measured on high efficiency cells. Cells have also been made with comparable CuInSe_2 layers, deposited in a single layer and with similar composition, in the substrate configuration (27). The CuInSe_2 in these devices was specular and had similar grain structure. The highest V_{oc} obtained with these cells was also only 0.33V. We speculate that in each case, the low V_{oc} may be associated with a high density of grain boundaries.

Table 5-1 summarizes the I-V characteristics of CuInSe_2 superstrate devices. Included are different CdS thicknesses and both In-doped and undoped films along with three different substrate temperatures, T_{sub} =300-400°C, for the CuInSe_2 deposition. There is little effect of the CdS thickness or doping on the device performance. For all the devices there is a dramatic light to dark cross-over in the I-V curves. This is probably a result of Cu diffusion into the CdS during the growth of the CuInSe_2 film resulting in highly compensated and

Figure 5-1 Superstrate Configuration

Figure 5-2 I-V Curve for CuInSe₂ Superstrate Cell

photconductive CdS. There is a correlation with the device performance and the CuInSe₂ substrate temperature with the best devices deposited at 300°C. The cells have low FF which is partly due to series resistance from the ITO/CdS layers and some cells had a second junction which was probably due to a non-ohmic Pt contact. Alternate metals and surface conditioning prior to the metal deposition are being evaluated to improve the contact.

Table 5-1. CuInSe₂ Superstrate Cells

V _{oc}	J _{sc}	FF	Eff	CdS Thickness/ Dopant	T _{sub}
0.34	34	47	5.1	0.1/None	300°C
0.33	34	53	5.5	0.6/In	300°C
0.33	34	42	4.4	1.0/None	300°C
0.34	27	29	2.5	0.6/In	350°C
0.32	9	46	1.3	0.5/In	400°C

Measured at 32°C

SECTION 6.0

CdTe SOLAR CELLS

6.1 BACKGROUND

All thin film CdTe-based solar cells having reported efficiencies greater than 10% share three features: 1) a superstrate configuration; 2) a CdTe growth step or heat treatment step at 400°C or greater; and 3) a CdTe contact containing a group Ib metal (28-33). The CdTe for these high efficiency cells has been deposited by CSVT (28), electro-deposition (29-31), screen printing (33), and MBE (34). The highest reported efficiency for a CdTe thin film cell was 12.3% (31). Previously, we reported on a process for fabricating cells using physical vapor deposition (PVD) CdTe films (35,36). While these devices utilized the three fabrication features, the best device parameters obtained for a single cell were only: $V_{oc} = 665$ mV; $J_{sc} = 20$ mA/cm²; and FF = 65%. The process was irreproducible with regard to V_{oc} and FF.

In view of the irreproducibility and low V_{oc} and FF obtained using PVD films, we initially investigated electrochemical deposition of CdTe and processing methods. An electrochemical system was designed, set up, and characterized. Eighty depositions were performed onto CdS/ITO substrates, yielding single phase 2 micron thick films. Device fabrication was limited to only a few runs. This approach was superseded in view of promising results that emerged from the alternate path described below.

Collaborative experiments with AMETEK were conducted to identify limitations of PVD CdTe and CdS layers for superstrate cells. The work with AMETEK was a natural extension of ongoing work between IEC and AMETEK on four terminal tandem cells (37).

IEC and AMETEK exchanged CdS, CdTe, and contacts in a round-robin of device fabrication. AMETEK had a process in place for making high efficiency devices and agreed to substitute IEC's PVD materials for their own at selected steps. We identified four fabrication steps for evaluation: 1) CdS layer; 2) CdTe layer; 3) high temperature heat treatment; and 4) back contact. Processing of IEC evaporated CdS/CdTe material at AMETEK with their heat treatment and Cu-doped ZnTe contact yielded devices with $V_{oc} \sim 720$ mV, $J_{sc} \sim 20$ mA/cm², and FF ~ 66% which represents significantly higher performance than we had achieved with PVD films using IEC's post-deposition processing. Device results from the entire exchange (Table 6-1) indicated that the CdS and CdTe deposition techniques were less critical than post-deposition processing for determining cell efficiency.

Table 6-1 Device results of IEC-AMETEK
Materials and Processing Exchange

CdS	Processing Step			Device Parameters			
	CdTe	HT	ZnTe:Cu	Voc (V)	Jsc (mA/cm ²)	FF (%)	Area (cm ²)
AM-spray	AM-echem	AM-CdCl ₂	AM-evap	750	19	60	1
IEC-evap	AM-echem	AM-CdCl ₂	AM-evap	704	16	60	1
AM-spray	IEC-evap	AM-CdCl ₂	AM-evap	740	18	56	0.08
IEC-evap	IEC-evap	AM-CdCl ₂	AM-evap	720	20	66	0.1
AM-spray	AM-echem	IEC	IEC-evap	700	19	44	0.4
IEC-evap	IEC-evap	IEC	IEC-evap	460	18	30	0.07

Accordingly, efforts under this Task were re-directed from electrodeposition studies to investigating post-deposition heat treatments and contacts.

6.2 INTRODUCTION

We have developed an optimization procedure which has led to a verified efficiency approaching 10% and more reproducible device results using PVD CdTe and CdS films. Prior to high temperature heat treatment at 400°C, the CdTe surface is coated with a 0.5 μm thick layer of CdCl₂, which is a known fluxing or crystallization agent in CdTe and is utilized in the preparation of screen printed CdTe films (38-40). The first reported use of CdCl₂ in post deposition processing (as a recrystallization agent) was by AMETEK (41). The optimum heat treatment temperature needed to obtain high J_{sc} is ~400°C when CdCl₂ is used, 150°C lower than is needed without CdCl₂ (35). Semi-transparent metal contacts permitted bifacial I-V and spectral response measurements to be made on the devices at each stage of optimization. After contacting, devices were optimized in two steps: 1) mild heat treatment at 150°C to maximize J_{sc} and 2) chemical treatment to enhance V_{oc} and FF.

Sections 6.3 and 6.4 present a detailed analysis of the effects of the 400°C heat treatment and CdCl₂ layer on the bulk and surface properties of the CdTe and device performance of PVD CdS/CdTe solar cells. We describe devices having V_{oc} as high as 0.8 V and FF up to 73%. The post-deposition optimization procedure produced similar device results with Ametek's electrodeposited CdTe and CdS films, suggesting a high degree of compatibility of CdTe cell processing with different CdTe

deposition techniques. Sections 6.5 through 6.10 contain results of related studies carried out in support of the primary task, such as investigation of alternate window layers, CdTe deposition conditions, and stability of cell performance over time. Despite achievement of nearly 10% efficiency, higher efficiencies are possible by adopting a more transparent window layer and by reducing the V_{oc} -limiting mechanism. Conclusions are presented in Section 6.11.

6.3 EXPERIMENTAL

6.3.1 Device Fabrication

The CdTe/CdS/ITO/7059 devices were prepared in a superstrate configuration by first sputter depositing 400 nm of ITO onto cleaned 1"x1" Corning 7059 glass substrates, resulting in a transparent conductive coating having 95% transmission at 900 nm and a sheet resistance of 10 ohm/□. Undoped CdS films 1 to 2 microns thick were then deposited by PVD from an effusion source bottle using high purity CdS powder onto the ITO/7059 superstrate. The CdS films typically had a resistivity of 10 ohm-cm.

The CdTe films were also deposited by PVD, using high purity (5N) CdTe powder. Nominally two micron thick films were deposited under a range of conditions: substrate temperature, 250°C to 300°C; and growth rate, 0.01 to 0.25 microns per minute. The growth rates and substrate temperatures used correspond to the single phase region of growth for CdTe.

Following CdTe deposition, a 1% (wt.) solution of $CdCl_2$ in CH_3OH was prepared by dissolving anhydrous $CdCl_2$ in electronic grade CH_3OH at room temperature. Five to seven drops of the solution were dispensed onto the CdTe using an eyedropper. The samples were dried in an oven at 50 to 90°C for several minutes. The solubility of the $CdCl_2$ in CH_3OH is only 1.7% at room temperature, and as the CH_3OH evaporates, the solution becomes supersaturated, leading to uniform precipitation of $CdCl_2$ onto the CdTe surface. Based on the volume of solution, concentration, substrate area and density, the thickness of the $CdCl_2$ layer is estimated to be 0.5 μm . Immediately following the $CdCl_2$ application, the glass/ITO/CdS/CdTe was heat treated in air in a tube furnace at a temperature of 400°C for 30 minutes. After heat treatment, the surface of the samples was rinsed in de-ionized water for 30 seconds.

Semi-transparent contacts consisting of typically 80Å Cu and 100Å Au were deposited onto the CdTe surface by electron beam evaporation. To minimize oxidation of the thin Cu film, the bell jar was backfilled with 4% H_2 -Ar, and a Ti flash evaporation was performed just prior to the Cu deposition, resulting in a system

pressure of 1×10^{-7} Torr. The effect of Cu and Au thickness was investigated over the range: Cu, 20Å-100Å and Au, 80Å to 1000Å. Indium-lead solder was used to make a robust contact to the ITO.

The first step of device optimization following deposition of the Cu/Au contact was a heat treatment in either flowing air or in 4% H₂-Ar in a tube furnace at 150°C for 30 min to 2 hrs. Next, the samples were chemically treated by immersion in either 0.02 M Br₂-CH₃OH for 5 seconds or in 95% N₂H₄-H₂O for up to 5 minutes. The CdTe/CdS structures were characterized at each stage of the post-deposition process to correlate processing steps, structural changes and device behavior.

6.3.2 Film and Device Characterization

The surface morphology of the CdTe layers was examined by optical microscopy (OM) at 100 - 800X and by scanning electron microscopy (SEM) at 1000 and 5000X. Scanning x-ray diffraction (XRD) with 35 kV CuK α radiation and Bragg-Bretano focusing geometry was used to characterize film structure and to determine the precision lattice parameter of the CdTe films at each step of the device processing and optimization.

Auger Electron Spectroscopic (AES), Secondary Ion Mass Spectroscopic (SIMS), and X-ray Photoelectron Spectroscopic (XPS) analysis were performed by the Solar Energy Research Institute (SERI) on samples of CdTe/CdS/ITO/Glass films at each step of processing. The AES and SIMS measurements were performed as a function of depth, resulting in depth profiles for each processing step. Surface and depth profiles AES were carried out for Cd, Te, S, O, Cu, and Au. The SIMS profiles were made for ¹²⁵Te, ³⁴S, O, ³⁷Cl, C, Cu, and Au. Quantitative analysis of atomic levels in each layer was not possible since absolute standards were not available, but relative changes in the observed levels were used primarily as a measure of interdiffusion.

XPS of the surface region of each sample was carried out for binding energies from -1000 eV to 0 eV. In particular, the Cd 3d_{5/2} (E = -405 eV) and Te 3d_{5/2} (E = -576 eV) peak area ratios were monitored for each processing step. High resolution XPS was used to infer the presence of CdTe, CdCl₂, and TeO₂ in the near surface region of the samples.

Optical transmission and reflection was measured over the range 300 to 1400 nm using a Perkin-Elmer spectrometer with an integrating sphere. The effects of processing on the fundamental band edge and sub-bandgap absorption were investigated.

Current-voltage (I-V) characteristics and spectral response were measured after contacting and after optimization steps. The I-V measurements were made in the dark and under illumination through both the CdS and the Cu/Au contact. Measurements were made at

32°C. Dark and illuminated measurements were performed as a function of temperature and intensity on selected samples.

6.4 RESULTS

6.4.1 Effect of CdCl₂ Application and Drying Technique

The effect of the CdCl₂ solution strength was investigated by diluting from the maximum solubility limit in CH₃OH (1.7%) to 0.2%. Compared to the control piece (1.7% CdCl₂), V_{oc} was unchanged, FF decreased slightly, but J_{sc} was only 3-4 mA/cm² compared to 20-21 mA/cm². The strong influence of CdCl₂ on improving J_{sc} was verified by applying the full strength solution to the top of a tilted substrate. Visual inspection confirmed that there was less CdCl₂ at the top than at the bottom. Table 6-2 shows the striking gradient in cell performance especially J_{sc}, with all parameters increasing towards the bottom (i.e., more CdCl₂).

Table 6-2
Cell test parameters for CdCl₂
applied to tilted substrate #40663.121

<u>Cell</u>	<u>Position</u>	V _{oc} (V)	J _{sc} (mA/cm ²)	FF (%)
1	top	.545	5	45.6
2	top-mid	.558	7	47.2
3	bot-mid	.581	17	55.7
4	bot	.588	19	57.5

The effect of doubling the CdCl₂ was investigated by applying a second coating after the first had dried. No difference in cell performance was noted over the control (single coating) piece. Therefore, we elected to use the 1.7% solution for the rest of our studies.

The CdCl₂ drying technique was investigated to determine its influence on uniformity and performance. Initially, the CdCl₂-CH₃OH solution was dispensed onto the surface with an eyedropper and the sample was allowed to dry by resting on the lab bench. During the summer months when high humidity, this resulted in visually non-uniform coating and poor device performance.

When samples are coated and dried on the lab bench, they are exposed to the ambient room conditions (temperature and humidity). In cases of high humidity, the CdCl₂-CH₃OH solution does not wet the CdTe surface and results in beading up of the solution as the drying progresses. We speculated that as the

methanol evaporated, which cools the sample, the deliquescent nature of the CdCl_2 and methanol gradually incorporated water into the solution. Such a solution has a very high solubility for CdCl_2 which when coupled with its non-wetting characteristics, would result in isolated islands of CdCl_2 instead of a film-like coating, and hence spatial non-uniformity.

To obtain uniform coatings, the samples must either be kept away from the atmosphere or kept at an elevated temperature to enhance the drying rate. We found that coating the samples in a warm (50°C) Petri dish, covering, and placing in a drying oven at 100°C for 30 sec to 1 minute gives consistently uniform CdCl_2 coatings.

6.4.2 Effect of 400°C Air Heat Treatment

As-deposited, PVD CdTe films on CdS/ITO/7059 substrates are specular and deep grey in appearance, SEM shows sub-micron facets and XRD indicates moderate orientation along the (111) axis of the cubic system (35). After coating with CdCl_2 , the surface took on the features of the CdCl_2 crystallites and exhibited a translucent white textured appearance. After heat treatment in air at 400°C for 30 minutes, the surface was slightly milky but exhibited a larger facet morphology. After rinsing off the CdCl_2 , SEM showed surface of facets dimensions of about one micron.

Changes in structure due to CdCl_2 coating and heat treatment are evident in XRD scans. All reflections for the as-deposited film may be indexed as either the ITO substrate, the wurtzite CdS phase, or the zinc blende CdTe phase and give a precision CdTe lattice parameter of $6.490 \text{ \AA} \pm 0.005 \text{ \AA}$. After coating with CdCl_2 , numerous CdCl_2 reflections are observed. The CdTe and CdS reflections are reduced in intensity somewhat but are otherwise unaltered by the coating.

After heat treatment at 400°C for 30 minutes, the CdTe film became more oriented, the CdTe reflections became sharper, and the CdTe lattice parameter was shifted slightly, to $6.480 \text{ \AA} \pm 0.005 \text{ \AA}$. In addition, reflections due to $\text{Cd}(\text{ClO}_2)_3 \cdot 2\text{H}_2\text{O}$ and CdO appeared in the XRD scan. Additional heat treatment time resulted in further reduction in lattice parameter and/or reduction in the degree of preferred orientation. Significantly, performing the 400°C air heat treatment on a CdTe/CdS/ITO/7059 structure without a CdCl_2 coating resulted in only a slight increase in orientation and no detectable change in lattice parameter or peak widths.

Electrodeposited CdTe films (from Ametek) exhibit an additional tellurium phase in the as-deposited condition. After the heat treatment, the reflections vanish from the scans, and the CdTe

film is restructured in the same way as the evaporated films. Table 6-3 summarizes the change in lattice parameter, (111) intensity, and (111) peak widths for evaporated CdTe and electrodeposited CdTe films.

Table 6-3. X-ray Diffraction Data for CdTe Films before and after 400°C heat treatment. I is the intensity in counts per second (CPS) and FWHM is the full width at half maximum of the (111) reflection.

Deposition Method	Condition	Phases	CdTe a_0 (Å)	I (111) (cps)	FWHM (111)
Evaporated	Initial	CdTe	6.490	940	0.35
Evaporated	HT 30 min	CdTe	6.480	2500	0.18
Evaporated	HT 120 min	CdTe	6.460	2000	0.18
Electrodeposited	Initial	CdTe, Te	6.490	1000	0.20
Electrodeposited	Heat Treat	CdTe	6.478	1850	0.16

AES and SIMS depth profiles of as-deposited films showed moderately sharp CdTe/CdS and CdS/ITO interfaces. In contrast, the SIMS profile for the same film after coating and heat treatment at 400°C for 30 minutes indicated extensive interdiffusion of S, Te, and Cl. In addition, a penetrating surface oxide was found on the CdTe layer.

The optical characteristics of the CdTe/CdS/ITO/7059 structure are changed by the 400°C heat treatment and by contacting as shown in Figure 6-1, which is a plot of $T/(1-R)$ versus wavelength for evaporated CdTe/CdS/ITO/7059: a) as deposited and; b) after CdCl₂ coating and 400°C air heat treatment. The sub-bandgap absorption in the as-deposited case (curve a) is due to free carrier absorption in the ITO layer. A shift in band gap from 1.51 eV before heat treatment to 1.48 eV after heat treatment after the 400°C air heat treatment may account for the difference between curves 6-2a and 6-2b in the region 0.8 to 0.85 μm . Taken together with the XRD results, AES data, SIMS data, and published data on the CdS_xTe_{1-x} system in thin films and single crystals, such a shift in band gap towards lower energy is expected from interdiffusion of S and Te in CdTe and CdS (42-44). Because the CdTe-CdS system is not isostructural at the temperatures of interest (300K-700K), a phase transformation from zinc blende to wurtzite occurs at composition CdS_{0.2}Te_{0.8} (45) and the band gap decreases with increasing S content up to the 20% point at which it reaches a minimum value of 1.3 eV (44). Based on values of E_g and a_0 and the relative changes observed in the SIMS depth profiles, the heat treated films are estimated to contain 1 to 2 mol% sulphur. No change in optical properties was observed on films heat treated at 400°C without a CdCl₂ coating.

Figure 6-1. Optical $T/(1-R)$ spectra for the CdTe/CdS/ITO/7059 structure at two stages of processing: a) as-deposited and; b) as-deposited plus CdCl_2 coating plus 400°C heat treatment and rinse.

The effect of heat treatment ambient (air, H_2/Ar , and N_2) was also investigated. After 30 minutes at $400^\circ C$ in H_2/Ar or N_2 , there was no $CdCl_2$ visible on the $CdTe$ surface. No improvement in cell performance occurred on devices heated in H_2/Ar or N_2 . This suggests that the $CdCl_2$ sublimes in the absence of oxygen. Therefore, all device results reported here were obtained for heat treatment in air at $400^\circ C$.

In summary, the $400^\circ C$ air heat treatment in the presence of a $CdCl_2$ surface layer produces significant structural changes in the $CdTe/CdS/ITO/7059$ structure. These changes are attributed to interdiffusion, recrystallization, and oxidation.

6.4.3 Initial Device Results

Depositing the thin Cu and Au did not produce any detectable change in the $CdTe/CdS/ITO/7059$ structure or morphology of the $CdTe$, CdS or ITO . However, the contact increased the total absorption as expected from transmission and reflection measurements for the Cu and Au on glass (Figure 6-1c).

After contacting, the devices exhibit poor performance when illuminated through the CdS (Figure 6-2a), having a V_{oc} less than 400 mV, J_{sc} less than 10 mA/cm^2 , FF less than 40%, and very pronounced light-to-dark crossover. Surprisingly, the J_{sc} and V_{oc} are comparable or slightly better for the device under illumination through the Cu/Au contact (Figure 6-2b). Quantum efficiency measurements of the as-deposited cells show roughly uniform collection for illumination through the CdS and Cu/Au sides of the device (Figure 6-3).

6.4.4 Effect of $150^\circ C$ Heat Treatment

The $150^\circ C$ air heat treatment produces significant changes in the I-V characteristics (Figure 6-4) and the quantum efficiency (Figure 6-5). For the CdS -illuminated case, J_{sc} increased to 19 mA/cm^2 , and V_{oc} increased to 500 mV. The dark I-V characteristic was not changed by the heat treatment. The quantum efficiency for illumination through the CdS increased uniformly while that for illumination through the Cu/Au contact decreased overall, with the greatest drop occurring in the blue response. These quantum efficiencies resemble those expected for a p-n heterojunction having its depletion layer within the p-type absorbing layer near the metallurgical interface. In such a device, we expect uniform collection for illumination through the n-type window layer, but poor blue response for illumination through the semi-transparent back contact, especially when the $CdTe$ thickness is greater than the minority carrier diffusion length.

Figure 6-2. Bifacial I-V curves for a device after contacting:
a) illuminated through CdS and b) illuminated through Cu/Au contact.

Figure 6-3. Bifacial quantum efficiency of the device of Figure 6-2 after contacting: a) illuminated through CdS and b) illuminated through Cu/Au contact.

Figure 6-4. Bifacial I-V curves for the device of Figure 6-2 after air heat treatment at 150°C for 2 hours: a) illuminated through CdS and b) illuminated through Cu/Au contact.

Figure 6-5. Bifacial quantum efficiency of the device of Figure 6-2 after air heat treatment at 150°C for 2 hours: a) illuminated through CdS and b) illuminated through Cu/Au contact.

AES profiles of the Cu and Au showed that prior to heat treatment at 150°C, the Cu and Au formed two distinct layers, but after heat treatment Cu and Au were interdiffused. From these depth profiles, it is difficult to ascertain the degree to which Cu or Au may have diffused into CdTe. XRD scans of Cu/Au on CdTe/CdS and of Cu/Au on 7059 glass made before and after the 150°C heat treatment, showed only a broad low intensity peak which remained unchanged after heat treatment. This is not surprising given the thinness of the layers: 80 Å Cu and 100 Å Au.

The effect of ambient (air or H₂/Ar) during the 150°C heat treatment was investigated. Equivalent cell results were obtained with either atmosphere. Most results discussed in this report were obtained with air during the 150°C heat treatment.

6.4.5 Effect of Chemical Treatment

An enhancement of the V_{oc} and the fill factor is obtained by the chemical treatment. We have obtained equivalent results by immersing the devices in either 0.02 M/l Br₂-CH₃OH for 5 seconds or 95% N₂H₄-H₂O for 4 to 5 minutes. Figure 6-6 shows the I-V behavior for a device following immersion in the bromine-methanol solution. The V_{oc} increased by 150 mV while the J_{sc} remained constant. (Increases of 50-100 mV were more typically seen). The contact becomes ohmic, as seen in the change in the forward bias portion of the I-V curves between Figures 6-4 and 6-6. The spectral response of the device did not change. The dark I-V curve was dramatically affected by the immersion treatment, resulting in a low series resistance and no light-to-dark crossover. Immersing the samples in either Br₂-CH₃OH or N₂H₄ produced no noticeable change in surface appearance, morphology, XRD pattern, or optical properties. AES showed, however, that the immersion caused depletion of Cd in the near-surface region. XPS analysis additionally shows a drop in the Cd/Te peak area ratio from 1.9 to 0.4. These observations suggest the formation of Cu₂Te or AuTe₂. The role of these intermetallic alloys as ohmic contacts to p-type CdTe is discussed below.

The sequence of optimization steps was tested and found to be crucial to the final performance of the devices. The effect of performing the chemical treatment immediately after contacting, with no heat treatment step, is to enhance V_{oc} with no change in the J_{sc} or spectral response. Without heat treatment, FF was poor (<50%) and relatively unchanged by the chemical treatment. The I-V behavior of such a device is shown in Figure 6-7. Subsequent air heat treatments at 150°C have no effect on the device performance.

Figure 6-6. Bifacial I-V curves for a device which was not heat treated prior to immersion in Br_2-CH_3OH : a) illuminated through CdS and b) illuminated through the Cu/Au contact.

Figure 6-7. Bifacial I-V curves for the device of Figure 6-2 after immersion in $\text{Br}_2\text{-CH}_3\text{OH}$ solution for 5 seconds: a) illuminated through the CdS and b) illuminated through the Cu/Au contact.

6.4.6 Application to Other CdTe Materials

Using electrodeposited films prepared and heat treated by AMETEK and using the contact and post deposition treatments described above, a cell was made with: $V_{oc} = 782$ mV; $J_{sc} = 19$ mA/cm² and FF = 70.8%. This demonstrates for the first time that CdTe layers deposited by vastly different techniques can be modified by the same post deposition treatments to produce devices with comparable performance.

Electrodeposited films initially contain a significant quantity of excess Te as-deposited which is eliminated in the post deposition processing. We also fabricated devices using CdTe/CdS provided by Photon Energy and obtained comparable V_{oc} and J_{sc} to devices fabricated wholly at Photon Energy. This indicates a broad tolerance of CdTe device performance to initial composition and structure of CdTe.

6.4.7 Discussion

The effects of the 400°C air heat treatment in the presence of a CdCl₂ on the CdS/CdTe materials are summarized in Section 6.4.2. After Cu/Au contacts are applied to heat treated CdTe, the devices initially exhibit low J_{sc} and uniform collection when illuminated from either side of the device. After a mild heat treatment (150°C) the overall collection improves when illuminated through the CdS side, and the blue response decreases for illumination through the Cu/Au contact side. Even without detailed device modelling, it is evident that heat treatment forms a p-n heterojunction. The as-deposited device resembles a p-i-n device, especially regarding the symmetry of collection efficiency for the CdS side and Cu/Au side illumination cases. The evolution for p-n behavior is consistent with the CdTe becoming more p-type throughout its bulk. We believe that Cu diffuses into the CdTe from the contact during the 150°C heat treatment, which dopes its p-type and reduces the space charge width.

The chemical treatment with B₂-CH₃OH or N₂H₄ reduces J_o in the device without changing J_L , causing V_{oc} to increase from 650 mV to typically 750 mV. This V_{oc} enhancement may be the result of an increase in effective lifetime due to passivation of grain boundaries by the chemical immersion.

Additionally, chemical immersion causes the contact resistance to decrease as seen in both dark and light I-V curves at $V > V_{oc}$. We believe this is related to formation of an intermetallic compound such as Cu₂Te or AuTe₂ between the CdTe and the contact layers which lowers the contact barrier which reduces the contact resistance thus increasing FF.

6.5 SPATIAL UNIFORMITY

The spatial uniformity of the CdTe samples deposited in a single deposition (8- 1"x1" samples over a 3"x3" area) was characterized with respect to device performance. Each sample was cut in half and given the identical post deposition treatments and contact. The samples were grouped at each processing step to identify possible effects of a particular step. A total of 64 CdTe/CdS cells were made on 16 half pieces, each processed through the CdCl₂ treatment, the 400°C heat treatment, the Cu/Au deposition, the 150°C heat treatment, and the chemical treatment on the same day. There was a significant variation in both V_{oc} and fill factor for devices on a single piece and from sample to sample. However, there was no correlation of device performance with substrate location in the evaporator or specific processing step. The distribution of V_{oc} and FF are shown in Figures 6-8 and 6-9, respectively. The J_{sc} for all cells was approximately 20 mA/cm² with less than 10% variation from cell to cell. Some half pieces exhibit devices having poor spatial uniformity and low overall performance while the other half-piece shows a tighter distribution. A striking example of the differences in uniformity and performance which can occur on two halves of the same 1"x1" substrate is shown in Table 6-4. The substrate was cut in half after the CdTe deposition, and both pieces were processed individually on the same day, as described above.

Table 6-4
Device results for both halves
of piece 40675.12

Piece	Cell #	Voc	Jsc	FF
121	1	567	18	59
	2	585	18	62
	3	598	19	61
	4	665	19	63
122	1	717	20	67
	2	711	20	67
	3	702	20	68
	4	686	20	68

This entire study was repeated with another set of CdS/CdTe pieces from a similar CdTe deposition, and similar results were found.

We conclude that non-uniformity from piece to piece is a result of a process step which is unique to each piece, most likely the CdCl₂ application and drying. Partly as a result of this study,

Figure 6-8. Histogram of V_{oc} for all devices fabricated from a single CdTe deposition and processed at the same time.

Figure 6-9. Histogram of FF for all devices fabricated from a single CdTe deposition and processed at the same time.

we developed the improved CdCl_2 drying procedure described in Section 6.4.1. Reproducibility and uniformity from piece to piece increased significantly.

6.6 ALTERNATE WINDOW LAYERS

Various TCO materials were investigated as alternatives to CdS as window layers. We evaluated the following materials by depositing CdTe directly on the TCO/glass substrate: ITO (sputtered at IEC); SnO_x (supplied by Solarex Thin Film Division); and ZnO (sputtered at IEC) on ITO or SnO_x . Standard ITO/CdS substrates were run as controls.

The various combinations of window layers were evaluated using five CdTe depositions and Table 6-5 summarizes the I-V parameters. In some cases, data for the CdTe/CdS control cell is also shown. Control pieces had V_{oc} between 0.6 and 0.7V. Pieces with the alternative window layers had V_{oc} below 0.4V and low FF (<50%) as well. However, J_{sc} of 24 mA/cm^2 was obtained with some SnO_x window layers as shown in Table 6-5. The increase in J_{sc} was due to an increase in the QE below 500 nm.

Table 6-5. I-V parameters for CdTe devices with alternate window layers.

Device	Date	Structure	V_{oc}	J_{sc}	FF	
40491.322-3	04/19/89	SnO_x/CdTe	410	23	-	†
40470.222-1	04/19/89	ITO/CdTe	330	17	-	†
40651.322	05/25/89	SnO_x/CdTe	410	22	50	
40651.321	05/25/89	SnO_x/CdTe	440	24	53	
40651.231	05/25/89	SnO_x/CdTe	320	21	-	†
40656.12-1	08/07/89	CdS/CdTe	624	17	55	
40656.31-1	08/07/89	SnO_x/CdTe	318	15	38	
40657.21-4	08/07/89	CdS/CdTe	672	17	62	
40657.12-1	08/07/89	$\text{SnO}_x/\text{ZnO}/\text{CdTe}$	231	21	37	
40657.13-2	08/07/89	ITO/ZnO/CdTe	276	20	39	

† Incomplete data sets are for cells measured on a single bulb ELH simulator and are thus only relative measurements.

6.7 CdS/CdTe DEVICE ANALYSIS

I-V measurements of high efficiency ($\eta \sim 10\%$) CdTe/CdS solar cells both in light and dark give effective diode quality factors between 1.5 and 2.0. These devices do not exhibit superposition. V_{oc} vs. T measurements yielded intercepts (barrier heights) between 1.3 and 1.4 eV. These measurements also depend on

illumination intensity (lower barrier heights with lower intensity). The measurements suggest that the CdTe is photoconductive in its high efficiency state. High values of (dJ/dV) at J_{sc} suggest a voltage dependent current collection ($J_L(V)$) mechanism as well.

Analysis of selected high efficiency cells shows that the FF and the resistance at V_{oc} (R_{voc}) are generally not correlated. $J(V)$ testing of these cells as a function of illumination intensity was performed at room temperature to determine the components of R_{voc} , more specifically to separate the non-light dependent component from the light dependent and diode component as we did previously (49). While this work is not yet completed, we have observed some notable results so far:

- 1) The light dependent component of R_{voc} is not correlated with the CdTe thickness, 1.5 to 3.5 microns and thus is not due to CdTe bulk photoconductance.
- 2) The light dependent component is not correlated with the Au thickness, 10 to 50 nm.
- 3) The various R_{voc} components are the same for recent high efficiency cells using the Cu/Au contact as for those reported in reference 2 for cells using the Cu/ITO contact. Yet, the FF is higher in the recent cells (60-70% versus 55-60%), therefore other parameters have been improved with the present optimization process.

Device analysis will continue and will be enhanced by the improvements in cell reproducibility. Emphasis will be on the evolution of the junction properties during fabrication/optimization and on identifying V_{oc} -limiting mechanisms.

6.8 STABILITY

Toward the end of this contract, we began to study the stability of CdTe devices stored in air. We found preliminary evidence of device instability in V_{oc} and FF by examining moderate efficiency (~9% cells) over periods of 3 to 9 months. Particular attention was given to differences in their CdTe and contact processing. Both CdTe/CdS samples prepared at IEC and Ametek were evaluated using either a Cu/Au contact or ZnTe:Cu contact. The primary difference between the stable and degraded cell was the type of contact, with the stable cells having a ZnTe:Cu contact. (Cell 40661.12-2 was an exception, i.e., a stable high efficiency device with a Cu/Au contact.)

Understanding the degradation mechanism(s) is far from clear at present. For example, a cell on 40579-231 remained stable at

7.5% while the best cell decreased by 25%. Several cells with $\eta > 10\%$ from different CdTe runs with the IEC Cu/Au contact show little or no degradation over 6 months. The modes of degradation vary as well. Some devices develop curvature in the light I-V beyond V_{oc} , others do not. In some cases the loss is primarily in FF, other cases V_{oc} , and others show losses in both V_{oc} and FF. J_{sc} tends to remain constant or even increase slightly. Degradation does not seem to correlate with CdTe deposition conditions. Both EV4 and EV5 material (1989 or 1986 vintage, respectively) exhibit the effect.

The data we have gathered to date suggests that the ZnTe:Cu contact, which has Cu but no Au, produces more stable devices than Cu/Au.

A substantial body of literature exists which links Au contacts with instability in CdTe cells (28,50-52). Since the Au contact is implicated in device degradation, we cannot be certain to what extent it influences initial device performance. Thus, alternative contacts such as Mo, ITO, Ni, or ZnTe:Cu are being examined.

6.9 HIGH EFFICIENCY CELL RESULTS

Samples were sent to SERI for testing soon after the new back contact process was developed. The highest efficiency measured at SERI was 9.6% on 50246-31-2, having $V_{oc}=729$ mV, $J_{sc}=18.95$ mA/cm², and FF=69.0%.

Cells were also fabricated during the contract period (Jan. 89 to Jan. 90), with CdTe were deposited in 1986. Devices made at that time were only in the 6-7% range. However, this same CdTe material was found to be capable of much higher efficiency with the new post-deposition processes. This also shows that ITO/CdS/CdTe material is stable over several years of storage in air. We also note that no high efficiency devices produced from July until November. We attribute this in part to the high humidity during the summer and fall which influenced the CdCl₂ drying before oven drying became a standard procedure, as discussed in Section 6.4.

6.10 CONCLUSIONS

We have developed a post deposition process for making a nearly 10% efficient thin-film CdS/CdTe device using CdS and CdTe layers prepared by PVD. By demonstrating high efficiency devices using CdTe and CdS deposited by evaporation and electrodeposition, we have shown that the CdTe and CdS deposition methods used are not as critical to the fabrication of high efficiency devices as might be expected. Instead, we find the post-deposition

processing steps are more crucial to the performance of devices. The post-deposition processing steps we investigated are: 1) CdCl_2 coating; 2) heat treatment; 3) contacting; 4) mild heat treatment; and 5) reactive chemical treatment.

Heat treating CdTe with a CdCl_2 coating increases CdTe grain size and interdiffuses Te and S. Without the CdCl_2 coating, higher temperatures ($T > 500^\circ\text{C}$) are needed to produce these changes. Reproducible device results have been obtained using CdTe heat treated with CdCl_2 .

Bifacial I-V and spectral response analyses show that the as-deposited devices operate in a p-i-n mode. After a mild heat treatment, which we believe diffuses Cu from the contact into the CdTe, the CdTe layer becomes more p-type, resulting in p-n device operation. Immersion of the devices into reactive liquids such as $\text{Br}_2\text{-CH}_3\text{OH}$ or $\text{N}_2\text{H}_4\text{-H}_2\text{O}$ results in V_{oc} enhancement and improvement of the contact. The relatively rapid effect of the chemical treatment suggests action through and along grain boundaries which results in a reduction in J_0 , hence the V_{oc} enhancement. AES and SIMS analysis indicate a sharp reduction in Cd at the near-surface region of the CdTe which makes conditions favorable for formation of Cu and Au tellurides, both of which form ohmic contact to p-type CdTe, hence the improved contact.

Observed variations in spatial uniformity and reproducibility do not appear to be related to CdTe evaporation or contact metallization, but rather are affected by interaction of the CdCl_2 with ambient humidity. Controlled drying of the CdCl_2 is important to maintain reproducibility, and increases overall performance as well.

Stability of the device performance over time is of concern. Preliminary studies suggest that the degradation is related to the contact, not the CdTe material.

Future work will include detailed examination of the role and influence of the CdCl_2 layer on the recrystallization of the CdTe; the influence of the 400°C heat treatment atmosphere on the CdCl_2 -CdTe interaction; the physical, chemical, and electronic action of the chemical immersion step on the near-surface properties of the CdTe and contact metals; and analysis of V_{oc} -limiting mechanisms.

SECTION 7.0

DEVICE ANALYSIS

The primary limitation on the efficiency of thin film CuInSe_2 polycrystalline solar cells is low open circuit voltage (V_{oc}). By analyzing the current-voltage (I-V) behavior and spectral response of thin film $\text{CuInSe}_2/(\text{CdZn})\text{S}$ solar cells, it has been possible to determine and quantify the mechanisms controlling device behavior under illumination and suggest possible improvements to enhance V_{oc} .

Previous measurements and analysis (53,54) have indicated that the open circuit voltage is limited by recombination in the space charge region. More recent analysis has focussed on quantifying this behavior with further analysis done on devices under various degrees of optimization (heat treatments) as well as accurate determinations of diffusion lengths and optical absorption coefficients as a function of processing (55,56).

7.1 Bifacial SPECTRAL RESPONSE

A method has been developed to determine the minority carrier diffusion length in operating $\text{CuInSe}_2/(\text{CdZn})\text{S}$ polycrystalline thin film solar cells. The technique involves measuring the spectral responses through both the $(\text{CdZn})\text{S}$ front side of the device and the semi-transparent molybdenum-glass back side. The simultaneous measurement of the quantum efficiency through both sides (bifacial) along with measurements of the optical transmission of the window layers and substrate allow the calculation of both the diffusion length and the absorption coefficient of the CuInSe_2 . For a typical high efficiency CuInSe_2 device, a diffusion length of $1.5 \mu\text{m}$ is obtained.

Thin film $\text{CuInSe}_2/\text{CdS}$ heterojunction solar cells have reached efficiencies around 14% (57) but device performance has been limited by low open circuit voltage. The low open circuit voltage has been shown to be due to Shockley-Read-Hall recombination in the CuInSe_2 (53). This recombination may be reduced by narrowing the space charge region in the CuInSe_2 . But first, the amount of current collected by this region must be determined in order to find the loss in current that would result from a narrowing of the space charge region.

In addition, it has been shown that the composition of CuInSe_2 in high efficiency solar cells can vary appreciably (57,58), while the optical absorption coefficient of CuInSe_2 is expected to change with composition (59). Therefore, the determination of collection width and diffusion length must be made without any prior assumptions of the CuInSe_2 optical absorption.

In order to do this, the diffusion length and space charge collection width should be measured on a finished device. This can be done by measuring the spectral response through both sides (bifacial) of a completed solar cell.

Spectral response is measured through both the ITO/(CdZn)S (frontwall) and 7059/Mo (backwall) sides of the device. By measuring and subtracting the optical losses due to the window layer and the semi-transparent back contact, one can determine both frontwall and backwall internal quantum efficiencies.

It is assumed that the minority carrier collections is controlled by a space charge collection region near the CuInSe₂/(CdZn)S heterojunction and diffusion. It is further assumed that the Mo contact is acting as a high recombination surface. Then, the following formulas apply (60):

Frontwall

$$\begin{aligned} \text{Internal Q.E. through (CdZn)S} &= 1 - \exp(-\alpha w) + \frac{\alpha L \exp(-\alpha w)}{\alpha^2 L^2 - 1} \\ &\quad \left\{ \alpha L - \frac{[\cosh(d/L) - \exp(-\alpha d)]}{\sinh(d/L)} \right\} \end{aligned} \quad (7.1)$$

Backwall

$$\begin{aligned} \text{Internal Q.E. through Mo} &= \frac{\alpha L}{\alpha^2 L^2 - 1} \\ &\quad \left\{ \frac{[1 - \exp(-\alpha d) \cosh(d/L)]}{\sinh(d/L)} - \alpha L \exp(-\alpha d) \right\} + \exp(-\alpha d) [1 - \exp(-\alpha w)] \end{aligned} \quad (7.2)$$

where: d = thickness of field free collection region

w = thickness of space charge collection region

t = thickness of CuInSe₂ = d + w

α = absorption coefficient of CuInSe₂ = α(λ)

L = diffusion length

Using equation 7.1, one can find α for each quantum efficiency measurement if a diffusion length (L) and space charge collection width (w) are assumed. Using these values in equation 7.2, one can predict a backwall internal quantum efficiency and compare it with the measured value.

This process can be repeated with adjusted values of diffusion length and space charge collection width until the predicted backwall quantum efficiency agrees with the measurement.

In this way, one determines the absorption coefficient ($\alpha(\lambda)$), diffusion length (L), and space charge collection width (w) from the bifacial spectral response measurements.

The following optical transmission measurements were done on separate window layer films that were deposited in the same way as on the final device. Unless otherwise stated, the quantum efficiency measurements reported here were made on device #32026-23-9 under AM1.5 white light bias without voltage bias.

Figure 7-1 shows the frontwall optical transmission through the ITO/(CdZn)S window layer. When the external quantum efficiency is corrected for these losses, one gets the internal quantum efficiency shown in Figure 7-2. Similar analysis done with the backwall 7059/Mo layers (Figure 7-3) lead to the internal quantum efficiency curves shown in Figure 7-4.

Using equations 7.1 and 7.2, a diffusion length of $1.5 \mu\text{m}$ and a space charge collection width of $0.03 \mu\text{m}$ give the predicted backwall quantum efficiencies which are shown along with measured values in Figure 7-5. The resulting optical absorption coefficient is shown in Figure 7-6. The optical absorption coefficients extending over three orders of magnitude agree well with published data (61).

Table 7-1 shows the results of this type of computation applied to quantum efficiency measurements done at various conditions of reverse voltage bias and illumination. Although not shown, the agreement between predicted and measured backwall quantum efficiencies is similar to that shown in Figure 7-5. The previous sections have shown that bifacial spectral response in conjunction with optical measurements can be used to determine the current collecting parameters and optical absorption of an operating photovoltaic device.

Specific measurements and analysis of semi-transparent CuInSe_2 /(CdZn)S devices have yielded results consistent with a diffusion length $\sim 1.5 \mu\text{m}$ and a negligible space charge collection width $< 0.1 \mu\text{m}$ under normal operating conditions of the solar cell. These results support the band gap profiling approach for achieving improved V_{oc} without loss in J_{sc} outlined in Section 3.

7.2 EFFECT OF OXIDATION-REDUCTION HEAT TREATMENTS ON CuInSe_2 /CdS DEVICE BEHAVIOR

In general, varying degrees of oxidizing heat treatments (e.g., 200°C in air for several hours) are commonly used to optimize

Figure 7-1. Optical transmission through ITO/(CdZn)S (frontwall) window layer corrected for reflection losses.

Figure 7-2. Measured quantum efficiency (external) through ITO/(CdZn)S of Device #32026-23-8 with AM1.5 light bias and no voltage bias with quantum efficiency corrected for window layer optical losses (internal).

Figure 7-3. Optical transmission through semi-transparent 7059 glass/Mo (backwall) substrate corrected for reflection losses.

Figure 7-4. Quantum efficiency through ITO/(CdZn)S and 7059/Mo corrected for optical losses.

Figure 7-5. Measured and predicted backwall quantum efficiency for $L = 1.5 \mu\text{m}$ and space charge collection width $\sim .03 \mu\text{m}$.

Figure 7-6. Calculated absorption coefficients with $L=1.5 \mu\text{m}$ and space charge collection width $\sim 0.03 \mu\text{m}$.

Table 7-1
Device #32026-23-8

ILLUMINATION (μm)	BIAS VOLTAGE (V)	SPACE CHARGE COLLECTION WIDTH
Dark	0.0	0.00
White Light AM 1.5	0.0	0.03
"	-0.5	0.09
"	-1.0	0.12
"	-1.5	0.13
"	-2.0	0.14
"	-2.5	0.14

Space Charge Collection Width as a Function of Light and Voltage
Bias from Bifacial Spectral Response with $L = 1.5 \mu\text{m}$

CuInSe₂/CdS device parameters (58). Consequently, various groups (62-64) have studied the influence of different atmosphere heat treatments. We continue our investigation (64) of the effect of reducing heat treatments (i.e., 200°C in H₂ for several hours).

Previous studies (64) have reported that oxidation-reduction heat treatments primarily affect the resistivity of the CuInSe₂ layer. For example, the dark resistivity was found to increase by around 2 orders of magnitude following reducing heat treatments. The CuInSe₂ Fermi level, E_{fp}, is shifted towards the middle of the bandgap as the device is reduced. The position of the CuInSe₂ Fermi level not only affects the junction characteristics of the CuInSe₂/CdS heterojunction but also influences the Mo/CuInSe₂ back contact behavior. A quantitative discussion of the effect of reducing heat treatments follows.

Spectral response and temperature dependent current-voltage (I-V vs. T) measurements were carried out as a function of oxidation-reduction heat treatments. Devices were heat treated in air or H₂ at 200°C in order to achieve oxidized or reduced states, respectively. As noted previously, spectral response and I-V characteristics of the CuInSe₂/CdS heterojunction solar cell were completely reversible during the oxidation-reduction cycle.

The mechanisms governing the CuInSe₂/CdS device behavior at various stages of the oxidation-reduction cycle were investigated by analyzing the I-V vs. T characteristics. In the oxidized state, the CuInSe₂ resistivity is low and a back diode in series with the CuInSe₂/CdS main heterojunction has a negligible collection width. But as the device is reduced, the CuInSe₂ resistivity increases, resulting in increased long wavelength collection efficiency due to extended collection width the CuInSe₂/CdS heterojunction. Typically, V_{oc} is low in the reduced devices, J_{sc} remains nearly the same and we observe increased J_o. A large decrease in V_{oc} (ΔV_{oc} ~ 0.3 V) in a highly reduced device is mainly due to the photovoltaic contribution of the back diode, caused by the increased collection width at the back contact diode. The low temperature forward bias I-V vs. T characteristics are analyzed to obtain the back diode parameters as the device is cycled through oxidized and reduced states.

Hence, the oxidizing-reducing heat treatments allow us to study CuInSe₂/CdS device characteristics and the rectifying CuInSe₂/Mo back contact corresponding to varying carrier concentration in CuInSe₂ with relative ease. Our study also indicates that the p-CuInSe₂ layer needs to reach a certain thickness (>1 μm, approx.) such that the collection width at the back diode has negligible contribution with respect to the CuInSe₂/CdS heterojunction.

In the earlier work (57), the current-voltage (I-V) behavior in high efficiency CuInSe₂/CdS solar cells was investigated in

detail and modelled in terms of a back diode at the Mo/CuInSe₂ interface in series with the main heterojunction of the solar cell.

I-V characteristics at various stages of the reducing heat treatment are presented in Figure 7-7. Figure 7-8 illustrates the I-V curves of a partially reduced device as a function of temperatures. As reported before (53,64), the open circuit voltages (V_{oc}) decrease when the device is reduced and the activation energy, ϕ extrapolated from V_{oc} vs. T plots also decreases (Fig. 7-9). Device behavior is first analyzed in the oxidized state and a modified quantitative model is proposed to describe the I-V characteristics in reduced state.

Based on analysis of I-V vs. T characteristics, the I-V relation for the CuInSe₂/CdS heterojunction in presence of light can be represented as follows:

$$J = J_o [\exp(qV_{HJ}/AkT) - 1] - J_L \quad (7.3)$$

and the symbols have their conventional meaning. A progressive increase in the blocking behavior with reduction in temperature is observed in all devices (oxidized/reduced) and a back diode in series with the main heterojunction solar cell has been considered (64,53).

Hence, the equivalent circuit model describing the CuInSe₂/CdS device characteristics is shown in Figure 7-10 and the voltage measured across the device is the sum of voltages across the main heterojunction solar cell, V_{HJ} , series resistance term, $R_s J$ and the back diode, V' .

$$\begin{aligned} V &= R_s J + V_{HJ} + V' \\ &= R_s J + (AkT/q) \ln(1 + (J_L + J)/J_o) \\ &\quad - (A' kT/q) (\ln(1 + (J_L' - J)/J_o')) \end{aligned} \quad (7.4)$$

where: $J_o = J_{oo} \exp(-q\phi/AKT)$

$$\text{and: } J_o' = J_{oo}' \exp(-q\phi'/A'KT) \quad (7.5)$$

The I-V' relation describing the back diode introduces a light generated current, J_L' depending on the collection width at the back (i.e., Mo/CuInSe₂ contact) and is given by:

$$J = J_L' - J_o' [\exp(-qV'/AkT) - 1] \quad (7.6)$$

Note: OXIDIZED = 200°C/AIR
REDUCED = 200°C/H₂

Figure 7-7. Current-voltage (I-V) characteristics of a .08 cm² device at room temperature in 1) oxidized state 2) moderately reduced state and 3) highly reduced state.

Figure 7-8. I-V characteristics as a function of temperature (I-V vs. T) of a partially reduced device measured under ELH illumination.

Figure 7-9. ϕ_{oxidized} and ϕ_{reduced} obtained from V_{oc} vs. T measurements.

A' and ϕ' are the diode ideality factor and activation energy characterizing the back diode, respectively.

Thus, from equation (2)) the V_{oc} measured across the device is given by:

$$V_{oc} = V_{oc}(HJ) - V_{oc}' \\ = (AkT/q) \ln(1 + J_L/J_o) - (A' kT/q) \ln(1 + J_L'/J_o') \quad (7.7)$$

or using equation (7.5)

$$V_{oc} = \phi - \phi' - (AkT/q) \ln(J_{oo}/J_L) + (A' kT/q) \ln(J_{oo'}/J_L') \quad (7.8)$$

The various symbols used in the above equations are defined as:

J_L = Light generated current
 J_o = Reverse saturation current
 A = Diode ideality factor
 ϕ = Activation energy
 R_s = Series resistance

and primed symbols are pertinent to the back diode.

Differentiating equation (7.4) and with respect to J and evaluating it at $V = V_{oc}$ results in

$$(dV/dJ)_{V_{oc}} = R_s + AkT/qJ_L + A' kT/qJ_o' \quad (7.9)$$

Using the main heterojunction parameters, measured values of $(dV/dJ)@ V = V_{oc}$ and assigning reasonable values for back diode parameters A' and J_L' , J_o' can be calculated as a function of temperature. Therefore, a quick way of estimating ϕ' associated with the back diode is possible by using equation (7.9) and obtaining ϕ' from $\ln(J_o')$ vs. T values.

The device parameters obtained in the oxidized and reduced case are listed in Table 7-2.

(a) Oxidized Device

The main heterojunction device parameters are obtained from I-V data at higher temperatures where the contribution due to the back diode can be neglected. From Figure 7-9, the activation energy, ϕ , is $\phi_{oxidized} \approx 1.0$ eV = bandgap of $CuInSe_2$. At lower temperatures, the I-V characteristics of the back diode are obtained by subtracting off the contribution of the $CuInSe_2/CdS$ main heterojunction (calculated from device parameters ϕ , A , J_{oo} , J_L obtained at high temperatures) and plotting the remainder.

EQUIVALENT CIRCUIT MODEL

Figure 7-10. Equivalent circuit model describing the $\text{CuInSe}_2/\text{CdS}$ device in oxidized and reduced states.

Figure 7-11 shows the J vs. V' plots as a function of temperature where the back diode indicate $J_L' \approx 0$. This is consistent with the earlier work (7.1) on high efficiency $\text{CuInSe}_2/\text{CdS}$ devices. Hence, $J_L' \approx 0$, $A' = 1$ and $\phi' \sim 0.2$ eV characterize the back diode for the oxidized device.

(b) Reduced Device

As the device is reduced, the resistivity of the CuInSe_2 increases, thus extending the collection widths at both the main $\text{CuInSe}_2/\text{CdS}$ heterojunction and the $\text{Mo}/\text{CuInSe}_2$ back diode. This introduces a non-zero $J_L' \sim 5 \text{ mA/cm}^2$ associated with the back diode and from equation (7.7) it is obvious that $J_L' \neq 0$ lowers the measured V_{oc} of a reduced device. Again, at higher temperatures, $J_L' \ll J_o'$ and $V_{oc}' \approx 0$.

The activation energy, ϕ_{reduced} extrapolated from V_{oc} vs. $T > \phi - \phi' = 0.88 \pm 0.04 \text{ eV}$. Thus, the main heterojunction (Table 7-2) is still governed by SRH recombination with $\phi \approx 1.0 \text{ eV}$ and $A \approx 2$. The lower value of ϕ_{reduced} is due to the back diode which affects the measured V_{oc} . The I - V' plots (Figure 7-12) are obtained as before and definitely indicate $J_L' \neq 0$; the device parameters characterizing the back diode are consistent with metal-semiconductor contact behavior. Hence, as the device is reduced, the back diode in series with the main heterojunction has a photovoltaic contribution.

On examining the I - V behavior in the oxidized state ($V_{oc} \approx 0.42 \text{ V}$), moderately reduced state ($V_{oc} \approx 0.30 \text{ V}$) and highly reduced state ($V_{oc} \approx 0.15 \text{ V}$) illustrated in Figure 7-8, it is evident that the forward bias blocking behavior at room temperature is most prominent in moderately reduced devices. At room temperature in the oxidized device, J_o' is large and governed by thermionic emission (53) i.e., J_o' is dominated by the exponential term, $\exp(-q\phi'/A'kT)$. An increase in the dark resistivity of CuInSe_2 indicates a shift of the Fermi level towards the middle of the gap as a consequence of reducing heat treatments. Thus, when the device is gradually reduced, E_f moves upwards in CuInSe_2 and decreases the electric field E in the semiconductor near the Mo boundary. The reduced device reaches a stage where J_o' drops rapidly as diffusion dominates (65) and J_{oo}' is controlled by an effective diffusion velocity, V_d , which is apparent as an increase in forward bias blocking behavior in the moderately reduced device at room temperature. In strongly reduced devices, E_f is shifted further towards the middle of the CuInSe_2 bandgap and the dark I - V characteristics show highly resistive behavior.

At this point, the contribution of the back diode can be neglected in comparison to the bulk resistivity, thus explaining the absence of blocking behavior.

TABLE 7-2. Device parameters of a $\text{CuInSe}_2/\text{CdS}$ heterojunction solar cell in oxidized and reduced states.

Device Parameters	OXIDIZED	REDUCED
	MAIN HETEROJUNCTION	
J_L (mA/cm^2)	33.7	33.7
R_s (Ωcm^2)	0.4	1.0
A	1.7	1.8
ϕ (eV)	1.0 ($E_g \text{ CuInSe}_2$)	1.0 ($E_g \text{ CuInSe}_2$)
J_{oo} (mA/cm^2)	4.3×10^7	6.0×10^7
	BACK DIODE	
ϕ' (eV)	0.2	0.2
A'	1.0	1.0
J_L' (mA/cm^2)	~0	~5

Figure 7-11. J vs. V' characteristics of the back diode when the device is in oxidized state and $J_L' \approx 0$.

Figure 7-12. J vs. V' characteristics of the back diode showing $J_L' \sim 5$ mA/cm² when the device is reduced.

Spectral response measurements of the device during an oxidation-reduction cycle are shown in Figure 7-13. A gain in long wavelength response (1000 - 1300 nm) occurs for the device in a reduced state, which is consistently observed in other high efficiency devices subjected to the reducing heat treatment. The shift in E_f towards the middle of the gap produces a weaker field in the CuInSe_2 , but extends it further into the bulk of the CuInSe_2 layer. The extended collection width results in increased minority carrier collection in the long wavelength region. A loss in short wavelength response is observed in many reduced devices. The weaker electric field at the $\text{CuInSe}_2/\text{CdS}$ junction may increase loss of photogenerated carriers due to recombination at the heterojunction.

In summary, current-voltage measurements on $\text{CuInSe}_2/\text{CdS}$ solar cell during oxidation-reduction heat treatments have yielded the following:

1. I-V vs. T behavior of the $\text{CuInSe}_2/\text{CdS}$ device in oxidized and reduced states can be modelled in terms of:
 - (a) a $\text{CuInSe}_2/\text{CdS}$ heterojunction governed by Shockley-Read-Hall recombination in the CuInSe_2 with $\phi \approx 1.0\text{eV}$ and $A \approx 2$.
 - (b) a back diode in series with the heterojunction characterized by $\phi' \approx 0.2\text{eV}$ and $A' = 1$ and which has a photovoltaic contribution (i.e., $J_L' \neq 0$) as the device is reduced.
2. Changes in blocking behavior of the back diode as a function of heat treatment at room temperature is explained in terms of the variation of carrier concentration in CuInSe_2 . Spectral response of reduced devices indicates enhanced minority carrier collection in the long wavelength region due to extended collection width of the main heterojunction.

Therefore, current-voltage behavior of $\text{CuInSe}_2/\text{CdS}$ heterojunction solar cells during an oxidizing-reducing heat treatment can be quantitatively modelled by considering the change in resistivity of the CuInSe_2 and its effect on the collection widths at both the $\text{CuInSe}_2/\text{CdS}$ main heterojunction and the back diode. All results from current-voltage and spectral response measurements are consistent with $\text{CuInSe}_2/\text{CdS}$ device models based solely on the movement of CuInSe_2 fermi level as a function of the oxidation-reduction heat treatment.

SPECTRAL RESPONSE

Figure 7-13. Normalized spectral response of a device during an oxidation-reduction cycle.

7.3 FUTURE WORK

The previous sections have shown that the oxidizing and reducing heat treatments can be used to control the space charge width in the CuInSe_2 . This fact coupled with the diffusion lengths $> 1.0 \mu\text{m}$, suggest that it may be possible to put at least some of the V_{oc} lowering space charge region into the window layer in order to increase V_{oc} .

Also, I-V and spectral response analyses are applicable to the CdTe/CdS devices and will be necessary for establishing the efficiency limiting mechanisms in these devices.

SECTION 8.0

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