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PHOTOVOLTAIC MECHANISMS IN POLYCRYSTALLINE THIN FILM
SILICON SOLAR CELLS

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By
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THIN FILM SILICON SOLAR CELLS

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FOR PERIOD

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MOTOROLA PROJECT NO. 2386

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Polycrystalline silicon is inherently a non-uniform material because of the presence of grain boundaries and other structural defects such as dislocations, stacking faults, and twins. A complete analysis of photovoltaic (P.V.) processes that take place in such a material involves two major steps: (i) Identification of the structural defects and an evaluation of the three dimensional nature of the non-uniformities arising due to them and (ii) study of the P.V. mechanisms associated with each type of defects, including kinetic behaviour such as modifications due to high temperature device processes. Detailed data thus obtained can serve as feedback for improved substrate growth and solar cell process optimization.

An experimental approach, developed by the Motorola Solar Energy R&D Group, to isolate the influences of each type of defect on cell parameters, consists of fabricating and analyzing small area diodes, and correlating their characteristics with the substrate structure underlying the diodes. Advantages of this approach, as well as correlation between structural defects and cell parameters, have been described in previous reports. It was, however, indicated that, due to the relatively large edge effects on small diodes, open circuit voltages (as a function of type and density of defects) were only relative. Furthermore, it was also brought out that surface and bulk dislocations influenced the cell parameters to different degrees.

This report describes two major developments in analytic techniques required to achieve the objectives of this approach. These are:

1. Fabrication of high quality small diodes with negligible edge effects.
2. A sectioning technique to determine three-dimensional topography of defects.

These are described in sections 2 and 3 of this report. Section 4 describes a unified approach towards applications of a two-wavelength laser scanner for photovoltaic material/device characterization.

2.0 FABRICATION AND EVALUATION OF SMALL AREA DIODES

In previous reports we have described the advantages of using small area devices for the analysis of P.V. mechanisms in polycrystalline silicon. It was shown that, on a relative basis, the cell parameters of diodes fabricated on a polycrystalline substrate agree well with the defect structure of the substrate underlying the diode. This procedure was used to isolate dependences of J_{SC} , V_{OC} , and F.F. on the type and density of defects. It was, however, found that, due to edge effects, V_{OC} requires a correction in order to predict large area cell performance. Although the data presented previously is very important in determining relative effects, edge effects need to be minimized in order to identify current transport processes using I-V characterization. Consequently, we have investigated various mechanisms that lead to device shunting caused by edge effects. Based on these results, the previous fabrication/evaluation techniques were improved to minimize edge effects. This section describes the sources of major contribution to edge effects in the diodes fabricated by earlier processes (1). A final version of diode fabrication and evaluation procedure is also given.

2.1 MECHANISMS OF EDGE EFFECTS

Three factors observed to contribute to edge leakage (p-type substrates) are:

2.1.1 FORMATION OF AN INVERSION SURFACE LAYER

It is well known that a surface inversion type of layer is formed on freshly etched p-type substrates. (This effect has been used to develop a surface photovoltage in many non-contact techniques for semiconductor characterization.) In a mesa diode, such a layer can be formed at the diode edges, constituting a low

quality diode in parallel with the main diode. Growth of a clean oxide will help in passivating such a surface. This effect on diode characteristics was clearly seen upon removal of the oxide layer. Figure 1 shows a comparison of the dark and illuminated I-V characteristics of a diode with and without an oxide layer. The diode was fabricated on a single crystal Cz wafer by the process described in previous reports. Solid and dashed lines indicate diode characteristics with and without the oxide. This figure clearly shows that removal of the oxide significantly lowers the V_{OC} (as well as F.F.). This loss is accompanied by a slight increase in J_{SC} . We have found that cleanliness of the diode edges before oxide growth, and of the ambient for oxidation, are both important for minimizing edge leakage. Optimum thickness of the oxide is not critical for passivation. However, too thick a layer interferes with current probing of the diode. It is believed that $\sim 100\text{\AA}$ of oxide is well suited for diode analysis.

2.1.2 EDGE QUALITY

Initial experiments with diode fabrication were done using low quality masks as well as non-optimal photolithography. Improvements in mask quality (using high resolution photographic plates), photoresist processing, and etching led to the improved edge quality and hence improved diode performance. It may be emphasized that improvements in edge roughness are limited by the low resolution of the negative photoresists (acid resistant) used as masks for silicon etching. For example, high resolution positive photoresist, AZ1350, is not suitable for silicon etching. Edge resolution obtainable with Waycoat (negative) photoresist using the etching technique described in Section 2.2 is indicated in Figures 2 and 3. Figure 2 shows a photograph of a diode fabricated on a single

FIGURE 1: Comparison of the I-V characteristics of a diode (diameter = 50 mils) with and without a surface oxide.

FIGURE 2: Nomarski photograph of a 50 mil diode
fabricated on a single crystal wafer.

Figure 3: Photographs showing edge roughness of (a) single crystal and (b) polycrystalline diodes.

crystal Cz wafer. Figure 3a shows a high magnification (1000X) optical micrograph of a section of the diode in figure 2. Figure 3b shows a similar micrograph (magnification 400X) of a section of a diode fabricated on an RTR ribbon. The diode of figure 3b was intentionally overetched to show that the substrate defects do not add to the edge roughness (as compared to that of the single crystal diodes).

2.1.3 GENERAL CLEANLINESS OF THE FABRICATION PROCESSES

General cleanliness of processing was found to be essential for obtaining high quality diodes. The tendency of impurities to be trapped at the edges necessitated several cleaning steps commonly employed for micro-fabrication. Of particular importance are precautions described in Section 2.2.3 (on mesa etching) to avoid carrying contamination from the photoresist coated wafer into the etchant.

2.2 DIODE FABRICATION

This section describes various major steps of the procedure evolved to fabricate high quality diodes. Some of the investigations carried out to arrive at optimum processing steps are also included. A major criterion for determination of diode quality was minimum difference ΔV_{OC} between the V_{OC} 's of a large area (typically ≥ 1 inch diameter) and a small area (typically 50 mils diameter) diode. Most of the work on process optimization (to minimize edge effects) was done using single crystal substrates for ease in comparison. However, processes such as surface preparation and orientation dependence of etching characteristics were independently carried out on polycrystalline substrates of RTR ribbons and Wacker Silso. Major process steps that lead to

FIGURE 4: STEPS OF DIODE ARRAY PROCESSING SEQUENCE.

$\Delta V_{OC} < 1$ MV for AM1 illumination are described below (schematically shown in figure 4).

2.2.1 DAMAGE-FREE POLISHING

This is the first step for diode fabrication. Substrates are damage-free polished, by a procedure described earlier, to minimize grain boundary grooving and grain-to-grain height variations (1). In order to confirm the damage-free nature of polishing, the following experiment was carried out. Single crystal Cz wafers (polished by conventional slurry polishing) were cleaved into two halves. One part of each wafer was repolished by the procedure developed for polishing polycrystalline substrates. Large area diodes were then fabricated on all the samples. A comparison of the V_{OC} 's of diodes on the same starting wafers showed no observable difference.

2.2.2 DIFFUSION OF EMITTER REGION

Polished substrates are diffused (unmasked) with appropriate impurities to form a shallow surface junction, ~ 0.5 μm deep. Since most polycrystalline cells use p-type substrates, much of this work was done on p-type material (a limited study was carried out on n-type substrates). A standard n diffusion, using POCl_3 for phosphorus predeposition, was employed for all p-type substrates.

2.2.3 MASKING AND MESA ETCHING

Diffused substrates are coated with photoresist (Waycoat 450) on the side where mesas are to be etched. Although recommended conditions for the photoresist work well, extra post baking ($\sim 180^\circ\text{C}$ for 10 minutes) helps when deeper

($\geq 4\mu\text{m}$) etching is desired. Cleanliness and a pinhole-free photoresist mask are essential to prevent surface degradation during etching.

Mesa etching is done using a $\text{HF}:\text{HNO}_3:\text{CH}_3\text{COOH}$ etchant. Although these types of etchants are very commonly used for polishing and thinning, the following problems arise in masked etching of polycrystalline silicon:

(i) Masking can be done only by photoresist; since the main use of the photoresist is in transfer masking, they are not well suited for silicon etching because (a) photoresists lift-off or dissolve in moderately strong acids, and (b) photoresists act as the source of contamination and often leave residues (particularly for shallow etching).

(ii) Conventional etchants exhibit anisotropic behavior which is undesirable for etching polycrystalline silicon.

We have observed that by selecting the ratio of the constituents of $\text{CH}_3\text{COOH}:\text{HF}:\text{HNO}_3$, etch characteristics can be altered significantly. Two different compositions found suitable for mesa etching are:

A - $\text{HF}:\text{CH}_3\text{COOH}:\text{HNO}_3::36:15:1$

B - $\text{HF}:\text{CH}_3\text{COOH}:\text{HNO}_3::36:15:2$

Etch depth versus time characteristics of these two etchants are shown in figure 5. Clearly, etching by A is more controllable and attacks photoresist to a lesser degree than B. However, A is quite sensitive to contamination which can leave a residue on the sample surface.

Following mesa etching, which also removes the unwanted n^+ region from the sides and back surface, photoresist is stripped off using $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$, and the substrates are given a dilute HF rinse.

FIGURE 5: Plots of etch depth versus time for the two etchants described in the text.

2.2.4 BACK CONTACT FABRICATION

Ohmic contact on the back side is produced by evaporating or sputtering Al. In the former case, alloying is necessary to make an ohmic contact. However, we have found that sputtered Al forms a good ohmic contact on low resistivity ($\sim 1 \Omega\text{-cm}$ or less) p-type substrates. Whenever necessary, Al may be alloyed at about 600°C to form a good ohmic contact.

2.3 DIODE EVALUATION

Evaluation of small diodes requires special caution in probing. We have designed a probe station which allows control of probe pressure; it is adjusted so as to punch through the mesa surface oxide without damaging the devices. Probe alignment, done for one device on each sample, allows the whole array of diodes to be probed. No degradation of diode characteristic was found to take place upon probing.

I-V characteristics of a small area diodes (50 mils) can be determined using a single probe with no series resistance effects. However, for larger devices the use of two probes was found necessary. Figure 6 shows a comparison of illuminated I-V characteristics of a 62.5 mil diode determined by using one and two probes. To avoid these effects, the routine I-V measurements are done by using two-probes.

Using the procedures described in previous sections we have fabricated diodes which exhibit $\Delta V_{OC} \ll 1 \text{ mV}$. Such devices can be analyzed using I-V characteristics to determine carrier transport mechanisms. For example, figure 7 shows dark I-V plots of a 50 mil diode fabricated on a single crystal Cz substrate. The two distinct components of the plot, kT/q and $2kT/q$, show diffusion and junction recombination current components. By using curve fitting

FIGURE 6: ILLUMINATED I-V CHARACTERISTICS OF A MESA DIODE (FABRICATED ON A Cz WAFER) SHOWING DIFFERENCES DUE TO PROBING TECHNIQUES.

FIGURE 7: Log I-V characteristics of a 50 mil diode fabricated on a $1 \Omega\text{-cm}$ Cz wafer.

techniques and temperature dependence of I-V characteristics, contributions to the current by various other mechanisms, such as tunneling and impurity band hopping, can be determined. Currently this approach is being extended to determine transport mechanisms associated with various defects.

2.4 CHARACTERIZATION OF SINGLE CRYSTAL SUBSTRATES BY SMALL DIODES

Due to increasing acceptance of the concept of low-cost substrates (single crystal) it is important to be able to carry out a detailed evaluation of these substrates. In particular, low-cost substrates are expected to exhibit a higher degree of lateral inhomogeneities compared to semiconductor grade substrates. The small diode technique directly lends itself to the detection and analysis of such non-uniformities. Lateral non-uniformities can easily be determined in terms of variations in V_{OC} or J_{SC} .

We have correlated the results of diode analysis on 3 inch wafers with those of large area cells. It was found that wafers which show a large spread in diode parameters make poor solar cells.

3.0 A SECTIONING TECHNIQUE FOR DEMOUNTABLE SEMICONDUCTOR SAMPLES

Analysis of defect and grain structure in semiconductors often involves sectioning (edge polishing) thin samples. In many cases the desirable features of sectioning are:

1. Sample should be demountable
2. Polishing should be damage-free
3. No chipping should occur (i.e. excellent edge quality)

A commonly used procedure for sectioning semiconductor samples consists of molding the sample in epoxy, followed by lapping and grit polishing. Various variations in sample mounting and polishing may be used depending on the type of material and the nature of analysis to be carried out. For example, several different types of epoxies are available which possess different degrees of chemical inertness, presenting the possibility of chemically softening the cured epoxy for sample demounting (2). This conventional procedure presents difficulties as follows:

- a) Mechanical polishing leaves on the surface a residual damage which may interfere with structural details revealed by defect etching. (Although chem. mech. polishing can be used to remove the surface damage, it may not be compatible with epoxy molding).
- b) Grit polishing results in poor edge quality.
- c) Large samples, especially polycrystalline, crack because of stresses present in cured epoxy.
- d) Chemical solutions used for softening a cured epoxy may react with the sample.

This report describes a sectioning technique that we have developed to circumvent the above difficulties. The procedure consists of wax mounting the sample in a suitable chuck followed by chemical-mechanical polishing using Nalcoag slurry. Basic features of a chuck design and the polishing characteristics are described. Some results of defect analysis of thin silicon sheets, afforded by this technique are briefly described.

3.1 SAMPLE MOUNTING AND POLISHING

We describe the design and operation of a chuck for sectioning (i.e. edge polishing) thin semiconductor samples utilizing wax mounting. The chuck provides:

- (i) ease in sample mounting/demounting
- (ii) self alignment of the sample and
- (iii) excellent edge protection during polishing.

A schematic cut-section showing basic features of the sample holder is given in Figure 8. Various parts of the holder are indicated in the figure and are self explanatory. Figure 9 gives an assembly drawing of the chuck. To mount the sample, the spring loaded pressure plunger is pulled out and the sample inserted into the sample chamber. Upon releasing the plunger the sample is held against the pressure pads. The sample holder is now inverted over a gauge block and aligned with one of the machined slots (5, 7 and 10 mils deep). By pulling the plunger temporarily the sample drops into the slot and is aligned for polishing. The sample holder is heated by energizing the heater element (typically 200W power) and chips of wax (glycol pathalate) dropped into the funnel shaped end of the holder. As the wax melts, it fills the sample cavity and flows to the sample end. At this time the heater is turned off and the sample allowed to cool. The sample is then chemically-mechanically polished using Nalcoag Slurry. A laboratory type of polishing machine, with a polyurethane impregnated polyester (such as Suba IV) pad, is well suited for this purpose. The chuck may be hand

A SCHEMATIC CUT-SECTION OF THE CHUCK.

FIGURE 8

ASSEMBLY DRAWING OF THE CHUCK

FIGURE 9

held during polishing with the aid of a supporting ring as shown in figures 8 and 9. Alternately, the supporting ring may be attached to the rocking arm of the machine for semi-automatic polishing. It has been shown that this procedure results in a damage-free surface (3).

To remove the sample after polishing, the chuck is supported on an annular metallic ring (with the sample side down) and reheated. After the wax melts, the pressure plunger is pulled to release the sample. This procedure causes the sample to slide out along with the molten wax, without need for pulling the sample.

3.2 RESULTS

This technique was applied to section several silicon ribbons for defect analysis. Some of these results are described briefly in order to show that (i), this technique results in a damage-free surface with excellent edge quality and (ii) as a consequence of the excellent polishing and sample demountable features of this technique it is possible to analyse defect/grain structure in greater detail than with conventional sectioning. Figures 10a and 10b are Nomarski photographs of two regions of a sectioned ribbon. These photographs clearly show two distinct features of this polishing technique. (i) excellent edge quality and (ii) slight delineation of grain boundaries and twins. Figures 11a and 11b are photographs of the same regions after defect etching; clarity of etch configuration and a lack of surface structure in defect-free regions indicate a damage-free surface.

Ease in sample mounting and demounting, without any appreciable risk of breakage, allows sectioning of the same sample in different directions -- a feature that can be very useful in defect characterization. In order to elucidate the importance of multiple sectioning let us consider a ribbon sample which was sectioned as shown schematically in figure 12. Sectioned planes B and C are, respectively, parallel and perpendicular to the ribbon growth direction,

(A)

(B)

FIGURE 10 PHOTOGRAPHS SHOWING TWO REGIONS OF
A RIBBON AFTER SECTIONING.

(A)

(B)

FIGURE 11 PHOTOGRAPH OF REGIONS SHOWN IN FIGURES 10A AND 10B, AFTER DEFECT ETCHING.

A SCHEMATIC OF A RIBBON SECTIONED IN PLANES B AND C.

FIGURE 12

and normal to the surface A. Figure 12 also shows orientations of these planes. Figures 13a, 13b and 13c show dislocation configurations in the planes A, B, and C respectively. Average dislocation density, n_d in each plane is indicated in figure 13. Notice that figure 13a does not show any definite dislocation structure. However, figures 13b and 13c clearly show that dislocations are of the slip type {parallel to (111) planes along [110] direction}. In addition, more dislocations occur along the growth direction as compared to those normal to the growth direction.

In order to demonstrate the degree of edge preservation, we sectioned a sample which was dislocation etched prior to sectioning. Figure 14 shows photographs of two edges of the sectioned sample revealing the shapes of dislocation pits in the sectioned plane. Notice that sharpness of the dislocation pits is well preserved. Another important observation from figure 14 is that, in this case there is one-to-one correspondence between dislocation pits on edges A and A', indicating that dislocation lines run parallel to the sectioned plane. This is yet another application of sectioning for defect characterization.

FIGURE 13A
MAGNIFICATION: 400X
 $N_D = 1 \times 10^5/\text{cm}^2$

SLIP /

FIGURE 13B
MAGNIFICATION: 400X
 $N_D = 9 \times 10^4$

FIGURE 13C
MAGNIFICATION: 200X
 $N_D = 3 \times 10^5$

FIGURE 13: PHOTOGRAPHS SHOWING DISLOCATIONS IN DIFFERENT PLANES (A) AS-GROWN SURFACE A, (B) SECTIONED PLANE B, (C) SECTIONED PLANE C, NORMAL TO GROWTH DIRECTION AND NORMAL TO A.

SIDE A

SIDE A'

MAGNIFICATION = 1100X

FIGURE 14 PHOTOGRAPHS OF A SECTIONED SAMPLE
 SHOWING PRESERVATION OF DISLOCATION
 FIGURES AND EDGE DURING SECTIONING.

Results described in this report clearly indicate that high quality small area diodes can be fabricated with negligible edge effects. It is shown that these devices can be used to determine carrier transport mechanisms, which, in turn, are related to the nature of defects present in the substrate. The sectioning technique, in conjunction with other techniques described previously, enables a detailed analysis of the nature of defects (and their propagation paths).

Improved diode fabrication and sectioning techniques for defect analysis are now being applied to isolate the electrical behaviour of two types of dislocations (viz line and networks) in RTR ribbons. Although some data have already been collected more work needs to be done in this direction. It is expected that correlation of diode performance with defect structure will lead to the prediction of large area cell performance.

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Applications of a Two-Wavelength Laser Scanner for Material/Device
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Abstract

Applications of a two-wavelength laser scanner for evaluating spatial variations in several material/device parameters in semiconductors are described. Use of two-wavelength scanning ($\lambda = 1.15 \mu\text{m}$ and $\lambda = 6328 \text{ \AA}$) permits excitation and collection of carriers from different depths below the surface of a semiconductor, thereby allowing separation of bulk and near surface (such as a surface junction) characteristics. These characteristics include minority carrier diffusion length, junction recombination, and local variations in photovoltaic effects caused by localized defects, twins and grain boundaries. Laser scanning may be done in two different modes. 1. Carrier generation and collection along the same direction -- in this mode the signal is related to carrier recombination effects. It is shown that the signal due to long wavelength excitation is proportional to the bulk diffusion length. Measurements may be done either on unprocessed substrates using a transparent electrode and capacitive coupling, or following P-N junction formation at the surface. 2. Carrier excitation and collection normal to each other -- this mode is used in unprocessed substrates (single or polycrystalline) to determine lateral variations in the internal fields arising from such effects as impurity inhomogeneities and grain boundaries.

Introduction

Optical techniques constitute an important segment for material/device characterization procedures. Many material/device parameters can be measured utilizing photoexcitation of carriers. Although many previously used techniques were aimed at the analysis of homogeneous materials/devices, recent interest in detecting inhomogeneities and evaluating their influences on device performance has necessitated development of scanning techniques where one can image the variations in important material and device parameters. Lasers are often used as sources of light in high resolution scanning due to the ease in focussing the light beam to a small size. Optical scanning has been used in a variety of ways for examination of various photosensitive materials and devices^{1,2,3}. Most of them use a single wavelength excitation source, usually in the visible range (a HeNe laser $\lambda = 0.6328 \mu\text{m}$). Although such an approach is quite useful for detection of defects and inhomogeneities in devices, detailed analysis of material/device characteristics often requires separation of bulk and surface effects. This can be accomplished (as described in this paper) by scanning the sample with light which will excite the carriers selectively either near the surface or uniformly throughout the bulk. This paper describes various approaches in which a two-wavelength laser scanner can be used for the evaluation of single and polycrystalline semiconductor material quality and device characteristics. Imaging can be obtained for variations in such parameters as minority carrier diffusion length, near surface (e.g. surface junction) recombination, and internal fields arising from the effects of impurity inhomogeneities and grain boundaries. Applications towards the analysis of photovoltaic mechanisms in single and polycrystalline silicon are emphasized.

Description of a two-wavelength laser scanner

Figure 1 shows a schematic of a two-wavelength laser scanner. It consists of two HeNe lasers -- one operating at $\lambda = 1.15 \mu\text{m}$ and the other at $6328 \text{ \AA}$. A light beam from either one of them can be selected by switching the mirror M_1 . The selected beam is focussed by the lens onto a sample located on the computer controlled x-y stage. Positioning of the mirror M_2 must be very precise to allow the colinear propagation of two beams, i.e. the two beams are focussed at the same spot on the stage with a high degree of precision. A chopper may be used for capacitive coupling of the signal from samples which do not have a P-N junction. The signal from the sample is processed to display an image on a storage scope (or an x-y recorder).

The scanning system shown in figure 1 utilizes sample movement as compared to beam deflection (stationary sample) often used in scanning systems. This approach allows high resolution scanning without any beam distortion effects that normally occur in beam deflection systems. Typical beam size used is $\sim 15 \mu\text{m}$, although much smaller focussed spots can be obtained. The scanning rates are inherently slow, typically less than 5 lines/sec.

Signal coupling

Photo-signals from the sample may be d.c. coupled when using a P-N junction device. How-

Figure 1. Schematic diagram of a two-wavelength laser scanner

ever, in the absence of a P-N junction, photo-generated carriers can be collected utilizing a surface inversion layer and a capacitive transparent electrode to determine photo-potential variations. A typical electrode for this purpose is shown schematically in figure 2. It uses a semitransparent top electrode consisting of a glass plate with an ITO layer covered by a thick layer of Ta_2O_5 . The electrode assembly is spring loaded to establish a uniform gap between the semiconductor surface and the electrode. In order to use this mode of coupling, the incident light is chopped and the signal from the sample is fed into a lock-in amplifier for synchronous detection. The output of the lock-in then follows the signal processing for image display.

Figure 2. Vacuum chuck and electrode assembly for photo-response imaging of unprocessed wafers.

Photosignals can be displayed in any one of the following modes (a) isometric display (b) Z-modulation image and (c) line scan. Figure 3 shows examples of these display modes for an n/p mesa diode (50 mil diameter) fabricated on a polycrystalline silicon substrate. Losses due to dislocation boundaries are clearly seen in figure 3. Figure 4 shows an optical photograph of the diode. Structure of the substrate in the region adjacent to the diode,

delineated by the etchant used for mesa fabrication is seen to consist of dislocations and several twins and grain boundaries.

Figure 3. Laser scanned images of a 50 mil diode.
(a) Isometric (b) Z-modulation (c) Line scan along the
where in (b).

Figure 4. An optical micrograph of the 50
mil diameter mesa diode used for
figure 3.

Basic principles of characterization by two-wavelength scanning

Characterization of materials/devices by two-wavelength laser scanning involves measurement of integrated photoresponse from different depths below the sample surface. Let us consider a semi-infinite semiconductor illuminated by a focussed light beam as shown in figure 5. Carrier generation rate due to this illumination is of the form $\alpha G_0 e^{-\alpha z}$, where G_0 and α represent the incident photon flux and the absorption coefficient, respectively. Density of excess carriers at the surface and the current $I(z)$ can be calculated utilizing Green's functions derived by Roosbroeck⁴. Such a procedure is quite involved and will be presented elsewhere. However, for simplicity we can assume that the wavelengths of the lasers used for the scanner are such that $\alpha \rightarrow \infty$ for the short wavelength and beam $\alpha \rightarrow 0$ for the long wavelength beam.

These correspond to excitation due to a point surface source and a line source respectively. Their steady-state carrier distributions have been analysed in detail previously⁵. From these results it can be concluded that the dominant contributions to carrier recombination for short and long wavelength excitations are due to surface and bulk mechanisms respectively.

Scanning may be done in two different modes. 1. Carrier generation (i.e. light propagation) and carrier collection are in the same direction as shown in figure 5a. This mode of operation is commonly used for determination of lateral variations in carrier recombination in devices with a surface junction such as in solar cells. 2. Carrier generation and collection are normal to each other as shown in figure 5b. In this mode of operation, ohmic

Figure 5a. Parallel configuration of generation and collection of carriers.

contacts are fabricated across the sample and the region between them is scanned with a light beam. The signal is generated by lateral variations in the internal fields as a result of the impurity inhomogeneities and the grain boundaries. A typical signal generated across a grain boundary is shown in figure 5c and represents the spatial variation in the grain boundary field.

Figure 5b. Configuration of light for transverse photovoltage technique.

Figure 5c. Signal due to light scan of an unbiased G.B.

It should be emphasized that although spatial variations in the recombination characteristics of a semiconductor will be reflected in both the current and the voltage signal, the former exhibits higher sensitivity. Moreover, current amplitude due to long wavelength excitation is directly proportional to the minority carrier diffusion length. These effects are both demonstrated in figures 6 and 7. Figures 6 and 7 show scanned images of a 50 mil diode, fabricated on a silicon ribbon, under different scanning conditions (indicated in the figures). The diode is located on a grain boundary separating two grains (A and B) as shown in an optical micrograph of the diode, figure 8. Two important conclusions from these figures are: (i) current scan at $\lambda = 6328 \text{ \AA}$ shows higher sensitivity as compared to the voltage scan. Variations in the $\lambda = 6328 \text{ \AA}$ image are due to P-N junction recombination caused by the defects (ii) The $\lambda = 1.15 \text{ \mu m}$ current scan image displays variations in the minority carrier diffusion length. Figure 7b shows the ratio (average response from grain A)/(average response of grain B) to be about 2. From actual measurements, diffusion lengths (L) of the grains A and B were found to be $48 \text{ \mu m}$ and $22 \text{ \mu m}$ respectively i.e. $L_A \approx 2L_B$.

Sample preparation

A two-wavelength laser scanner can be used for a variety of applications involving detection and analysis of material/device inhomogeneities. Sample preparation, in particular for the evaluation of substrate inhomogeneities, plays an important role in obtaining correct results. The following process steps are employed for preparing samples for scanning

1. Polishing the substrate surface to minimize light scattering at the surface as well as reduce carrier recombination velocity at the surface. Although single crystalline samples can easily be polished (or etched) to generate a damage-free surface, difficulties are encountered in polishing (or etching) polycrystalline semiconductors without creating undesirable grooving at the grain boundaries and/or grain-to-grain height variations. These local profiles can lead to unpredictable scattering of the focussed light beam resulting in a change in reflection coefficient as well as a change in the direction of light propagation. Light scattering at a V-groove and at a step are schematically shown in figure 9. To circumvent these difficulties a damage-free polishing procedure was recently

(a) Voltage scan

(b) Current scan

Figure 6. Laser scanned image of the diode at $\lambda = 6328 \text{ \AA}$.

Voltage scan

Current scan

Figure 7. Laser scanned images of the diode at $\lambda = 1.15 \text{ }\mu\text{m}$

Figure 8. Photograph of the diode

developed for polycrystalline silicon⁶.

2. Fabrication of carrier collection region. Three different procedures are used for this purpose, depending on the nature of the carrier collection. (a) In the case of surface photovoltage scanning, the polished sample may be given a simple treatment consisting of a dilute HF dip for P-type silicon and boiling in D.I. Water for n-type silicon. This procedure forms an inversion type of surface layer. (b) A shallow P-N junction (depth $\sim 0.5 \text{ }\mu\text{m}$) may be fabricated on the polished side for direct signal coupling. A procedure found to be very useful in analysing photovoltaic losses due to defects and grain boundaries in polycrystalline silicon consists of fabricating arrays of small area (typically 50 mil diameter) mesa diodes and scanning the selected diodes with two-wavelength laser scanner. This approach has been described previously⁷. Figure 10 shows typical diode arrays on single and polycrystalline silicon substrates. (c) For transverse carrier collection, ohmic contacts can be fabricated in damage-free polished samples by alloying Ni and Al for n-type and p-type silicon substrates respectively.

Figure 9. Light scattering at a (a) V-groove and (b) step.

Figure 10. Photographs showing completed diode arrays on (a) a 3 inch single crystal Cz wafer and (b) a 1 inch square Wacker silso substrate.

Typical applications

This section gives a discussion of some typical applications.

1. **Material inhomogeneities:** Inhomogeneities in substrate material can be due to a host of reasons associated with either growth or subsequent processing involving heat treatments. Defect and impurity segregation are commonly known to occur in Czochralski pulled silicon, resulting in spatial variations in bulk carrier lifetime (or diffusion length). It has been observed that these inhomogeneities can be carried through (perhaps somewhat modified) to the final device leading to device degradation⁸. These inhomogeneities may be studied in the substrate by long wavelength scanning using a capacitively coupled photovoltage signal. Figure 11a shows a three inch diameter silicon wafer with swirl defects; Figure 11b shows the laser scanned image (at $\lambda = 1.15 \mu\text{m}$) of a section of the wafer marked in figure 11a. It should be emphasized that the sample was scanned prior to swirl enhancement annealing. Similar patterns have also been observed in scanned images of solar cells⁸.

Inhomogeneities in polycrystalline substrates, due to grain boundaries, defects, and changes in characteristics resulting from different grain orientations, can also be determined by capacitive coupling. Figure 12 shows a line scan, at $\lambda = 1.15 \mu\text{m}$, depicting diffusion length variations along the width of a silicon ribbon.

2. **Influence of substrate structure on the photovoltaic losses:** Two-wavelength laser scanning is very valuable for the evaluation of photovoltaic losses due to defects and grain boundaries. Figure 13a shows a line scan taken across a 50 mil diode fabricated on a polycrystalline silicon ribbon. Figure 13b shows the structure of the substrate in the vicinity of the diode. The substrate structure is lightly delineated by the etchant used for fabricating mesa diodes. Various twins and dislocation boundaries, and their corresponding locations on the line scan, are indicated in figure 13.

Figure 11. (a) Photograph of a 3 inch diameter silicon wafer with swirl defects.
(b) Diffusion length variations due to swirl defects.

Figure 12. Line scan of SPV response by focussed laser scanner ($\lambda = 1.15 \mu\text{m}$) (Response beyond the edges is due to edge illumination by scattered light).

3. Evaluation of residual surface damage: A residual non-uniform surface damage can be present in semiconductor wafers due to incomplete removal of the saw damage by polishing/etching. Surface damage can often go undetected. When the wafer is processed using thermal treatments, the damage can propagate below the surface into the junction resulting in low performance devices (such as a solar cell). Laser scanning can reveal this effect as a non-uniformity in short wavelength scan (long wavelength response will not suffer to any significant degree). Figure 14a shows a photograph of a solar cell fabricated on a substrate having residual surface damage due to sawing. Figure 14b shows the laser scanned image ($\lambda = 6328 \text{ \AA}$) of the section of the cell indicated in figure 14a. Presence of the surface damage was also confirmed by an alternate method⁹.

4. Imaging grain boundary "activity": We have shown earlier (figure 5c) that a photo-signal can be generated by scanning a grain boundary with a focussed light beam. This principle can be extended to image a grain boundary in terms of the grain boundary "activity" (defined in terms of the photovoltaic loss due to the combined effect of the intrinsic recombination and the barrier height associated with the grain boundary). To image a grain boundary the substrate is damage-free polished and ohmic contacts are fabricated on the polished side surrounding the grain boundary. Figure 15a shows a photograph of a sample with metal contacts. Because of polishing, G.B.s are not seen on the polished side; however, the transmission mode of an IR microscope can be used to photograph the G.B.s. Figure 15b is such a photograph showing G.B.s that run between two contacts. Figure 15c shows an image of the G.B. generated by scanning the region between two contacts with a laser scanner. (An inversion in the G.B. images of figures 15b and 15c is due to the microscope.) An amplitude scan along the direction of the arrow in figure 15c, is given in figure 15d to indicate the relative signal levels at various positions along the G.B. Figure 15c shows an important result: G.B. "activity" may vary along the G.B. length. G.B. imaging can be very useful in evaluating influences of various processing steps on G.B. characteristics.

Figure 13. (a) Line scan showing photocurrent losses at various G.B.s on a diode ($\lambda = 6328 \text{ \AA}$)
 (b) Photograph showing structure of the substrate in the vicinity of the diode.

Figure 14. (a) Photograph of a cell with residual surface damage
 (b) Scanned image of the area marked in (a)

Figure 15a. Photograph of a polished sample with metal contacts.

Figure 15b. IR photograph of the back (unpolished) side of the sample showing G.B.s.

Figure 15c. Light scan mode of the G.B.

Figure 15d. Line scan signal along the arrow in adjacent photograph.

Conclusions

A two-wavelength scanner is effective for detection and analysis of material/device inhomogeneities. Variation in parameters such as minority carrier diffusion length, surface (or junction) recombination, and internal fields, can be studied. Three modes of scanning are used for determining particular parameters. Proper sample preparation is particularly important. This procedure has been applied to the detection and analysis of swirl defects, residual surface damage, photovoltaic losses due to crystalline defects and grain boundaries, and imaging grain boundary "activity".

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